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EZR32HG Wireless MCUs
EZR32HG220 Data Sheet

EZR32HG220 Wireless MCU family with ARM Cortex-M0+ CPU and sub-GHz Radio

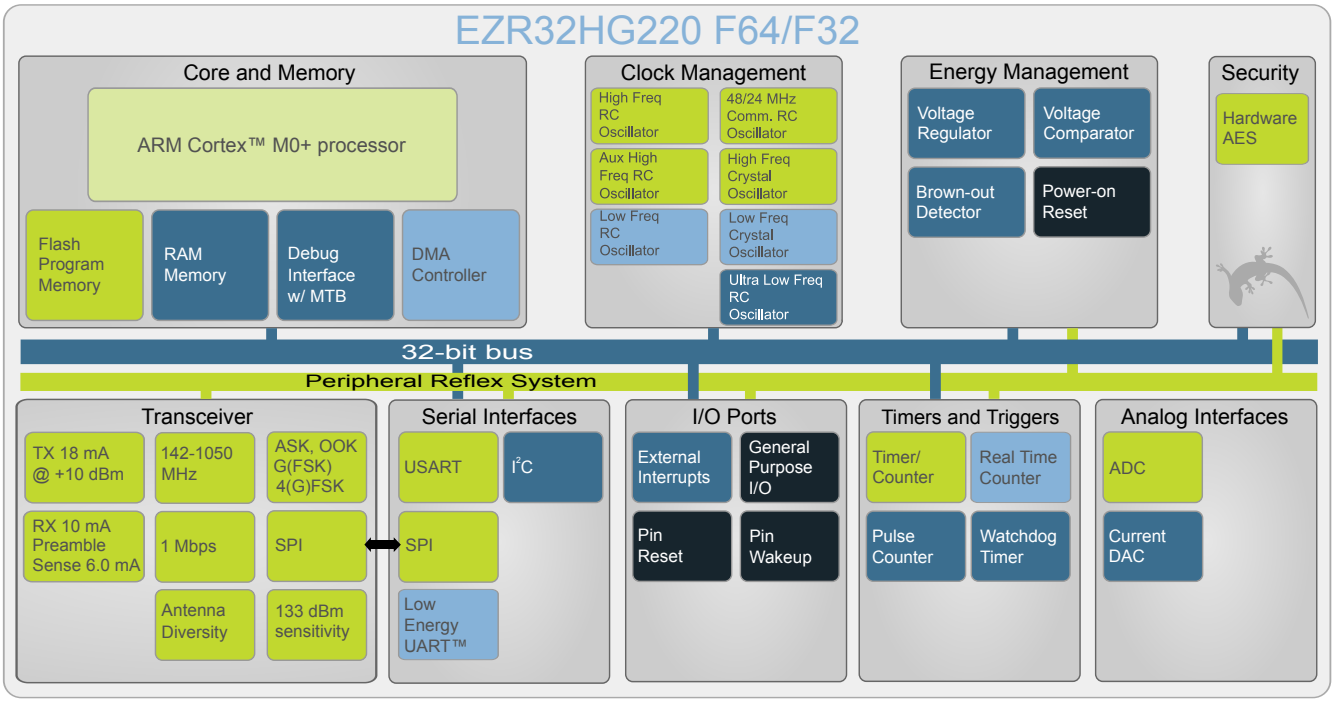
The EZR32HG Wireless MCUs are the latest in Silicon Labs family of wireless MCUs delivering a high performance, low-energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit MCU, the EZR32HG family provides designers the ultimate in flexibility with a family of pin-compatible devices that scale with 64/32 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times of the Silicon Labs energy friendly 32-bit MCUs, combined with the low transmit and receive power consumption of the sub-GHz radio, result in a solution optimized for battery powered applications.

32-Bit ARM Cortex wireless MCUs applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Consumer electronics
- Alarm and security systems
- Building and home automation

KEY FEATURES

- Silicon Labs' energy efficient 32-bit Wireless MCUs
- Based on ARM Cortex M0 CPU core with 64 kB of flash and 8 kB RAM
- Best-in-class RF performance with EZradio and EZRadioPro transceivers
- Ultra-low power wireless MCU
  - Low transmit and receive currents
  - Ultra-low power standby and sleep modes
  - Fast wake-up time
- Rich set of peripherals including 12-bit ADC and IDAC, multiple communication interfaces (UART, SPI, I2C), multiple GPIO and timers
- AES Accelerator with 128-bit keys



1. Feature List

The HG highlighted features are listed below.

MCU Features

- ARM Cortex-M0+ CPU platform
  - Up to 25 MHz
  - 64/32 kB Flash w/8 kB RAM
  - Hardware AES with 128-bit keys
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode
  - 127 µA/MHz @ 3 V Run Mode
- Timers/Counters
  - 3× Timer/Counter
  - 3×3 Compare/Capture/PWM channels
  - Real-Time Counter
  - 16/8-bit Pulse Counter
  - Watchdog Timer
- Communication interfaces
  - 1× USART (UART/SPI)
  - 1× Low Energy UART
  - 1× I2C Interface with SMBus support
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s ADC
  - On-chip temperature sensor
  - Current Digital to Analog Converter
- Up to 27 General Purpose I/O pins

RF Features

- Frequency Range
  - 142-1050 MHz
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK, OOK
- Receive sensitivity up to -133 dBm
- Up to +20 dBm max output power
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm
  - 6 mA @ 1.2 kbps (Preamble Sense)
- Data rate = 100 bps to 1 Mbps
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- IEEE 802.15.4g compliant

System Features

- Power-on Reset and Brown-Out Detector
- Debug Interface
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- QFN48 package

2. Ordering Information

The table below shows the available EZR32HG220 devices.

Table 2.1. Ordering Information

Ordering	Radio	Flash (kB)	RAM (kB)	Power Amplifier (dBm)	Max Sensitivity (dBm)	Supply Voltage (V)	Package
EZR32HG220FxxR55G-B0	EZRadio	32-64	8	+13	-116	1.98 - 3.8	QFN48
EZR32HG220FxxR60G-B0	EZRadioPro	32-64	8	+13	-126	1.98 - 3.8	QFN48
EZR32HG220FxxR61G-B0	EZRadioPro	32-64	8	+16	-126	1.98 - 3.8	QFN48
EZR32HG220FxxR63G-B0	EZRadioPro	32-64	8	+20	-126	1.98 - 3.8	QFN48
EZR32HG220FxxR67G-B0	EZRadioPro	32-64	8	+13	-133	1.98 - 3.8	QFN48
EZR32HG220FxxR68G-B0	EZRadioPro	32-64	8	+20	-133	1.98 - 3.8	QFN48
EZR32HG220FxxR69G-B0	EZRadioPro	32-64	8	+13 & 20	-133	1.98 - 3.8	QFN48

Table 2.2. Flash Sizes

Example Part Number	Flash Size
EZR32HG220F32R55G	32 kB
EZR32HG220F64R55G	64 kB

Note: Add an "(R)" at the end of the device part number to denote tape and reel option.

Visit www.silabs.com for information on global distributors and representatives.

3. System Overview

3.1 Introduction

The EZR32HG220 Wireless MCUs are the latest in the Silicon Labs family of wireless MCUs delivering a high-performance, low-energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit ARM Cortex-M0+, the EZR32HG family provides designers with the ultimate in flexibility with a family of pin-compatible parts that scale from 32 to 64 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times combined with the low transmit and receive power consumption of the sub-GHz radio result in a solution optimized for low power and battery powered applications. For a complete feature set and in-depth information on the modules, the reader is referred to the *EZR32HG Reference Manual*.

The EZR32HG220 block diagram is shown below.

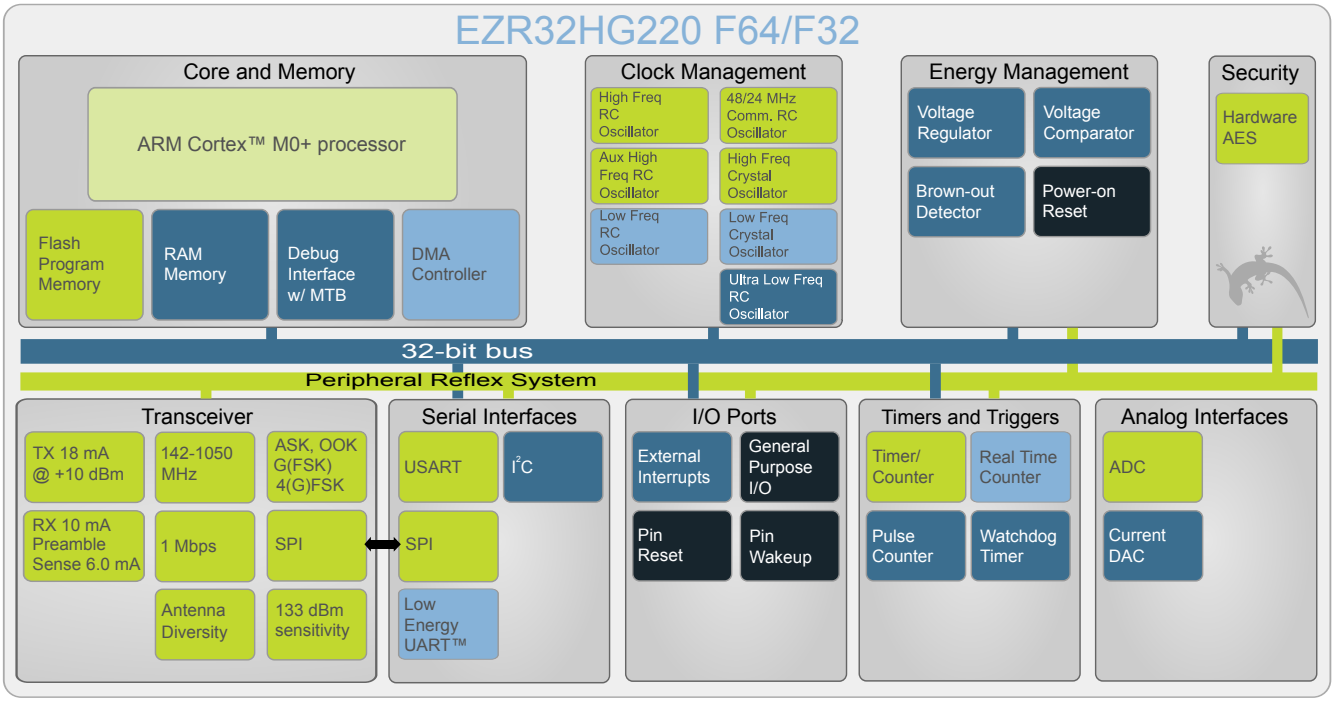


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EZR32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

3.1.2 Debugging Interface (DBG)

These devices include hardware debug support through a 2-pin serial-wire debug interface.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EZR32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks: the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving, for instance, data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The Reset Management Unit (RMU) is responsible for handling the reset functionality of the EZR32HG.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manages all the low energy modes (EM) in EZR32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EZR32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may, for example, be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

3.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note *AN0003* is pre-programmed in the device at the factory. Autobaud and destructive write are supported. The autobaud feature, interface, and commands are described further in the application note.

3.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique Low Energy Universal Asynchronous Receiver/Transmitter (LEUART™), the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.17 Voltage Comparator (VCMP)

The Voltage Supply Comparator (VCMP) is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.18 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

3.1.19 Current Digital to Analog Converter (IDAC)

The current digital to analog converter (IDAC) can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

3.1.20 Advanced Encryption Standard Accelerator (AES)

The Advanced Encryption Standard Accelerator (AES) performs AES encryption and decryption with 128-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations (i.e., 8- or 16-bit operations are not supported).

3.1.21 General Purpose Input/Output (GPIO)

In the EZR32HG220, there are 27 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.22 EZRadio® and EZRadioPro® Transceivers

The EZR32HG family of devices is built using high-performance, low-current EZRadio and EZRadioPro RF transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. These devices offer outstanding sensitivity of up to –133 dBm (using EZRadioPro) while achieving extremely low active and standby current consumption. The EZR32HG devices using the EZRadioPro transceiver offer frequency coverage in all major bands and include optimal phase noise, blocking, and selectivity performance for narrow band and licensed band applications, such as FCC Part 90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times is optimized for extended battery life in the most demanding applications. The EZR32HG devices can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, and ARIB. All devices using the EZRadioPRO tranceiver are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be programmed and configured via Simplicity Studio, available at www.silabs.com.

Communications between the radio and MCU are done over USART and IRQ, which requires the pins to be configured in the following way:

Table 3.1. Radio MCU Communication Configuration

EZR32HG MCU	RF	EZR32HG Function Assignment
PA2	SDN	GPIO Output
PC0	$_{n}$SEL	US1_CS #5
PC1	SDI	US1_MOSI #5
PC2	SDO	US1_MISO #5
PC3	SCLK	US1_CLK #5
PC4	$_{n}$IRQ	GPIO_EM4WU6 (GPIO Input with IRQ enabled)

3.1.22.1 EZRadio and EZRadioPRO Transceivers GPIO Configuration

The EZRadio and EZRadioPRO Transceivers have 4 General Purpose Digital I/O pins. These GPIOs may be configured to perform various radio-specific functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.

3.2 Configuration Summary

The features of the EZR32HG220 are a subset of the feature set described in the *EZR32HG Reference Manual*. The table below describes device specific implementation of the features.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_CLK0, CMU_CLK1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
UART0	Full configuration with IrDA and I2S	US0_TX, US0_RX, US0_CLK, US0_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
USARTRF1	Reduced configuration	USRF1_RX, USRF1_TX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7, 6, 5, 4, 1, 0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	27 pins	Available pins are shown in 5.4 GPIO Pinout Overview

3.3 Memory Map

The EZR32HG220 memory map is shown below with RAM and flash sizes for the largest memory configuration.

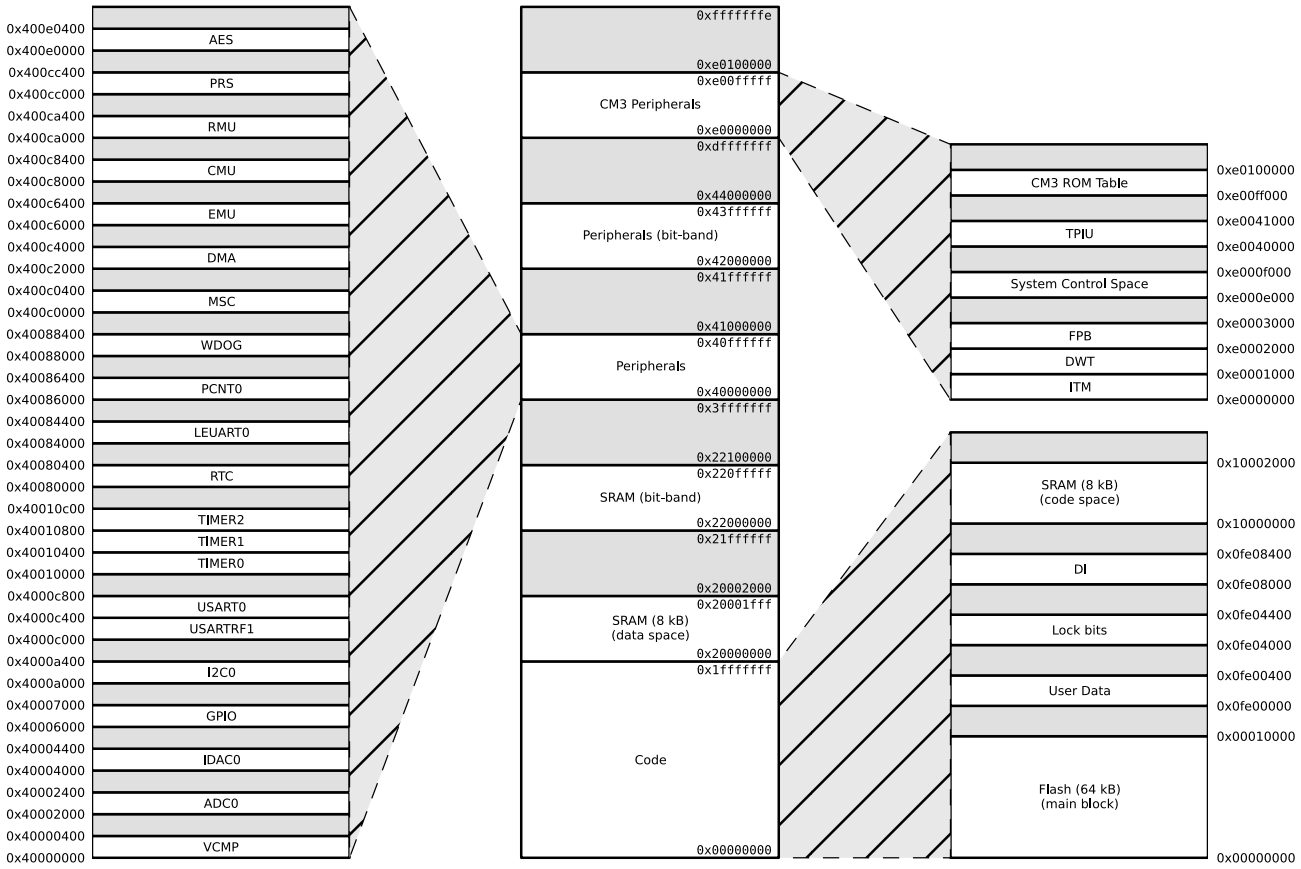


Figure 3.2. EZR32HG220 Memory Map with Largest RAM and Flash Sizes

4. Electrical Specifications

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB} = 25°C and V_{DD} = 3.0 V, as defined in Table 4.3 General Operating Conditions on page 10, by simulation and/or technology characterisation unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 4.3 General Operating Conditions on page 10, by simulation and/or technology characterisation unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the table below may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 4.3 General Operating Conditions on page 10.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-55	—	150[1]	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V

Note:

1. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.3 Thermal Characteristics

Table 4.2. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}		-40	—	85	°C
Junction temperature value	T_J		—	—	105[1]	°C
Thermal impedance junction to ambient	TI_{JA}	+13/+16 dBm on 2-layer board	—	—	61.8	°C/W
		+20 dBm on 4-layer board	—	—	20.7[2]	°C/W
Storage temperature range	T_{STG}		-55	—	150	°C

Note:

1. Values are based on simulations run on 2 layer and 4 layer PCBs at 0m/s airflow.
2. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.4 General Operating Conditions

Table 4.3. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}	-40	—	85	°C
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V
Internal APB clock frequency	f_{APB}	—	—	25	MHz
Internal AHB clock frequency	f_{AHB}	—	—	25	MHz

Latch-up sensitivity passed: ±100 mA/1.5 × V_{SUPPLY}(max) according to JEDEC JESD 78 method Class II, 85 °C.

4.5 Current Consumption

Table 4.4. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash.	I_{EM0}	24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	148	158	µA/MHz
	I_{EM1}	24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	153	163	µA/MHz
	I_{EM2}	24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	161	172	µA/MHz
	I_{EM3}	24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	163	174	µA/MHz
	I_{EM4}	24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	127	137	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	129	139	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	131	140	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	134	143	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	134	143	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	137	145	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	136	144	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	139	148	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	142	150	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	146	154	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	184	196	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	194	208	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM1 current		24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25 °C	—	64	68	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	67	71	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	85	91	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	86	92	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	51	55	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	52	56	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	53	57	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	54	58	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	56	59	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	57	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	58	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	59	63	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	64	68	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	67	71	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	106	114	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	114	126	µA/MHz
EM2 current		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	0.9	1.35	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	1.6	3.50	µA
EM3 current		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	0.6	0.90	µA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	1.2	2.65	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM4 current		V_{DD} = 3.0 V, T_{AMB} = 25 °C	—	0.02	0.035	µA
		V_{DD} = 3.0 V, T_{AMB} = 85 °C	—	0.18	0.480	µA

4.5.1 EM0 Current Consumption

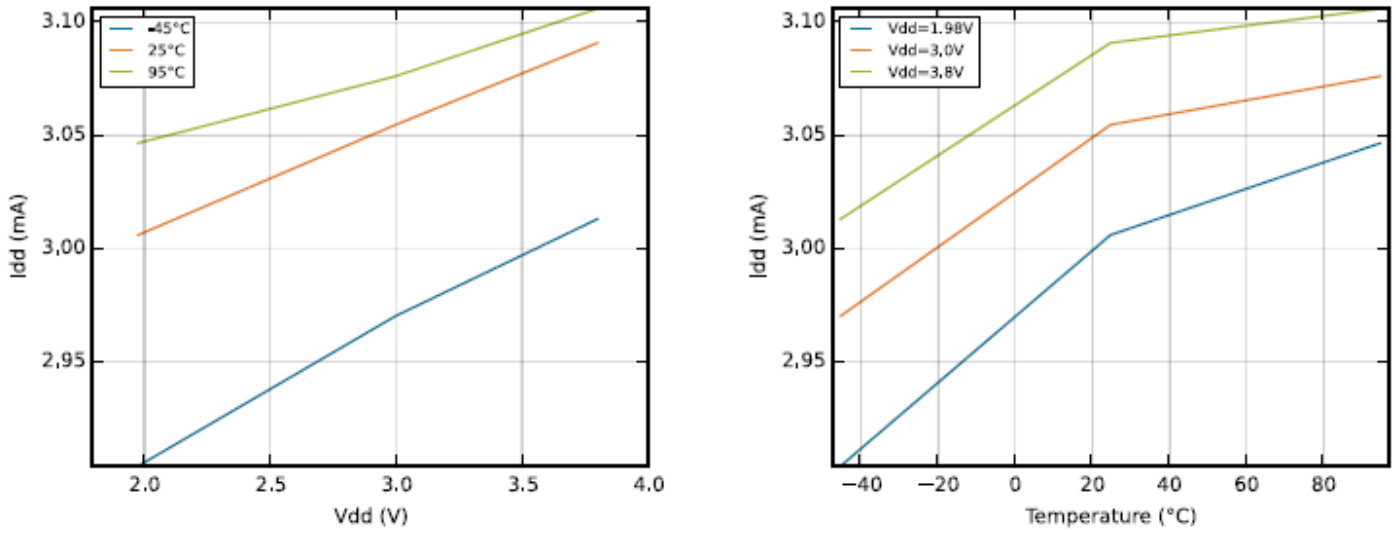


Figure 4.1. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 24 MHz

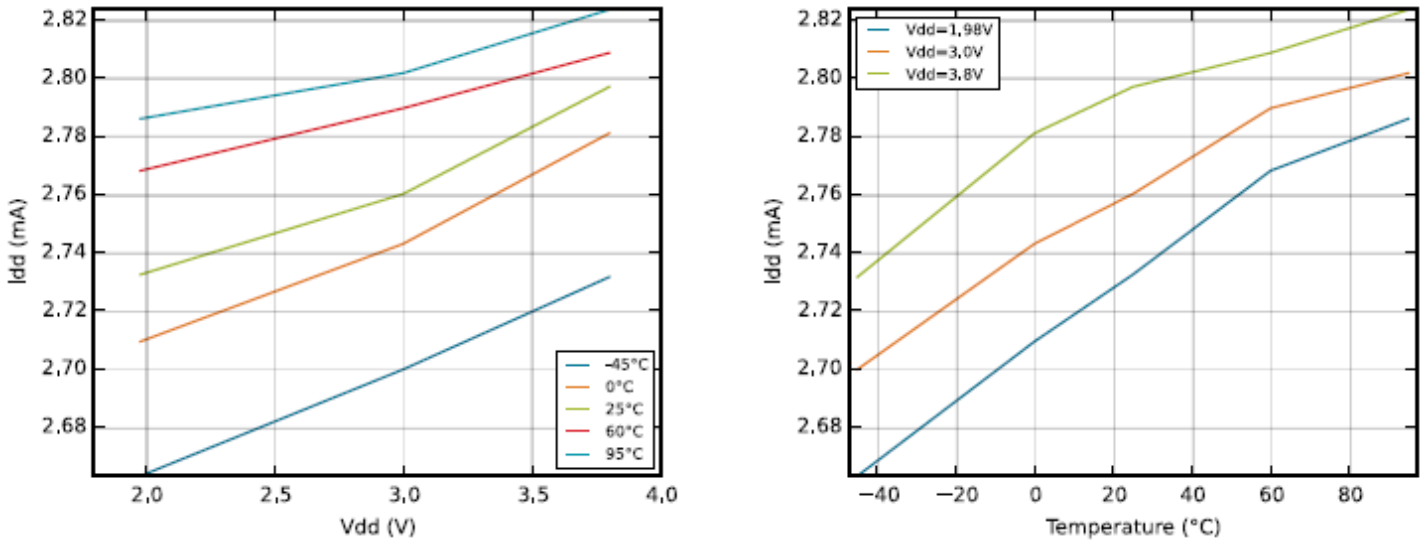


Figure 4.2. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 21 MHz

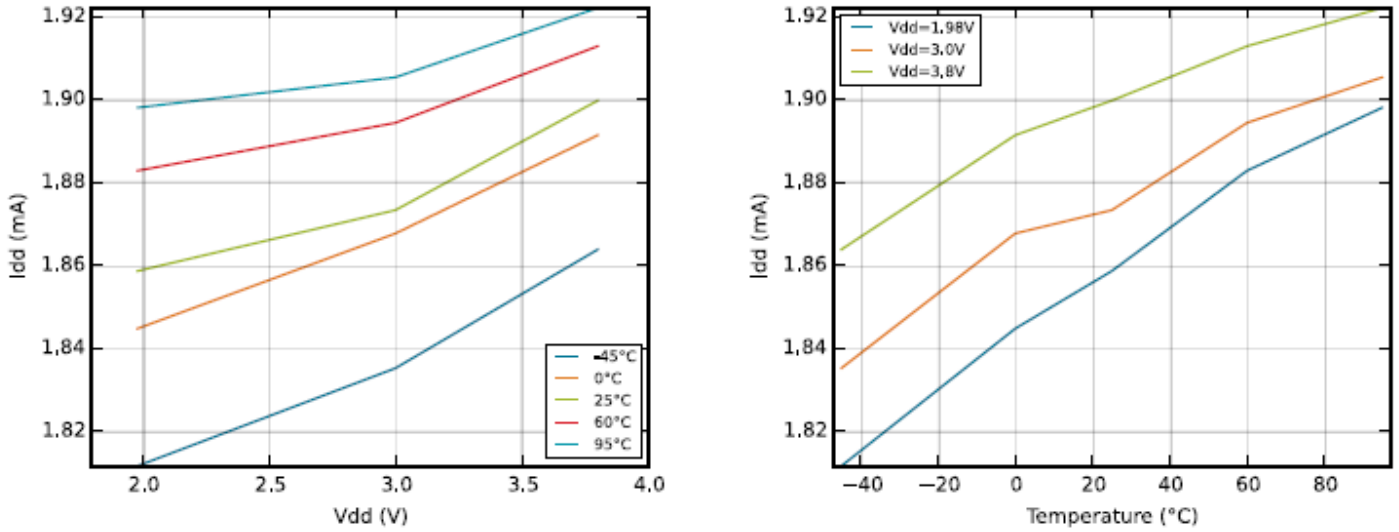


Figure 4.3. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 14 MHz

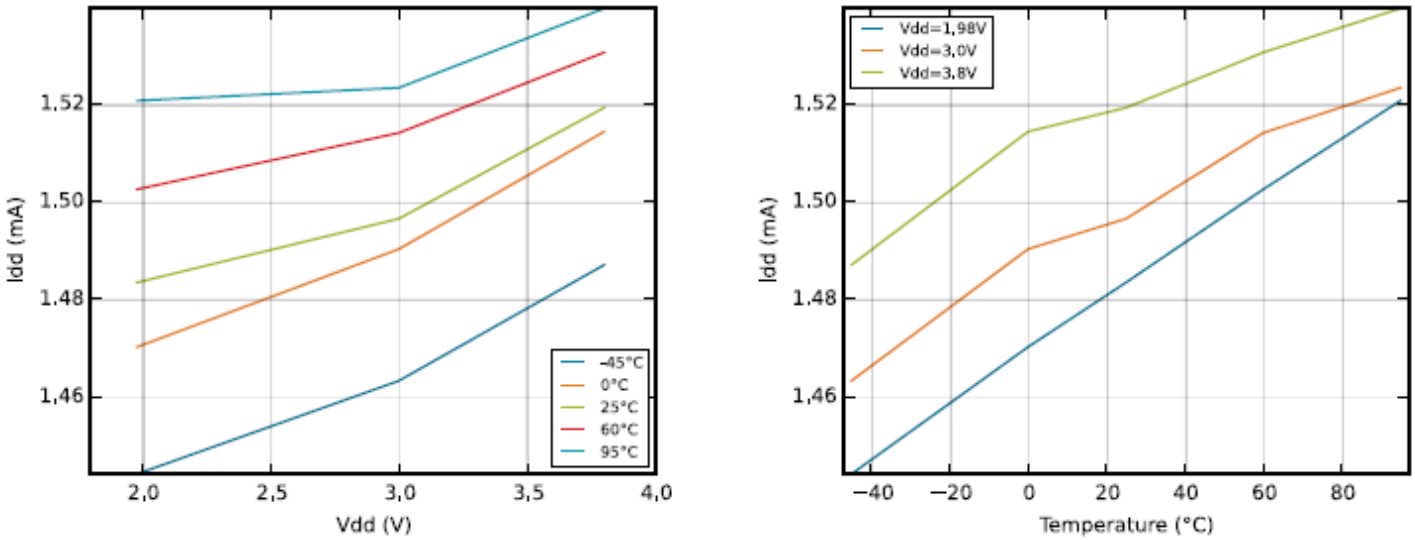


Figure 4.4. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 11 MHz

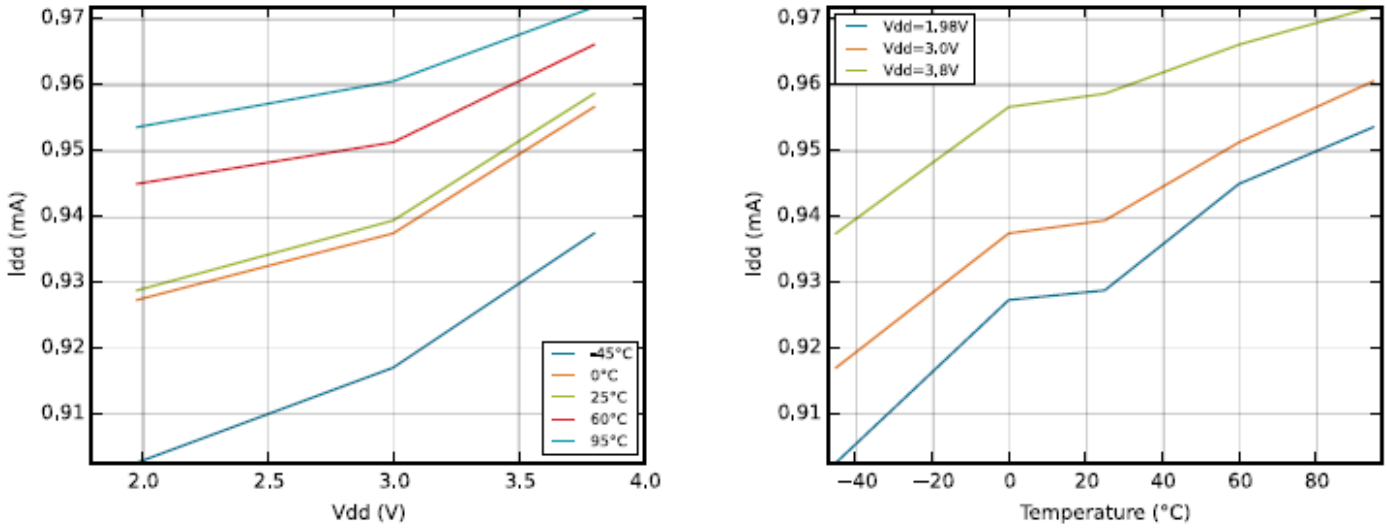


Figure 4.5. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 6.6 MHz

4.5.2 EM1 Current Consumption

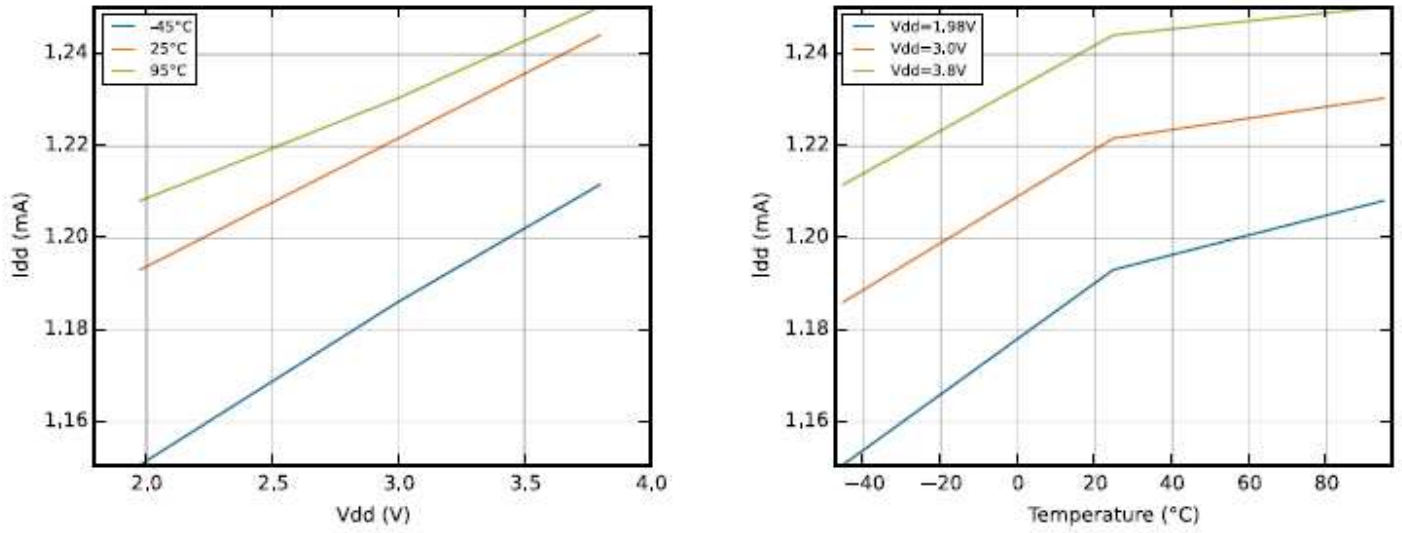


Figure 4.6. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 24 MHz

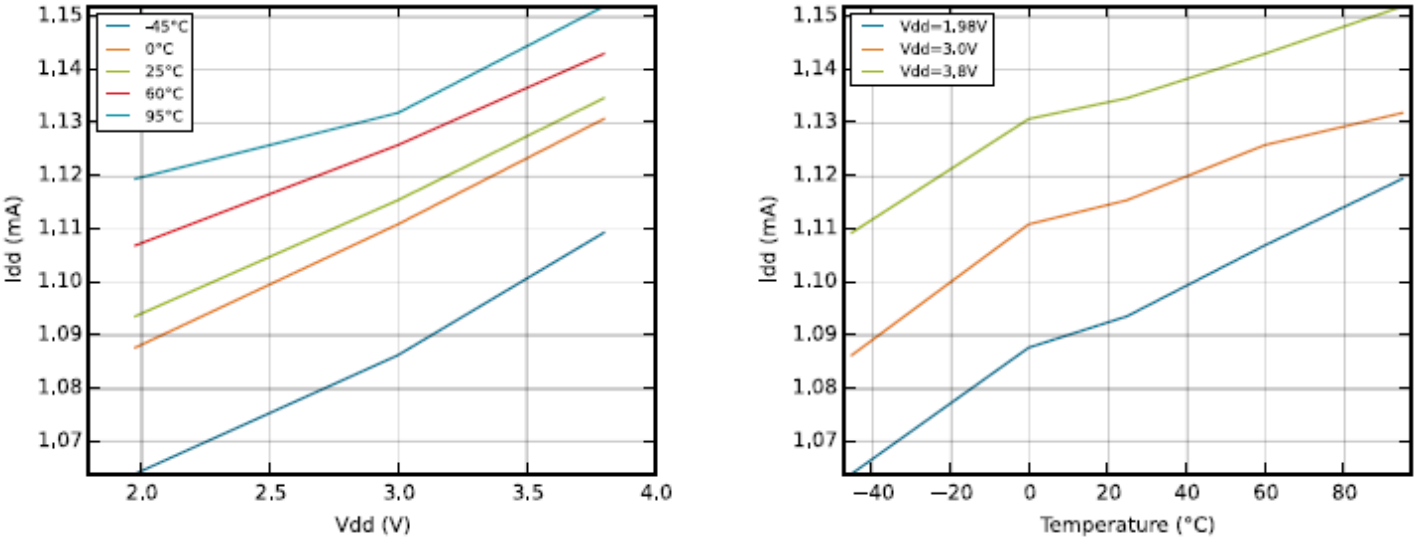


Figure 4.7. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 21 MHz

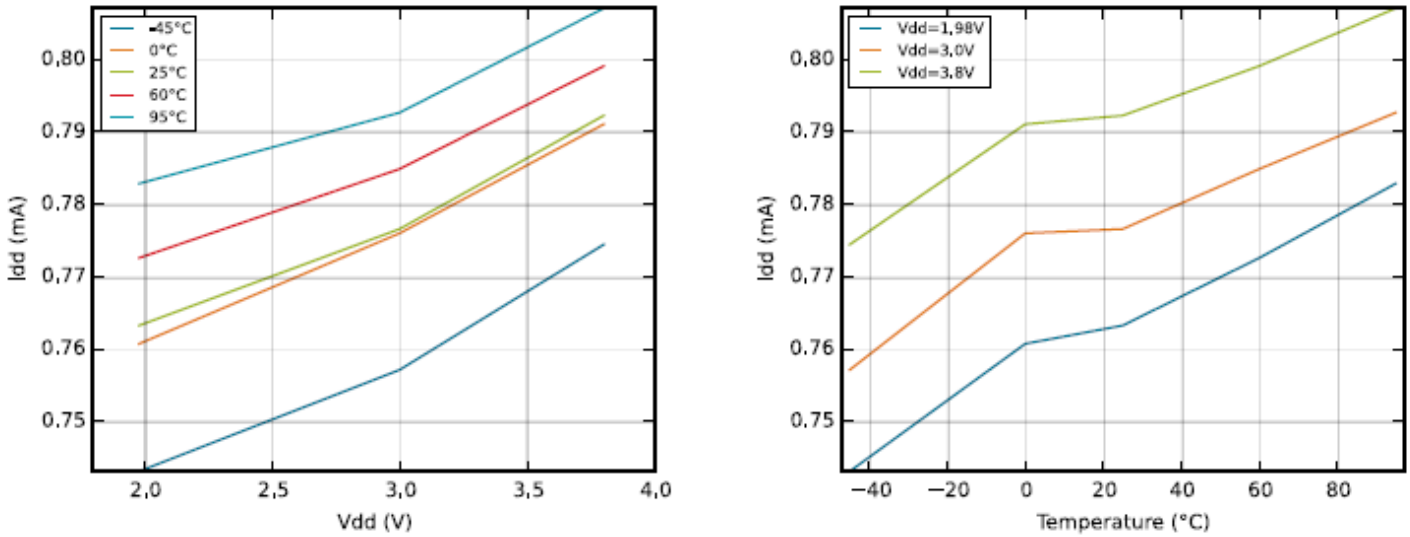


Figure 4.8. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 14 MHz

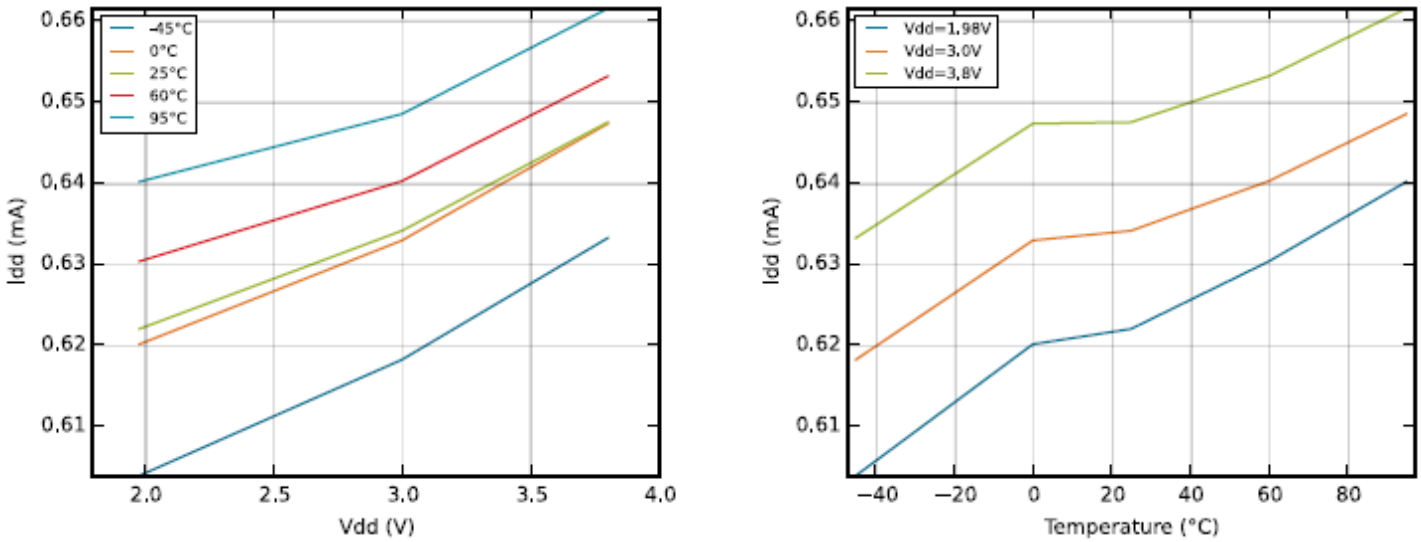


Figure 4.9. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz

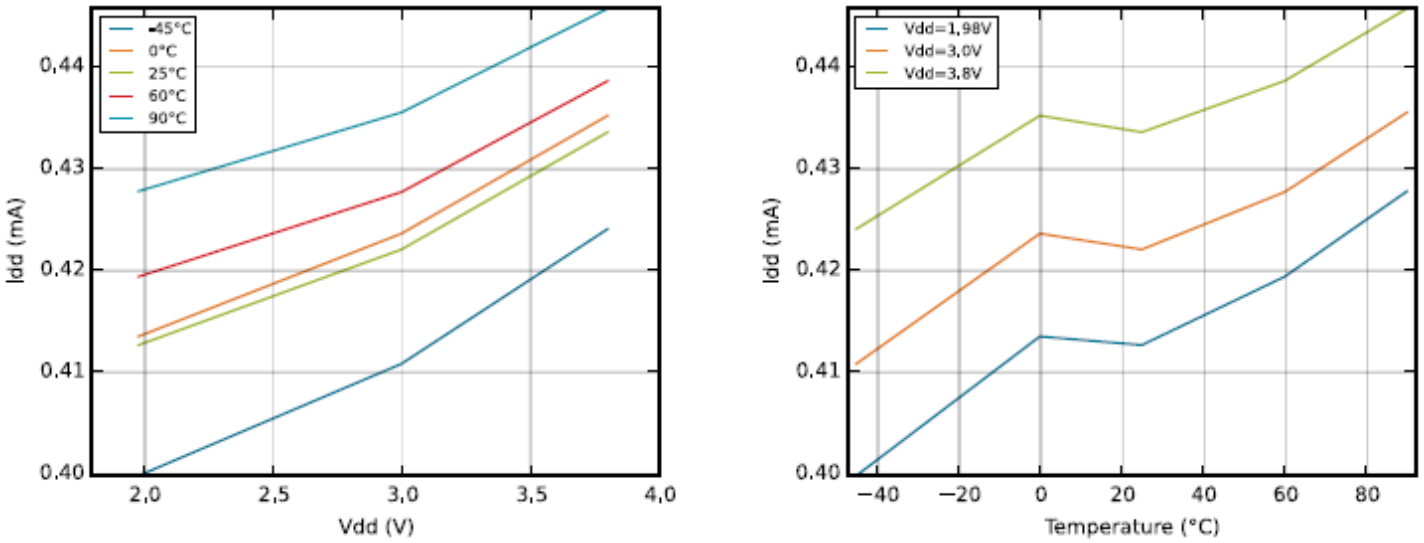


Figure 4.10. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz

4.5.3 EM2 Current Consumption

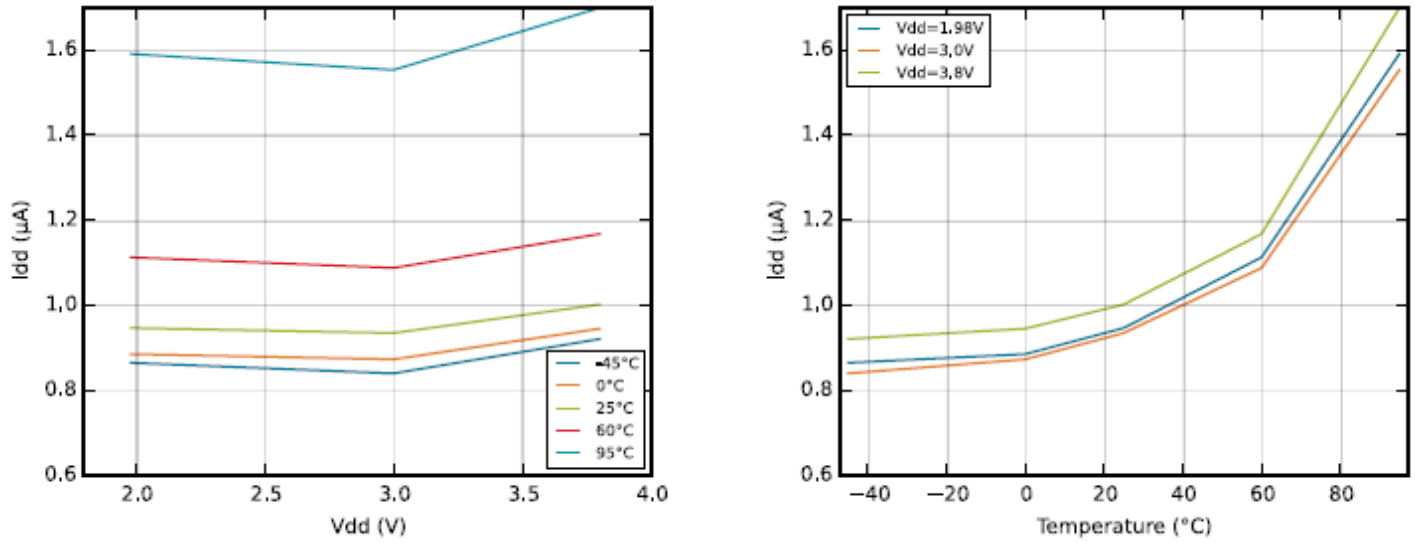


Figure 4.11. EM2 Current Consumption, RTC Prescaled to 1 kHz, 32.768 kHz LFRCO

4.5.4 EM3 Current Consumption

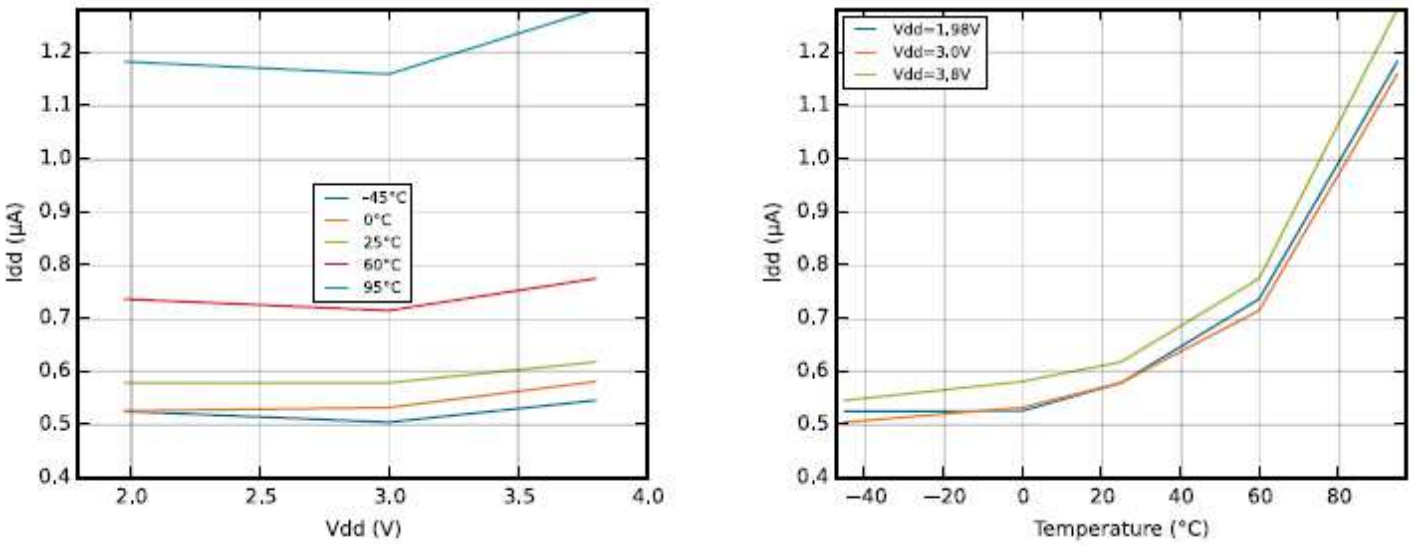


Figure 4.12. EM3 Current Consumption

4.5.5 EM4 Current Consumption

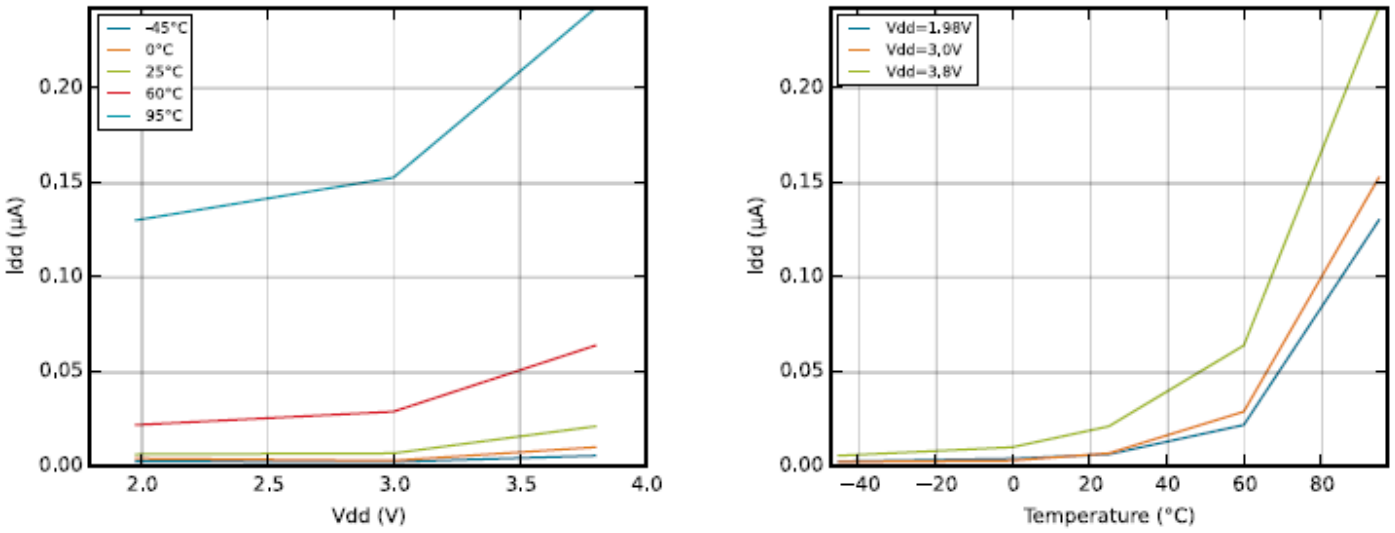


Figure 4.13. EM4 Current Consumption

4.6 Transitions between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.5. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	µs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	µs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	µs

4.7 Power Management

The EZR32HG requires the AVDD_x, VDD_DREG, RFVDD_x and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002: EFM32 Hardware Design Considerations*.

Table 4.6. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$	EM0	1.74	—	1.96	V
	$V_{BODextthr+}$	EM2	1.71	1.86	1.98	V
BOD threshold on rising external supply voltage	t_{RESET}		—	1.85	—	V
Delay from reset is released until program execution starts	$C_{DECOUPLE}$	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	µs
Voltage regulator decoupling capacitor.		X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	µF

4.8 Flash

Table 4.7. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 °C	10000	—	—	h
		T_{AMB}<85 °C	10	—	—	years
		T_{AMB}<70 °C	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time	t_{PERASE}		20	20.4	20.8	ms
Device erase time	t_{DERASE}		40	40.8	41.6	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

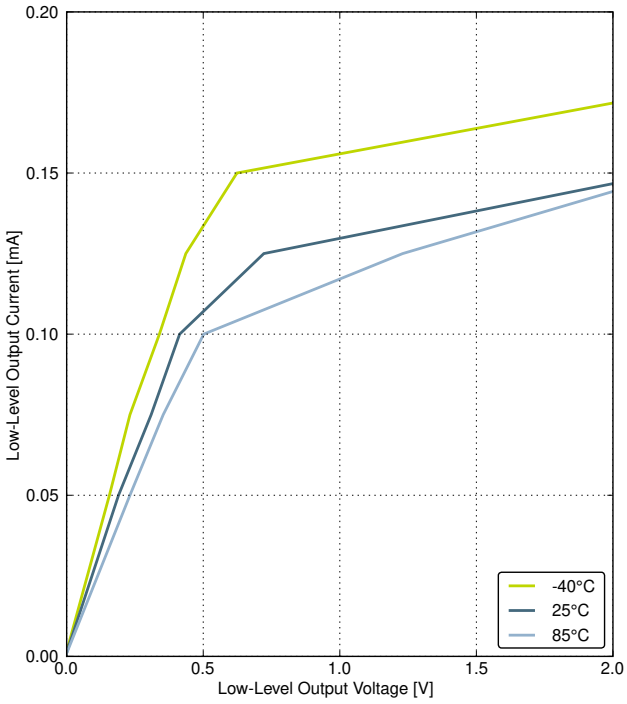
Note:
1. Measured at 25 ºC.

4.9 General Purpose Input Output

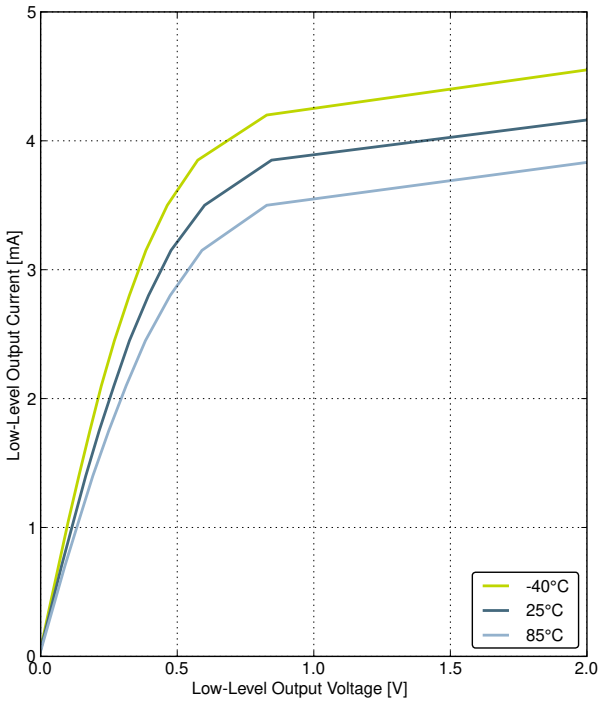
Table 4.8. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	0.30 V_{DD}	V
Input high voltage	V_{IOIH}		0.70 V_{DD}	—	—	V
Output high voltage (Production test condition = 3.0V, DRIVE-MODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.80 V_{DD}	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.90 V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.85 V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.90 V_{DD}	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75 V_{DD}	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80 V_{DD}	—	—	V

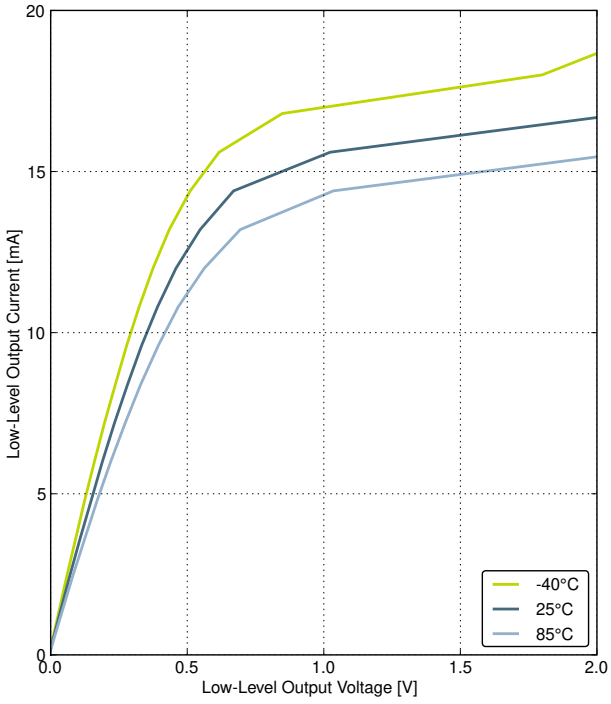
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output low voltage (Production test condition = 3.0 V, DRIVEMODE = STANDARD)	V_{IOOL}	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.20 V_{DD}	—	V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.05 V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.30 V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.20 V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.35 V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.25 V_{DD}	V
Input leakage current	I_{IOLEAK}	High Impedance IO connected to GROUND or Vdd	—	±0.1	±40	nA
I/O pin pull-up resistor	R_{PU}		—	40	—	kOhm
I/O pin pull-down resistor	R_{PD}		—	40	—	kOhm
Internal ESD series resistor	R_{IOESD}		—	200	—	Ohm
Pulse width of pulses to be removed by the glitch suppression filter	$t_{IOGLITCH}$		10	—	50	ns
Output fall time	t_{IOOF}	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25 pF.	20+0.1 C_L	—	250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600 pF	20+0.1 C_L	—	250	ns
I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{IOHYST}	V_{DD} = 1.98 - 3.8 V	0.1 V_{DD}	—	—	V



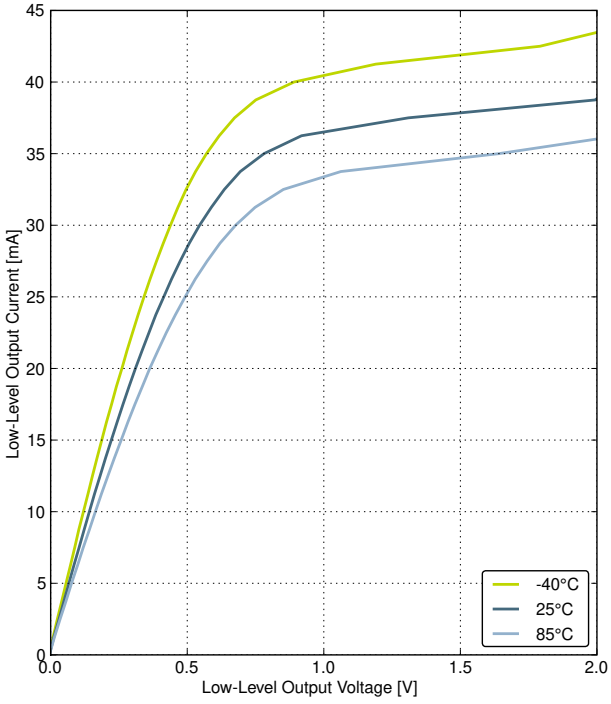
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = High

Figure 4.14. Typical Low-Level Output Current, 2 V Supply Voltage