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EZR32LG Wireless MCUs
EZR32LG230 Data Sheet

EZR32LG230 Wireless MCU family with ARM Cortex-M3 CPU and sub-GHz Radio

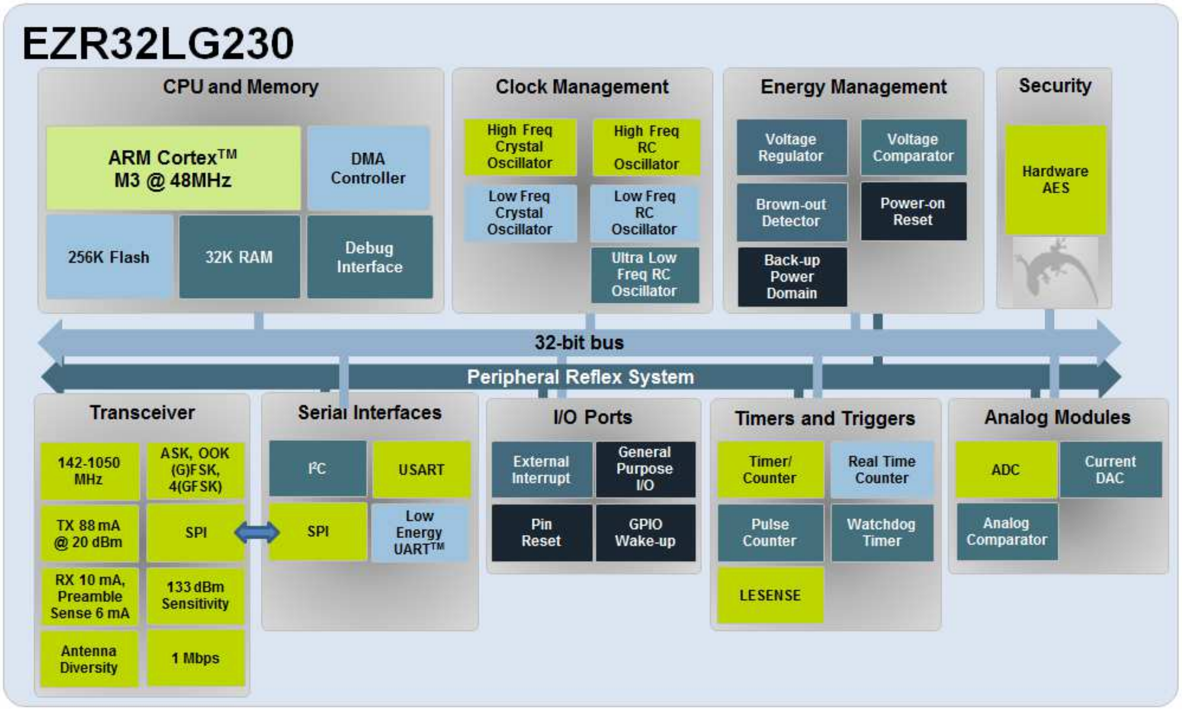
The EZR32LG Wireless MCUs are the latest in Silicon Labs family of wireless MCUs delivering a high performance, low energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit MCU, the EZR32LG family provides designers the ultimate in flexibility with a family of pin-compatible devices that scale with 64/128/256 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times of the Silicon Labs energy friendly 32-bit MCUs, combined with the low transmit and receive power consumption of the sub-GHz radio, result in a solution optimized for battery powered applications.

32-Bit ARM Cortex wireless MCUs applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Consumer electronics
- Alarm and security systems
- Building and home automation

KEY FEATURES

- Silicon Labs' first 32-bit Wireless MCUs
- Based on ARM Cortex M3 (LG) and M4 (WG) CPU cores with 256 kB of flash and 32 kB RAM
- Best-in-class RF performance with EZradio and EZRadioPro transceivers
- Ultra-low power wireless MCU
  - Low transmit and receive currents
  - Ultra-low power standby and sleep modes
  - Fast wake-up time
- Low Energy sensor interface (LESENSE)
- Rich set of peripherals including 12-bit ADC and DAC, multiple communication interfaces (UART, SPI, I2C), multiple GPIO and timers
- AES Accelerator with 128/256-bit keys



1. Feature List

The LG highlighted features are listed below.

MCU Features

- ARM Cortex-M3 CPU platform
  - Up to 48 MHz
  - 64/128/256 kB Flash w/32 kB RAM
  - Hardware AES with 128/256-bit keys
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.65 µA @ 3 V Stop Mode
  - 211 µA/MHz @ 3 V Run Mode
- Timers/Counters
  - 4× Timer/Counter
  - 4×3 Compare/Capture/PWM channels
  - Low Energy Timer
  - Real-Time Counter
  - 16/8-bit Pulse Counter
  - Watchdog Timer
- Communication interfaces
  - 2× USART (UART/SPI)
  - 2× UART
  - 2× Low Energy UART
  - 2× I2C Interface with SMBus support
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s ADC
  - On-chip temperature sensor
  - 12-bit 500 ksamples/s DAC
  - 2× Analog Comparator
  - 2x Operational Amplifier
- Low Energy Sensor Interface (LESENSE)
- Up to 41 General Purpose I/O pins

RF Features

- Frequency Range
  - 142-1050 MHz
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK, OOK
- Receive sensitivity up to -133 dBm
- Up to +20 dBm max output power
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm
  - 6 mA @ 1.2 kbps (Preamble Sense)
- Data rate = 100 bps to 1 Mbps
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- IEEE 802.15.4g compliant

System Features

- Power-on Reset and Brown-Out Detector
- Debug Interface
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- QFN64 package

2. Ordering Information

The table below shows the available EZR32LG230 devices.

Table 2.1. Ordering Information

Ordering	Radio	Flash (kB)	RAM (kB)	Power Amplifier (dBm)	Max Sensitivity (dBm)	Supply Voltage (V)	Package
EZR32LG230FxxxR55G	EZRadio	64-256	32	+13	-116	1.98 - 3.8	QFN64
EZR32LG230FxxxR60G	EZRadioPro	64-256	32	+13	-129	1.98 - 3.8	QFN64
EZR32LG230FxxxR61G	EZRadioPro	64-256	32	+16	-129	1.98 - 3.8	QFN64
EZR32LG230FxxxR63G	EZRadioPro	64-256	32	+20	-129	1.98 - 3.8	QFN64
EZR32LG230FxxxR67G	EZRadioPro	64-256	32	+13	-133	1.98 - 3.8	QFN64
EZR32LG230FxxxR68G	EZRadioPro	64-256	32	+20	-133	1.98 - 3.8	QFN64
EZR32LG230FxxxR69G	EZRadioPro	64-256	32	+13 & 20	-133	1.98 - 3.8	QFN64

Table 2.2. Flash Sizes

Example Part Number	Flash Size
EZR32LG230F64R55G	64 kB
EZR32LG230F128R55G	128 kB
EZR32LG230F256R55G	256 kB

Note: Add an "(R)" at the end of the device part number to denote tape and reel option.

Visit www.silabs.com for information on global distributors and representatives.

3. System Overview

3.1 Introduction

The EZR32LG230 Wireless MCUs are the latest in Silicon Labs family of wireless MCUs delivering a high performance, low energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit ARM Cortex-M3, the EZR32LG family provides designers with the ultimate in flexibility with a family of pin-compatible parts that scale from 64 to 256 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times combined with the low transmit and receive power consumption of the sub-GHz radio result in a solution optimized for low power and battery powered applications. For a complete feature set and in-depth information on the modules, the reader is referred to the *EZR32LG Reference Manual*.

The EZR32LG230 block diagram is shown below.

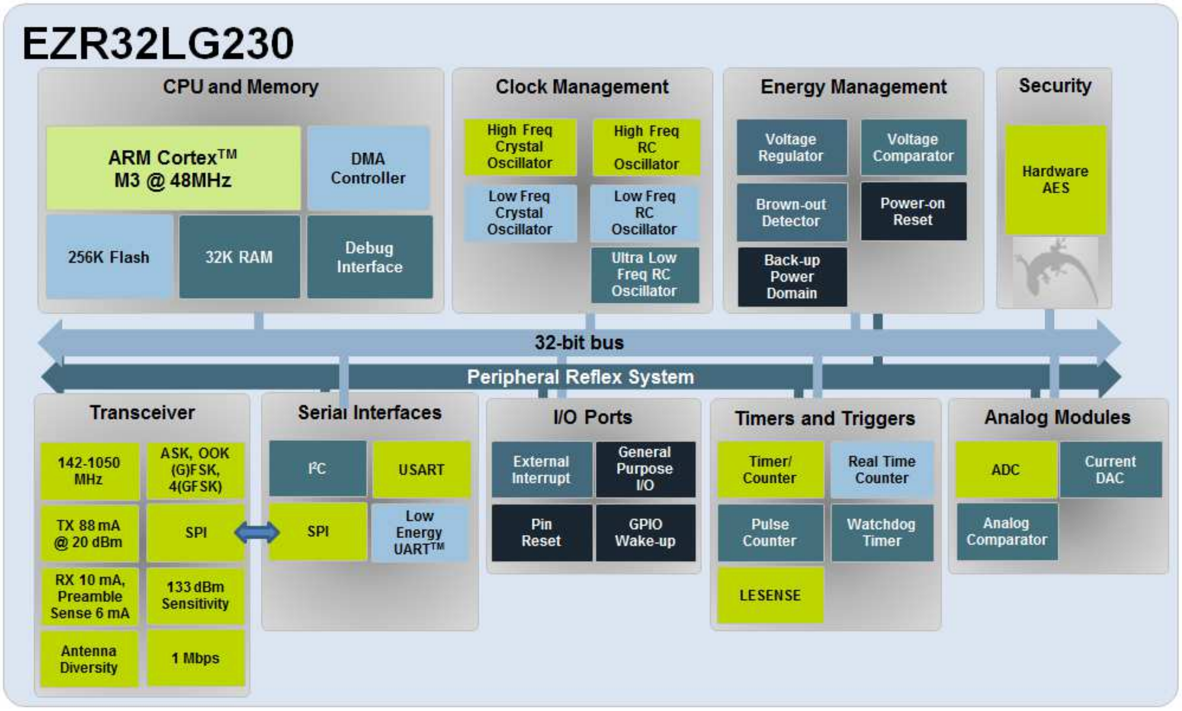


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EZR32 implementation of the Cortex-M3 is described in detail in *EZR32 Cortex-M3 Reference Manual*.

3.1.2 Debugging

These devices include hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EZR32LG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks: the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving, for instance, data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μDMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EZR32LG.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manages all the low energy modes (EM) in EZR32LG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EZR32LG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may, for example, be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, and I2S devices.

3.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note *AN0003* is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface, and commands are described further in the application note.

3.1.13 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

3.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.17 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

3.1.18 Low Energy Timer (LETIMER)

The unique LETIMER™, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

3.1.19 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.20 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.21 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.22 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

3.1.23 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

3.1.24 Operational Amplifier (OPAMP)

The EZR32LG230 features 2 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors, etc.

3.1.25 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.1.26 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EZR32LG230 to keep track of time and retain data, even if the main power source should drain out.

3.1.27 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations (i.e., 8- or 16-bit operations are not supported).

3.1.28 General Purpose Input/Output (GPIO)

In the EZR32LG230, there are 41 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.29 EZRadio® and EZRadioPro® Transceivers

The EZR32LG family of devices is built using high-performance, low-current EZRadio and EZRadioPro RF transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. These devices offer outstanding sensitivity of upto –133 dBm (using EZRadioPro) while achieving extremely low active and standby current consumption. The EZR32LG devices using the EZRadioPro transceiver offer frequency coverage in all major bands and include optimal phase noise, blocking, and selectivity performance for narrow band and licensed band applications, such as FCC Part 90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times is optimized for extended battery life in the most demanding applications. The EZR32LG devices can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be programmed and configured via Simplicity Studio, available at www.silabs.com.

Communications between the radio and MCU are done over USART, PRS and IRQ, which requires the pins to be configured in the following way:

Table 3.1. Radio MCU Communication Configuration

EZR32LG Pin	Radio Assignment	EZR32LG Function Assignment
PE8	SDN	GPIO Output
PE9	$_n$SEL	Bit-Banged SPI.CS (GPIO Output)
PE10	SDI	US0_TX #0
PE11	SDO	US0_RX #0
PE12	SCLK	US0_CLK #0
PE13	$_n$IRQ	GPIO_EM4WU5 (GPIO Input with IRQ enabled)
PE14	GPIO1	PRS Input
PA15	GPIO0	PRS Input

3.1.29.1 EZRadio® and EZRadioPRO® Transceivers GPIO Configuration

The EZRadio and EZRadioPRO Transceivers have 4 General Purpose Digital I/O pins. These GPIOs may be configured to perform various radio-specific functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.

Two of the radio GPIO pins are directly connected to pins on the package (GPIO2 and GPIO3). However, the remaining two radio GPIO pins (GPIO0 and GPIO1) connect internally on the EZR32LG to the pins shown in 3.1.29 EZRadio® and EZRadioPro® Transceivers. These radio GPIOs may be routed to external package pins using the EZR32LG's peripheral reflex system (PRS). Note that the maximum frequency of the GPIO pins routed through PRS pins may be limited to ~10 MHz.

Below is some example code illustrating how to configure the EZR32LG PRS system to output the radio GPIO0/GPIO1 functions to EZR32LG pins PA0 / PA1, respectively. Note that the radio GPIO0/GPIO1 functions could also be connected to EZR32LG pins PF3/PF4.

```
/* PRS routing radio GPIO0 and GPIO1 to external pin PA0&PA1 */
/ * Note that this code example uses the emlib library functions for CMU, GPIO, and PRS */
/* Enable PRS clock */
CMU_ClockEnable(cmuClock_PRS, true);

/* Setup input pins */
GPIO_PinModeSet(gpioPortA, 15, gpioModeInput, 0);
GPIO_PinModeSet(gpioPortE, 14, gpioModeInput, 0);

/* Setup output pins */
GPIO_PinModeSet(gpioPortA, 0, gpioModePushPull, 0);
GPIO_PinModeSet(gpioPortA, 1, gpioModePushPull, 0);

/* Configure INT/PRS channels */
GPIO_IntConfig(gpioPortA, 15, false, false, false);
GPIO_IntConfig(gpioPortE, 14, false, false, false);

/* Setup PRS */
PRS_SourceAsyncSignalSet(0, PRS_CH_CTRL_SOURCESEL_GPIOH, PRS_CH_CTRL_SIGSEL_GPIOPIN15);
PRS_SourceAsyncSignalSet(1, PRS_CH_CTRL_SOURCESEL_GPIOH, PRS_CH_CTRL_SIGSEL_GPIOPIN14);
PRS->ROUTE = (PRS_ROUTE_CH0PEN | PRS_ROUTE_CH1PEN);

/* Make sure PRS sensing is enabled (should be by default) */
GPIO_InputSenseSet(GPIO_INSENSE_PRS, GPIO_INSENSE_PRS);
```

3.2 Configuration Summary

The features of the EZR32LG230 are a subset of the feature set described in the *EZR32LGReference Manual*. The table below describes device specific implementation of the features.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USARTRF0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0]

Module	Configuration	Pin Connections
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUT-xALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	41 pins	Available pins are shown in 5.4 GPIO Pin-out Overview

3.3 Memory Map

The EZR32LG230 memory map is shown below with RAM and flash sizes for the largest memory configuration.

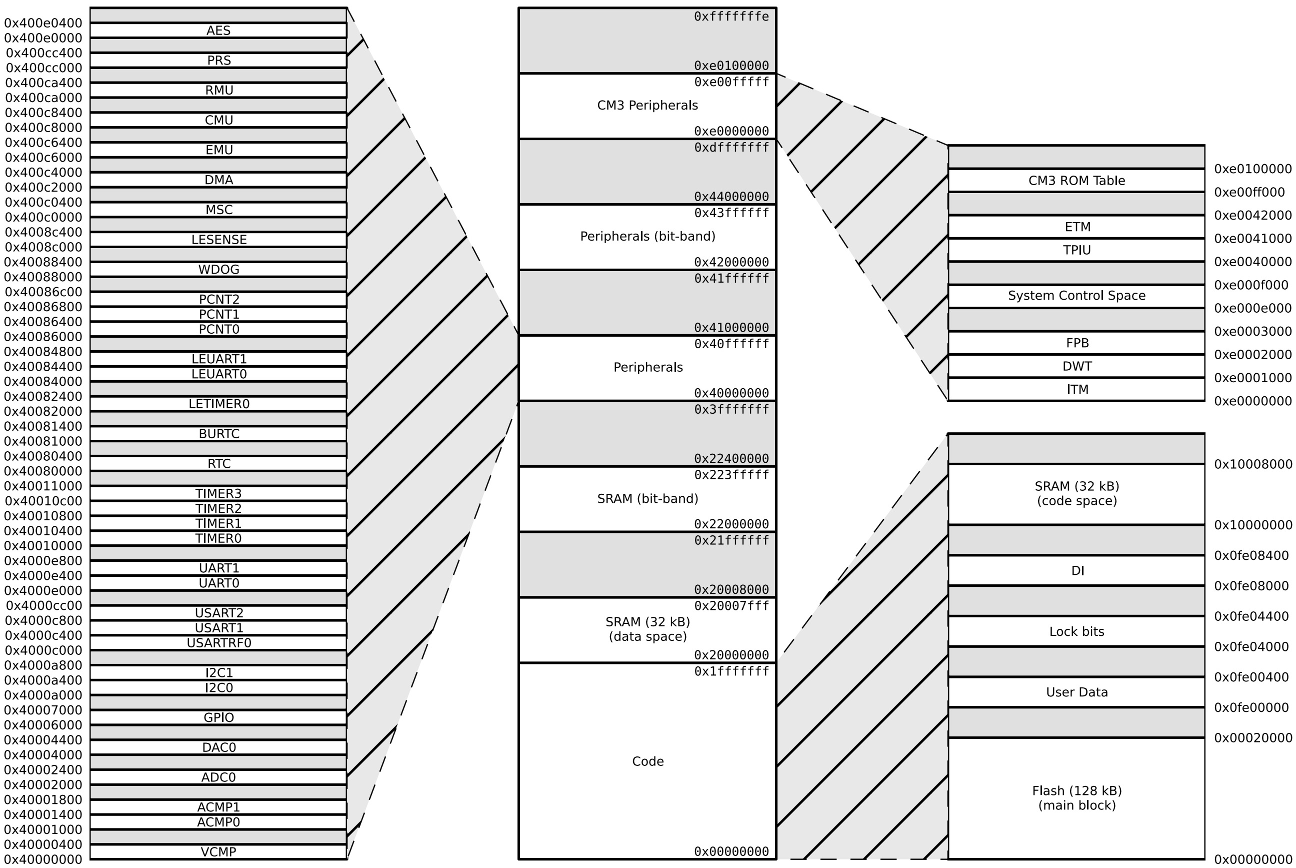


Figure 3.2. EZR32LG230 Memory Map with Largest RAM and Flash Sizes

4. Electrical Specifications

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB} = 25°C and V_{DD} = 3.0 V, as defined in Table 4.3 General Operating Conditions on page 12, by simulation and/or technology characterisation unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 4.3 General Operating Conditions on page 12, by simulation and/or technology characterisation unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the table below may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 4.3 General Operating Conditions on page 12.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-55	—	150[1]	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V

Note:

1. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.3 Thermal Characteristics

Table 4.2. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}		-40	—	85	°C
Junction temperature value	T_J		—	—	105[1]	°C
Thermal impedance junction to ambient	TI_{JA}	+13/+16 dBm on 2-layer board	—	—	61.8	°C/W
		+20 dBm on 4-layer board	—	—	20.7[2]	°C/W
Storage temperature range	T_{STG}		-55	—	150	°C

Note:

1. Values are based on simulations run on 2 layer and 4 layer PCBs at 0m/s airflow.
2. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.4 General Operating Conditions

Table 4.3. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}	-40	—	85	°C
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V
Internal APB clock frequency	f_{APB}	—	—	48	MHz
Internal AHB clock frequency	f_{AHB}	—	—	48	MHz

Table 4.4. Environmental

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ESD (Human Body Model HBM)	V_{ESDHBM}	T_{AMB}=25 °C	—	—	2000	V
ESD (Charged Device Model, CDM)	V_{ESDCDM}	T_{AMB}=25 °C	—	—	500	V

Latch-up sensitivity passed: ±100 mA/1.5 × V_{SUPPLY}(max) according to JEDEC JESD 78 method Class II, 85 °C.

4.5 Current Consumption

Table 4.5. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	211	225	µA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	211	230	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	212	220	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	213	223	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	214	224	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	215	226	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	216	231	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	217	237	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	218	239	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	219	239	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	224	242	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	224	250	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	257	285	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	261	293	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM1 current (Production test condition = 14 MHz)	I_{EM1}	48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	63	75	µA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	65	76	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	64	75	µA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	65	77	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	65	76	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	66	78	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	67	79	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	68	82	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	68	81	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	70	83	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	74	87	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	76	89	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	106	120	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	112	129	µA/MHz
EM2 current	I_{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=25 °C	—	0.95[1]	1.7	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD}= 3.0 V, T_{AMB}=85 °C	—	3.0[1]	4.0[1]	µA
EM3 current	I_{EM3}	V_{DD}= 3.0 V, T_{AMB}=25 °C	—	0.65	1.3	µA
		V_{DD}= 3.0 V, T_{AMB}=85 °C	—	2.65	4.0	µA
EM4 current	I_{EM4}	V_{DD}= 3.0 V, T_{AMB}=25 °C	—	0.02	0.055	µA
		V_{DD}= 3.0 V, T_{AMB}=85 °C	—	0.44	0.9	µA

Note:

1. Using backup RTC.

4.6 Transitions between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.6. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	µs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	µs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	µs

4.7 Power Management

The EZR32LG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002: EFM32 Hardware Design Considerations*.

Table 4.7. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$		1.74	—	1.96	V
BOD threshold on falling internally regulated supply voltage	$V_{BODintthr-}$		1.57	—	1.7	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$		—	1.85	1.98	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	t_{RESET}	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	µs
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	µF

4.8 Flash

Table 4.8. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 °C	10000	—	—	h
		T_{AMB}<85 °C	10	—	—	years
		T_{AMB}<70 °C	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time	t_{PERASE}		20	20.4	20.8	ms
Device erase time	t_{DERASE}		40	40.8	41.6	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

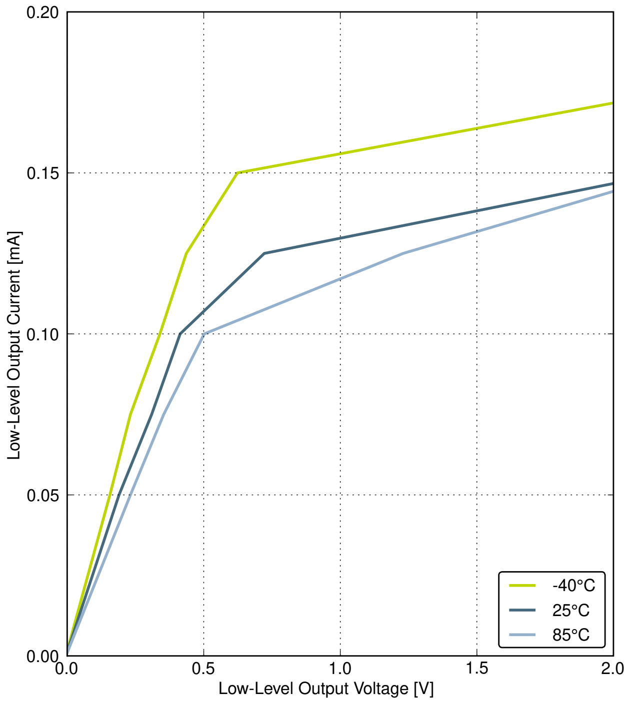
1. Measured at 25 ºC.

4.9 General Purpose Input Output

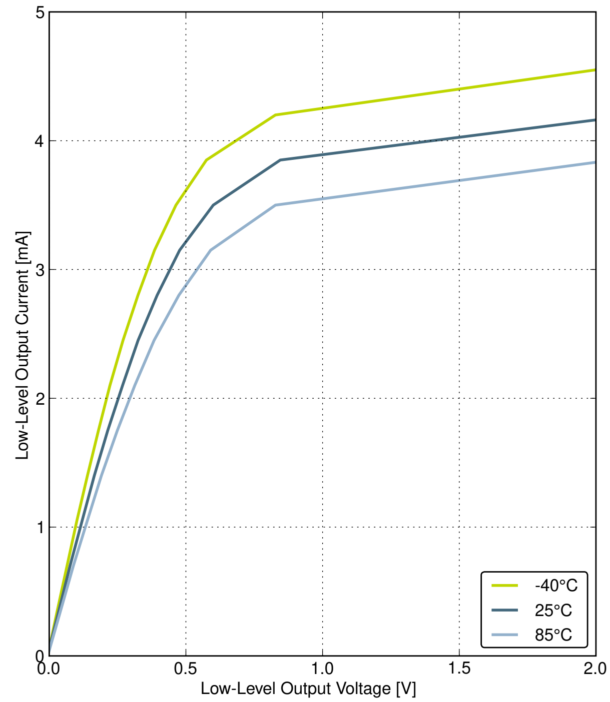
Table 4.9. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	0.30 V_{DD}	V
Input high voltage	V_{IOIH}		0.70 V_{DD}	—	—	V
Output high voltage (Production test condition = 3.0V, DRIVE-MODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.80 V_{DD}	—	V
		Sourcing 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.90 V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.85 V_{DD}	—	V
		Sourcing 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.90 V_{DD}	—	V
		Sourcing 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75 V_{DD}	—	—	V
		Sourcing 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80 V_{DD}	—	—	V

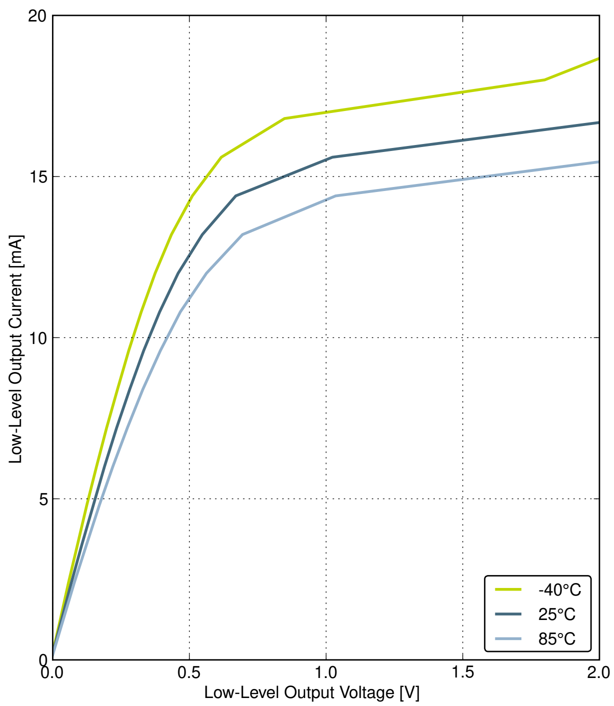
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output low voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD)	V_{IOOL}	Sinking 0.1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.20 V_{DD}	—	V
		Sinking 0.1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.05 V_{DD}		V
		Sinking 6 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.30 V_{DD}	V
		Sinking 6 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.20 V_{DD}	V
		Sinking 20 mA, V_{DD}=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.35 V_{DD}	V
		Sinking 20 mA, V_{DD}=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.25 V_{DD}	V
Input leakage current	I_{IOLEAK}	High Impedance IO connected to GROUND or Vdd	—	±0.1	±100	nA
I/O pin pull-up resistor	R_{PU}		—	40	—	kOhm
I/O pin pull-down resistor	R_{PD}		—	40	—	kOhm
Internal ESD series resistor	R_{IOESD}		—	200	—	Ohm
Pulse width of pulses to be removed by the glitch suppression filter	$t_{IOGLITCH}$		10	—	—	ns
Output fall time	t_{IOOF}	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L=12.5-25 pF.	20+0.1 C_L	—	250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L=350-600 pF	20+0.1 C_L	—	250	ns
I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{IOHYST}	V_{DD} = 1.98 - 3.8 V	0.10 V_{DD}	—	—	V



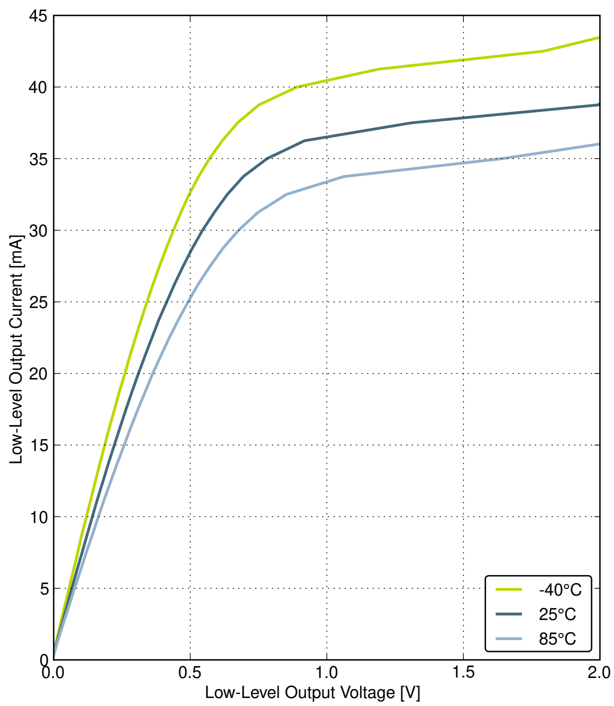
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

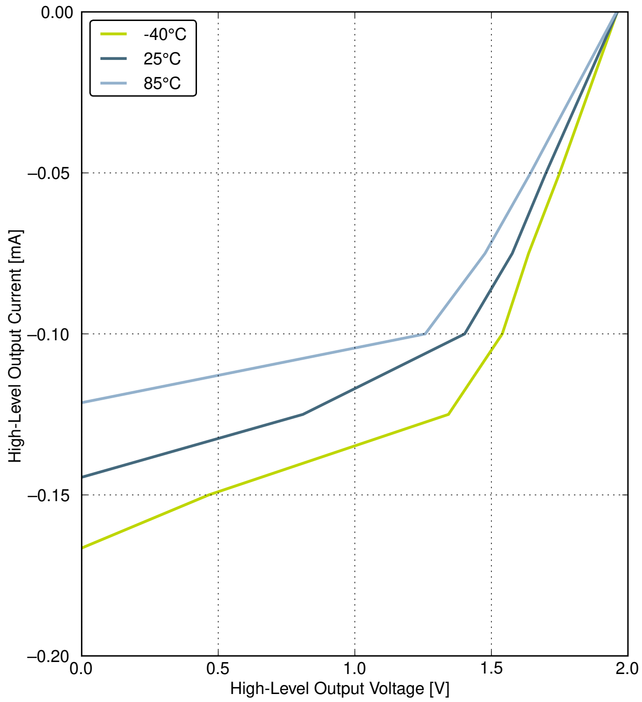


GPIO_Px_CTRL DRIVEMODE = STANDARD

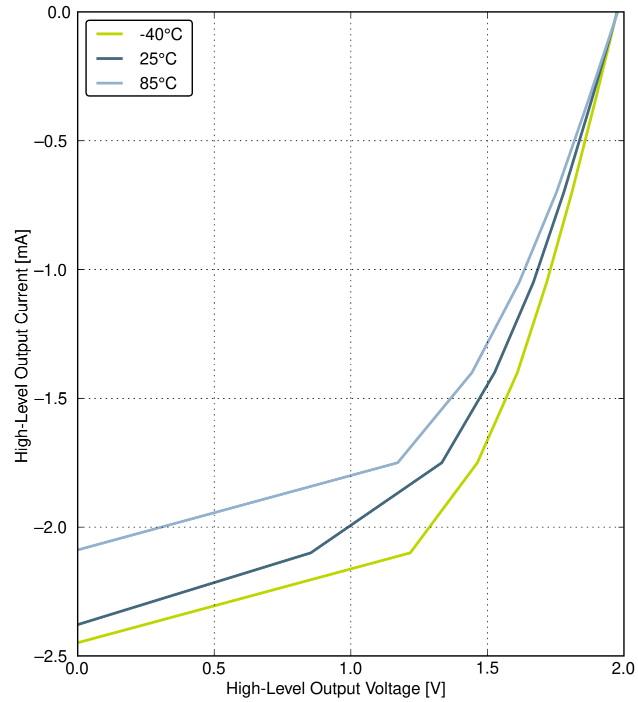


GPIO_Px_CTRL DRIVEMODE = High

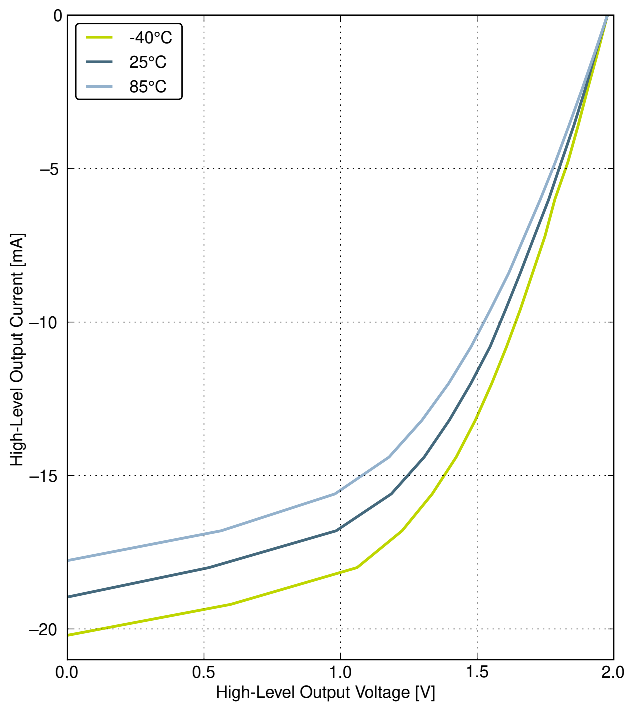
Figure 4.1. Typical Low-Level Output Current, 2 V Supply Voltage



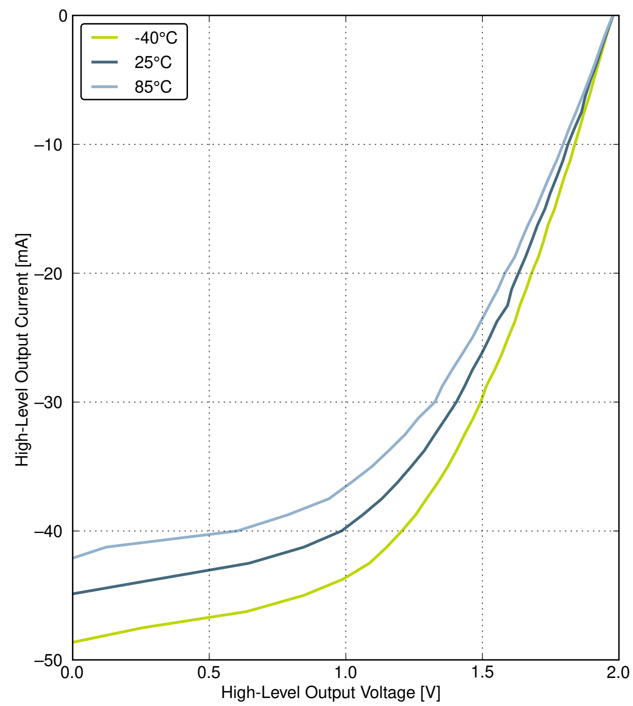
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

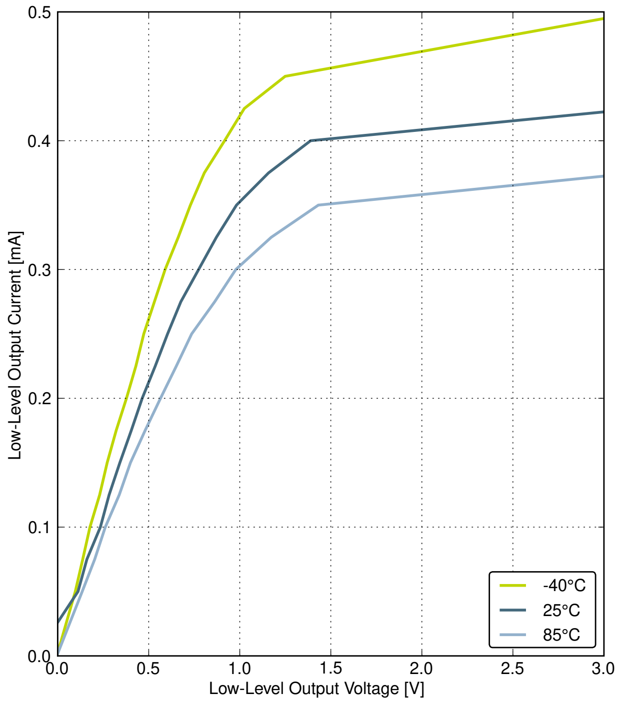


GPIO_Px_CTRL DRIVEMODE = STANDARD

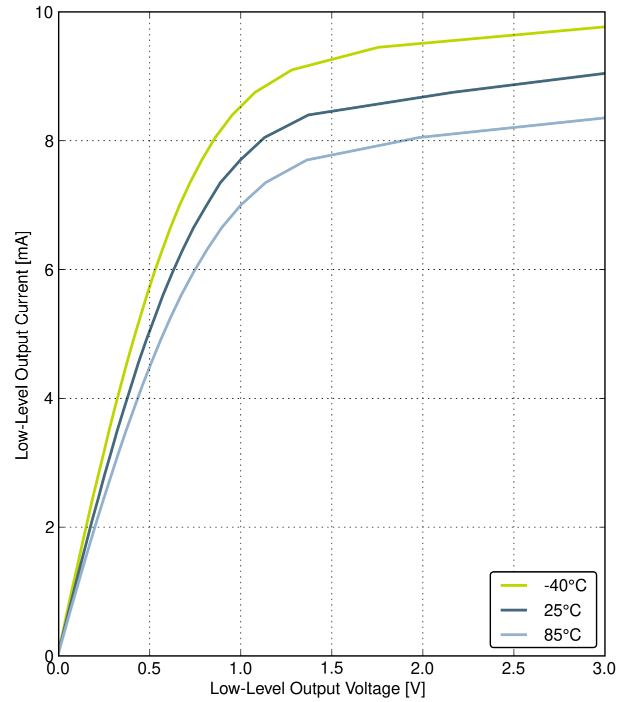


GPIO_Px_CTRL DRIVEMODE = High

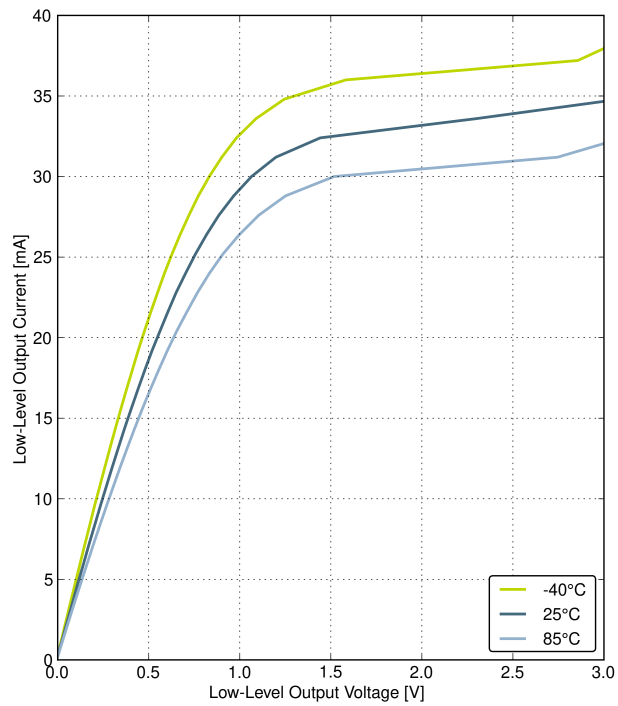
Figure 4.2. Typical High-Level Output Current, 2 V Supply Voltage



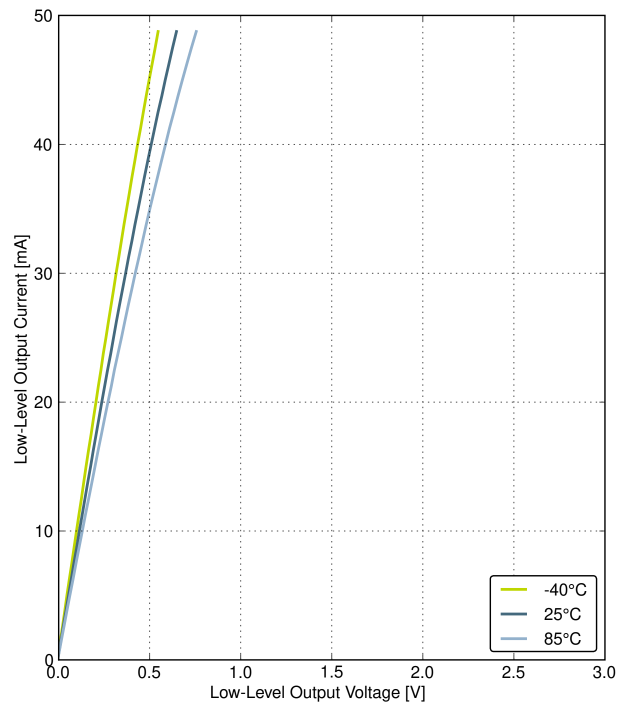
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

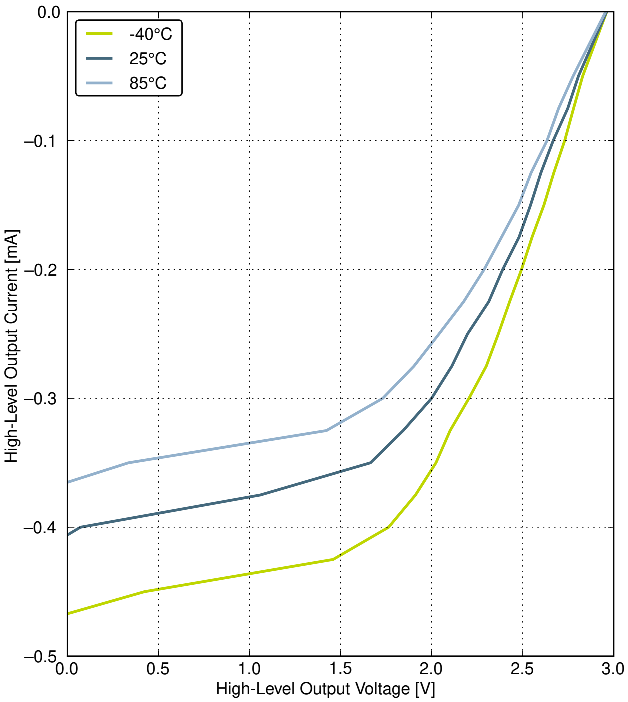


GPIO_Px_CTRL DRIVEMODE = STANDARD

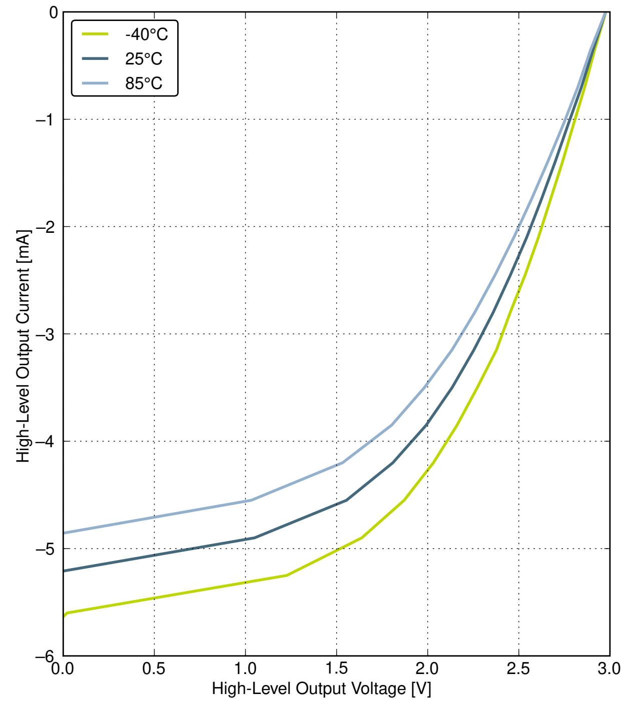


GPIO_Px_CTRL DRIVEMODE = High

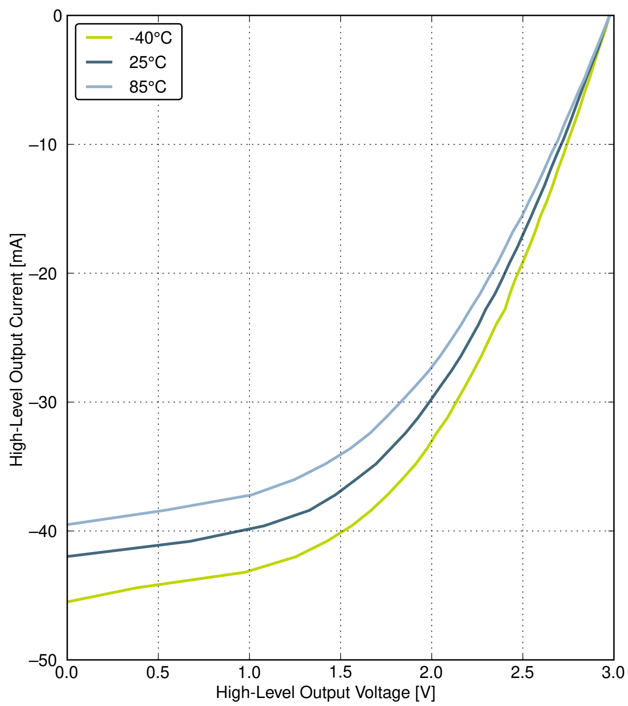
Figure 4.3. Typical Low-Level Output Current, 3 V Supply Voltage



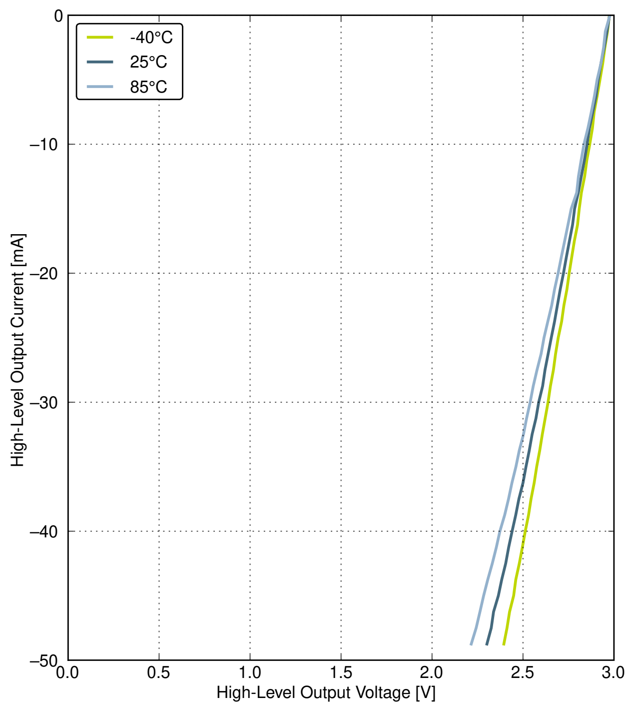
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

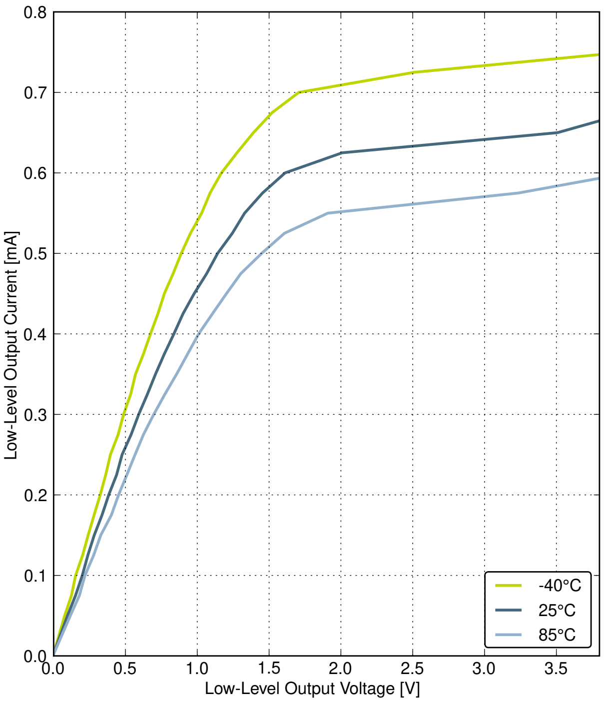


GPIO_Px_CTRL DRIVEMODE = STANDARD

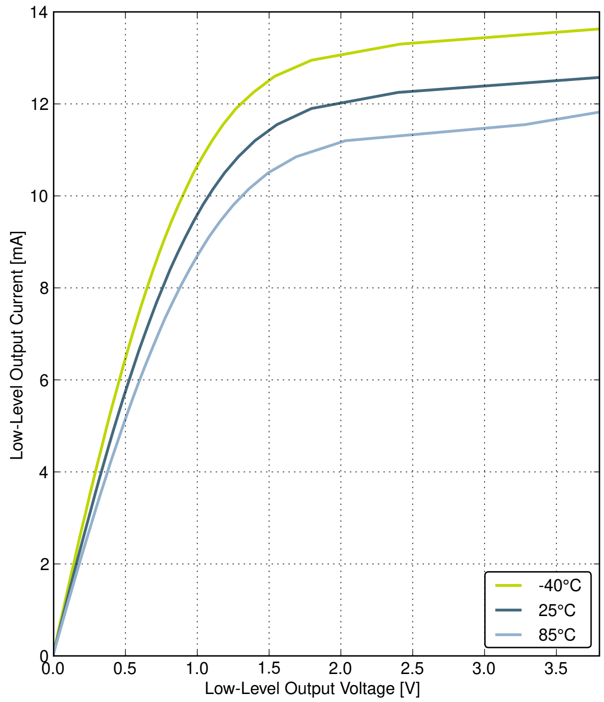


GPIO_Px_CTRL DRIVEMODE = High

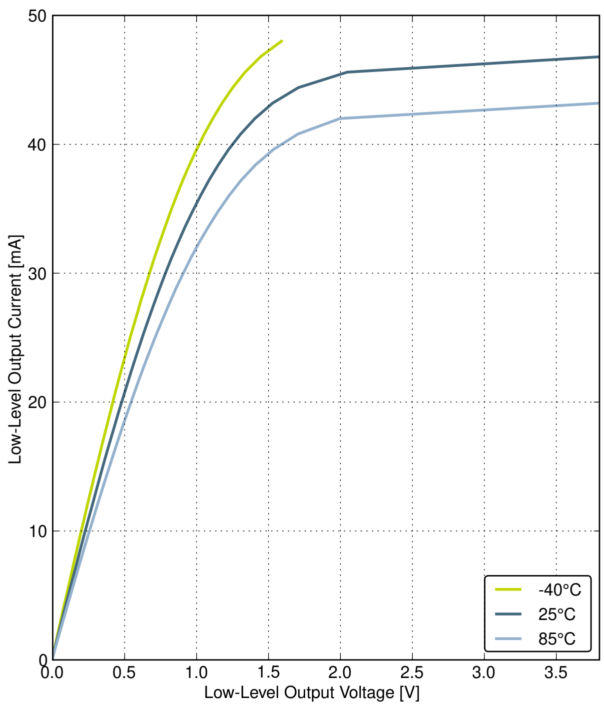
Figure 4.4. Typical High-Level Output Current, 3 V Supply Voltage



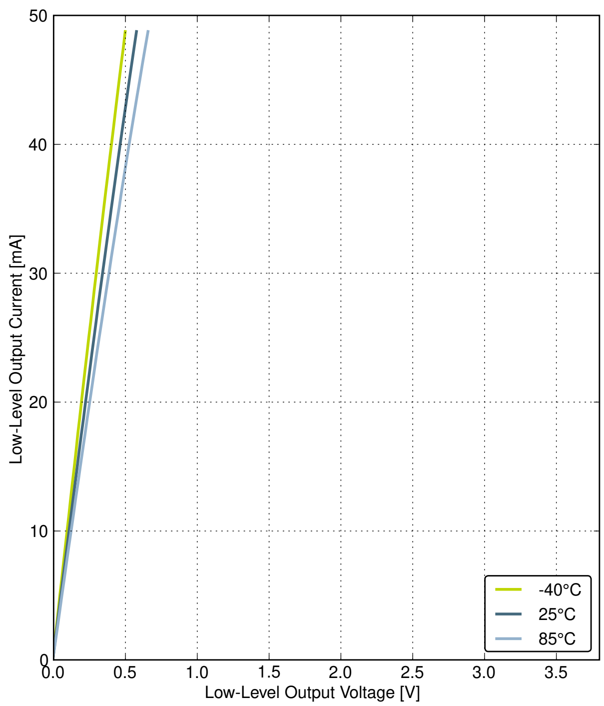
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

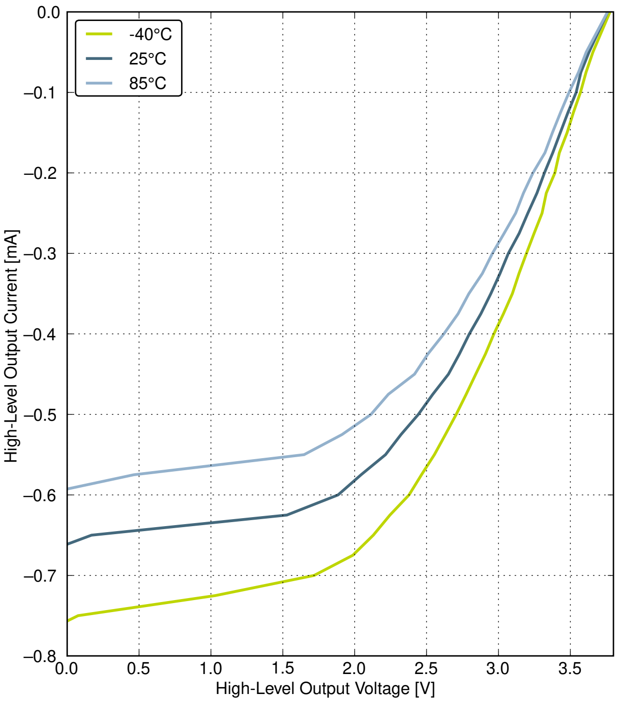


GPIO_Px_CTRL DRIVEMODE = STANDARD

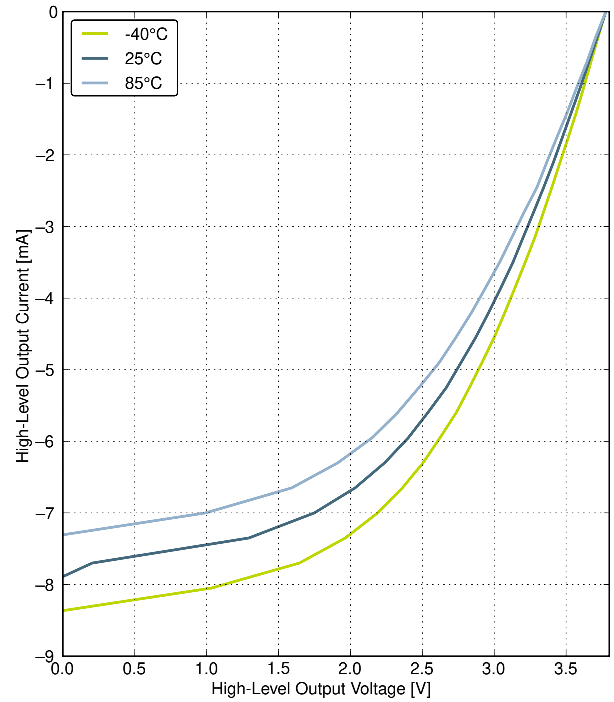


GPIO_Px_CTRL DRIVEMODE = High

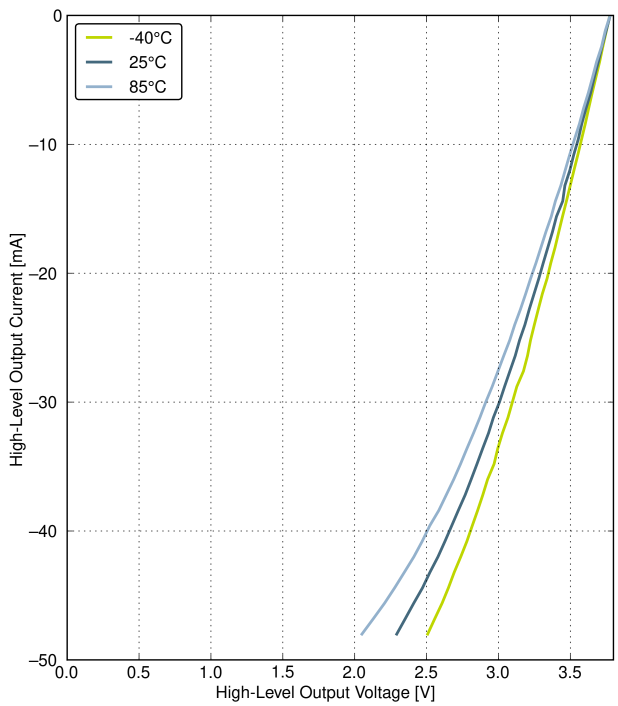
Figure 4.5. Typical Low-Level Output Current, 3.8 V Supply Voltage



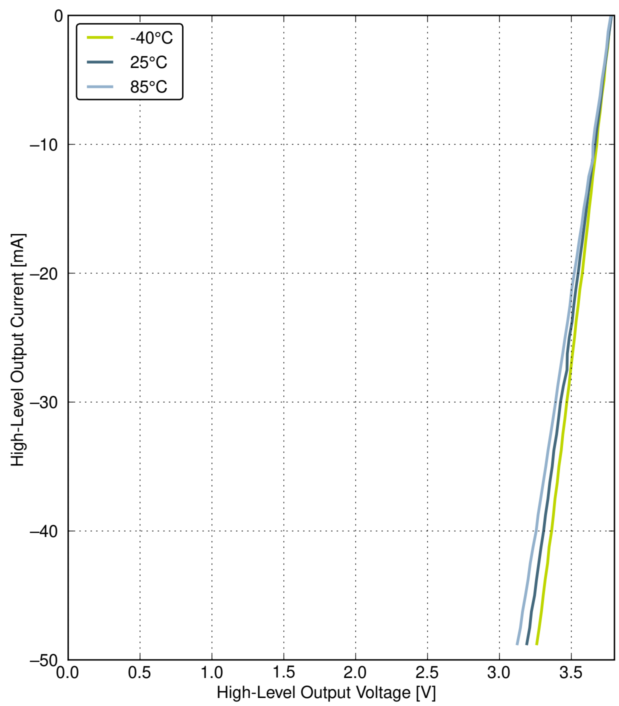
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = High

Figure 4.6. Typical High-Level Output Current, 3.8 V Supply Voltage