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Freescale Semiconductor
Data Sheet: Advance Information

F104S8A Data Sheet

Quad-Port 10/100/1000BASE-T PHY with QSGMII MAC

Supports
F104S8A
F104X8A

F104S8A
Rev. 1
02/2015

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Document Number: F104S8A
Rev. 1, 02/2015

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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 1

Revision 1 of this datasheet was published in February 2015. The following change is implemented in the datasheet:

- Updated the description of Table 79 to explain that the specifications are valid "only when V_{VDD1} = 1.0 V, V_{VDD1A} = 1.0 V, and V_{VDD25A} = 2.5 V."

Revision 0

Revision 0 of this datasheet was published in January 2015. This was the first public release of this document.

1 Product Overview

The F104S8A device is a low-power Gigabit Ethernet transceiver with copper media interfaces. It has a low electromagnetic interference (EMI) line driver, and integrated line-side termination resistors that conserve both power and printed circuit board (PCB) space.

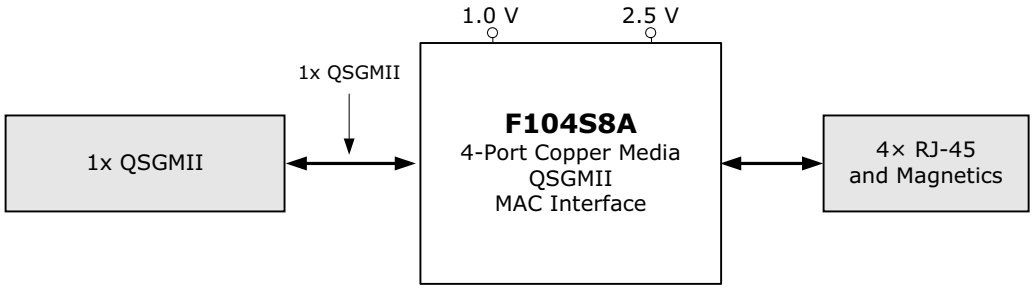
The F104S8A device includes Vitesse's EcoEthernet™ 2.0 technology that supports Energy Efficient Ethernet and power saving features to reduce power based on link state and cable reach.

The F104S8A device uses Vitesse's mixed signal and digital signal processing (DSP) architecture to ensure robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 100 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environmental and system electronic noise.

The F104S8A device also includes fast link failure indication for high-availability networks. Fast link failure indication identifies the onset of a link failure in less than 1 ms typical to go beyond the IEEE 802.3 standard requirement of 750 ms ±10 ms (link master).

The following illustration shows a high-level, general view of a typical F104S8A application.

Figure 1. Copper Transceiver Application Diagram



1.1 Key Features

This section lists the main features and benefits of the device.

1.1.1 Superior PHY and Interface Technology

- Four integrated 10/100/1000BASE-T Ethernet copper transceivers (IEEE 802.3ab-compliant) with VeriPHY™ cable diagnostics
- QSGMII SerDes MAC interface

- Patented line driver with low EMI voltage mode and integrated line side termination resistors
- HP Auto-MDIX support and forced MDI/MDIX option
- Jumbo frame support up to 16 kB with programmable synchronization FIFOs
- IEEE 802.3bf register support for standardized access to information on data delay between the MDI and xMII interface for a given PHY

1.1.2 Best-in-Class Power Consumption

- EcoEthernet™ 2.0 green energy efficiency with ActiPHY™, PerfectReach™, and IEEE 802.3az Energy Efficient Ethernet
- Fully optimized power consumption for all link speeds
- Integrated LED brightness control
- Clause 45 registers to support IEEE 802.3az Energy Efficient Ethernet and IEEE 802.3bf

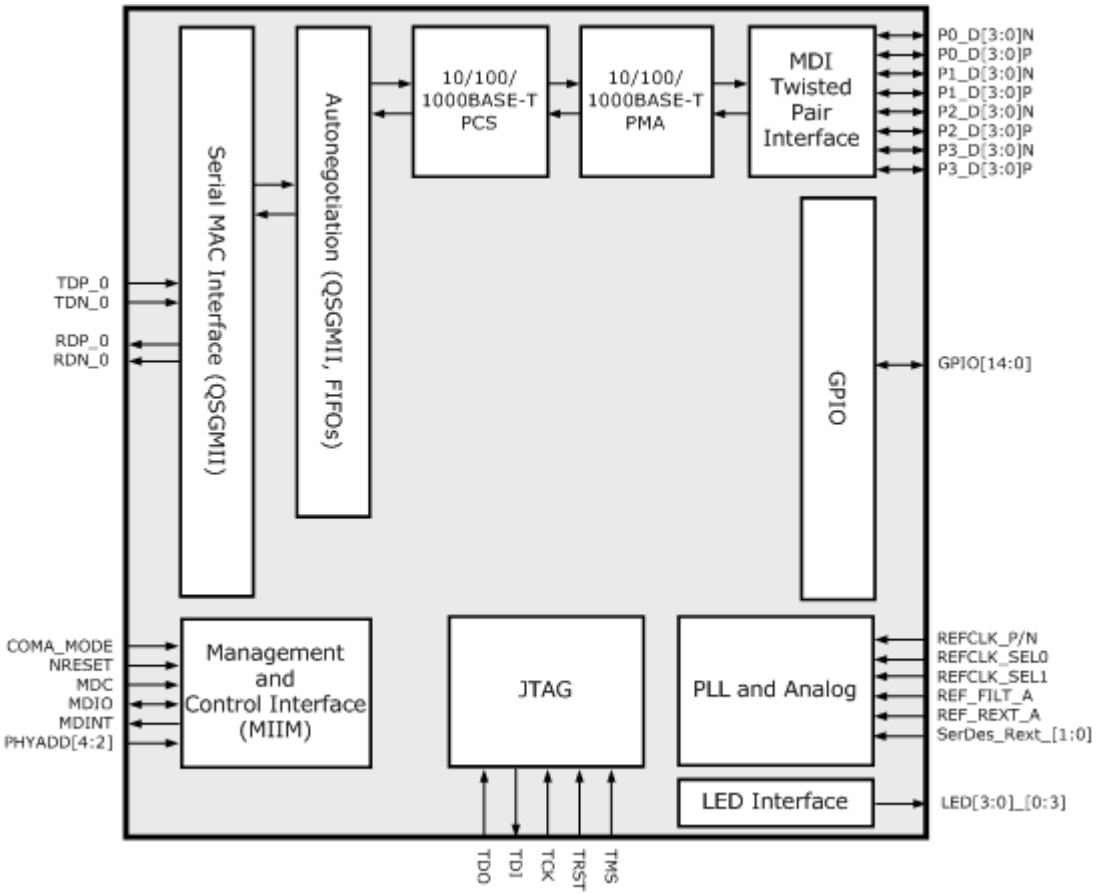
1.1.3 Key Specifications

- 1.0 V and 2.5 V power supplies
- 3.3 V-tolerant 2.5 V inputs (single-ended and bi-directional TTL/CMOS I/Os)
- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, and 1000BASE-T)
- QSGMII v1.3 and IEEE 1149.1 JTAG boundary scan
- Devices support operating temperatures of –40 °C ambient to 125 °C junction or 0 °C ambient to 125 °C junction
- Available in 12 mm x 12 mm, 138-pin, multi-row plastic QFN package

1.2 Block Diagram

The following illustration shows the primary functional blocks of the F104S8A device.

Figure 2. Block Diagram



2 Functional Descriptions

This section provides detailed information about the functionality of the F104S8A device, including available configurations, operational features, and testing functionality. It includes descriptions of the various device interfaces and their configuration. With the information in this section, the device setup parameters can be determined for configuring the device for use in a particular application.

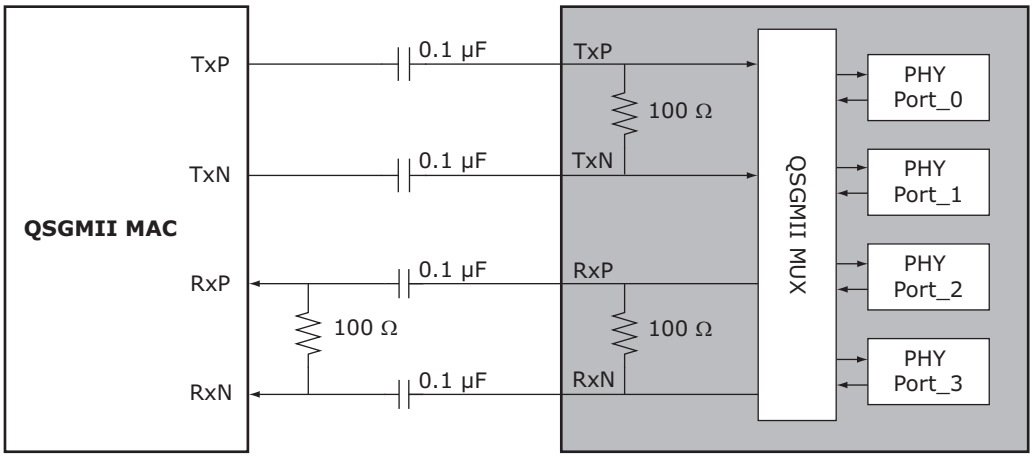
2.1 SerDes MAC Interface

The SerDes MAC interface performs data serialization and deserialization functions using an integrated enhanced SerDes operating in QSGMII mode. The termination resistor is integrated into the enhanced SerDes block in the device but does not include integrated AC decoupling capacitors.

2.1.1 QSGMII MAC

The device supports a QSGMII MAC to convey two ports of network data and port speed between 10BASE-T, 100BASE-TX, and 1000BASE-T data rates and operates in both half-duplex and full-duplex at all port speeds. The MAC interface protocol for each port within QSGMII can be either 1000BASE-X or SGMII, if the QSGMII MAC that the F104S8A device is connecting to supports this functionality. The device also supports SGMII MAC-side autonegotiation on each individual port, enabled through register 16E3, bit 7, of that port.

Figure 3. QSGMII MAC Interface



2.2 PHY Addressing and Port Mapping

The device includes three external PHY address pins, PHYADD[4:2], to allow control of multiple PHY devices on a system board sharing a common management bus. These

pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 1) and the setting of the PHY address reversal bit in register 20E1, bit 9.

The device also includes one 5 GHz enhanced SerDes macro operating in QSGMII mode.

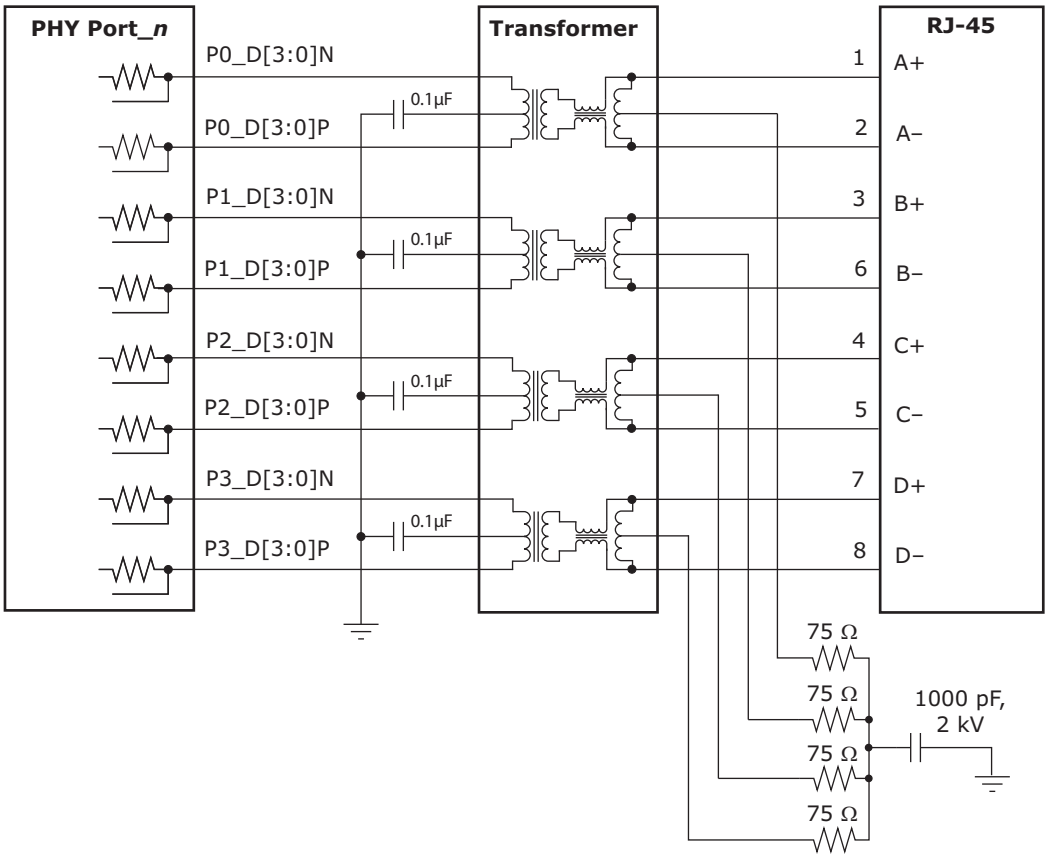
2.3 Cat5 Twisted Pair Media Interface

The F104S8A twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az standard for Energy Efficient Ethernet.

2.3.1 Voltage Mode Line Driver

The F104S8A device uses a patented voltage mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's Cat5 interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 4. Cat5 Media Interface



2.3.2 Cat5 Autonegotiation and Parallel Detection

The F104S8A device supports twisted pair autonegotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Autonegotiation also enables a connected MAC to communicate with its link partner MAC through the F104S8A device using optional next pages to set attributes that may not otherwise be defined by the IEEE standard.

If the Category 5 (Cat5) link partner does not support autonegotiation, the F104S8A device automatically uses parallel detection to select the appropriate link speed.

Autonegotiation is disabled by clearing register 0, bit 12. When autonegotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode.

Note While 10BASE-T and 100BASE-TX do not require autonegotiation, IEEE 802.3-2008 Clause 40 has defined 1000BASE-T to require autonegotiation.

2.3.3 1000BASE-T Forced Mode Support

The F104S8A device provides support for a 1000BASE-T forced test mode. In this mode, the PHY can be forced into 1000BASE-T mode and does not require manual setting of master/slave at the two ends of the link. This mode is for test purposes only, and should not be used in normal operation. To configure a PHY in this mode, set register 17E2, bit 5 = 1 and register 0, bits 6 and 13 = 10.

2.3.4 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the F104S8A device includes a robust automatic crossover detection feature for all three speeds on the twisted pair interface (10BASE-T, 100BASE-T, and 1000BASE T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs — a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note The F104S8A device can be configured to perform HP Auto-MDIX, even when autonegotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To use the feature, also set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 1. Supported MDI Pair Combinations

1, 2	3, 6	4, 5	7, 8	Mode
A	B	C	D	Normal MDI

Table 1. Supported MDI Pair Combinations *(continued)*

1, 2	3, 6	4, 5	7, 8	Mode
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

2.3.5 Manual MDI/MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

2.3.6 Link Speed Downshift

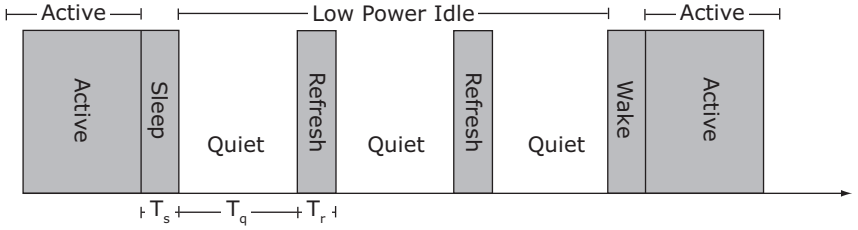
For operation in cabling environments that are incompatible with 1000BASE-T, the F104S8A device provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state when a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1. For more information, see Table 45, page 59.

2.3.7 Energy Efficient Ethernet

The F104S8A device supports the IEEE 802.3az Energy Efficient Ethernet standard to provide a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low-power idles (LPI) to achieve this objective.

Figure 5. Low-Power Idle Operation



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low-power idle state. Energy is saved on the link by cycling between active and low-power idle states. During LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization. The F104S8A uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation.

In addition, the IEEE 802.3az standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V_{p-p} to approximately 3.3 V_{p-p}. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T compliant PHYs over 100 m Cat5 cable or better.

To configure the F104S8A device in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional energy efficient Ethernet features are controlled through Clause 45 registers. For more information, see "Clause 45 Registers to Support Energy Efficient Ethernet and 802.3bf," page 76.

2.4 Reference Clock

The device reference clock supports 125 MHz and 156.25 MHz compliant clock signals. The clock signal must be capacitively coupled and LVDS complaint.

2.4.1 Configuring the Reference Clock

The REFCLK_SEL1 and REFCLK_SEL0 pins configure the reference clock speed. The following table shows the functionality and associated reference clock frequency.

Table 2. REFCLK Frequency Selection

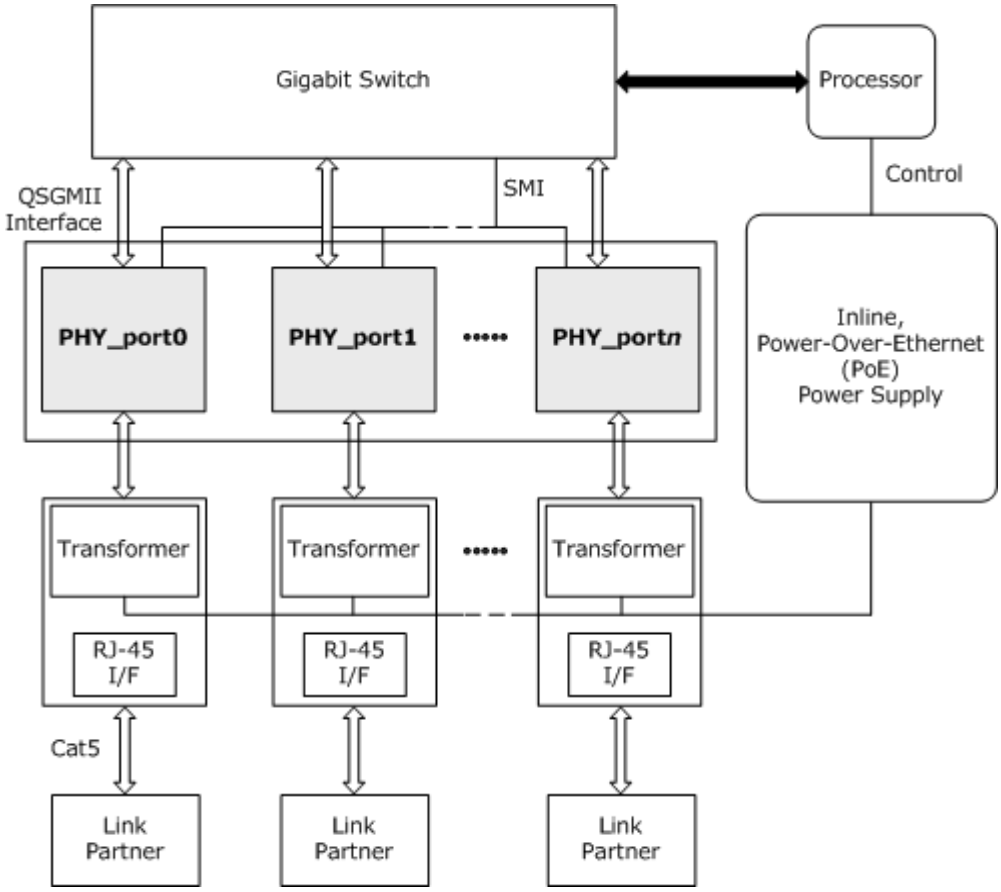
REFCLK_SEL1	REFCLK_SEL0	Frequency
0	0	125 MHz
1	0	156.25 MHz

2.5 Ethernet Inline-Powered Devices

The F104S8A device can detect legacy inline-powered devices in Ethernet network applications. Inline-powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline-powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline-powered device detection, visit the Cisco Web site at www.cisco.com. The following illustration shows an example of an inline-powered Ethernet switch application.

Figure 6. Inline-Powered Ethernet Switch Diagram



The following procedure describes the process that an Ethernet switch must perform to process inline-power requests made by a link partner that is, in turn, capable of receiving inline-power:

1. Enable the inline-powered device detection mode on each F104S8A PHY using its serial management interface. Set register bit 23E1.10 to 1.

2. Ensure that the autonegotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse signal to the link partner. Reading register bit 23E1.9:8 returns 00 during the search for devices that require power over Ethernet (PoE).

3. The F104S8A PHY monitors its inputs for the fast link pulse signal looped back by the link partner. A link partner capable of receiving PoE loops back the fast link pulses when the link partner is powered down. This is reported when register bit 23E1.9:8 reads back 01. It can also be verified as an inline-power detection interrupt by reading register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. When a link partner device does not loop back the fast link pulse after a specific time, register bit 23E1.9:8 automatically resets to 10.

4. If the F104S8A PHY reports that the link partner requires PoE, the Ethernet switch must enable inline-power on this port, independent of the PHY.

5. The PHY automatically disables inline-powered device detection when the register bits 23E1.9:8 automatically reset to 10, and then automatically changes to its normal autonegotiation process. A link is then autonegotiated and established when the link status bit is set (register bit 1.2 is set to 1).

6. In the event of a link failure (indicated when register bit 1.2 reads 0), it is recommended that the inline-power be disabled to the inline-powered device, independent of the PHY. The F104S8A PHY disables its normal autonegotiation process and re-enables its inline-powered device detection mode.

2.6 IEEE 802.3af Power Over Ethernet Support

The device is compatible with designs that are intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

2.7 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of fast link pulse over copper media.

The ActiPHY power management mode in the device is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

- Low-power state
- Link partner wake-up state
- Normal operating state (link-up state)

The F104S8A device switches between the low-power state and link partner wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low-power state after the expiration of the link status time-out timer. After reset, the PHY enters the low-power state.

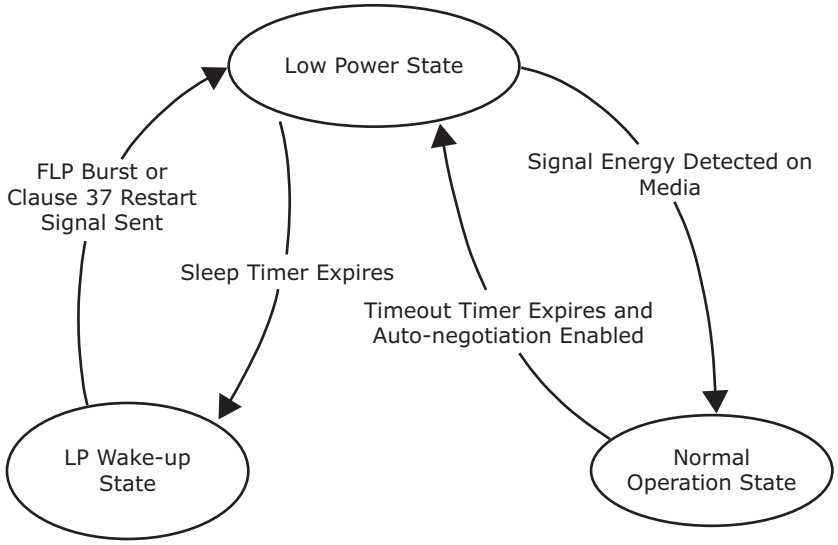
When autonegotiation is enabled in the PHY, the ActiPHY state machine operates as described.

When autonegotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low-power state, the PHY continues to transition between the low-power and link partner wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped.

When autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low-power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 7. ActiPHY State Diagram



2.7.1 Low-Power State

In the low-power state, all major digital blocks are powered down. However, the SMI interface (MDC, MDIO, and MDINT) functionality is provided.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low-power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Autonegotiation-capable link partner
- Another PHY in enhanced ActiPHY link partner wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to link partner wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

2.7.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete fast link pulse bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, SMI interface (MDC, MDIO, and MDINT) functionality is provided.

After sending signal energy on the relevant media, the PHY returns to the low-power state.

2.7.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low-power state.

2.8 Serial Management Interface

The device includes an IEEE 802.3-compliant serial management interface (SMI) that is controlled by its MDC, MDIO, and MDINT pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

Energy efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For information about available register settings, see Table 24, page 47 and Table 72, page 76.

The SMI is a synchronous serial interface with input data to the device on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2-kΩ pull-up resistor is required on the MDIO pin.

2.8.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

Figure 8. SMI Read Frame

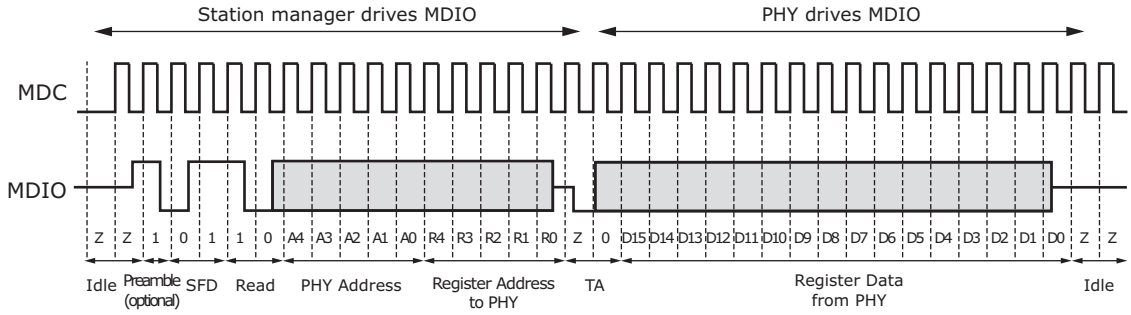
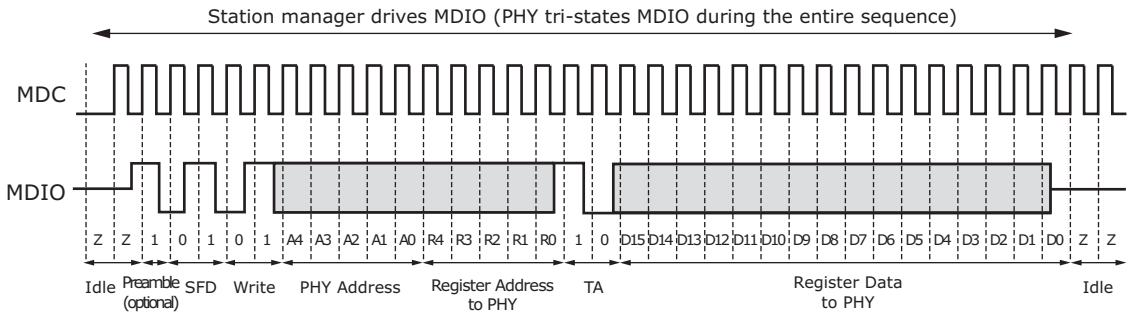


Figure 9. SMI Write Frame



The following list defines the terms used in the SMI read and write timing diagrams.

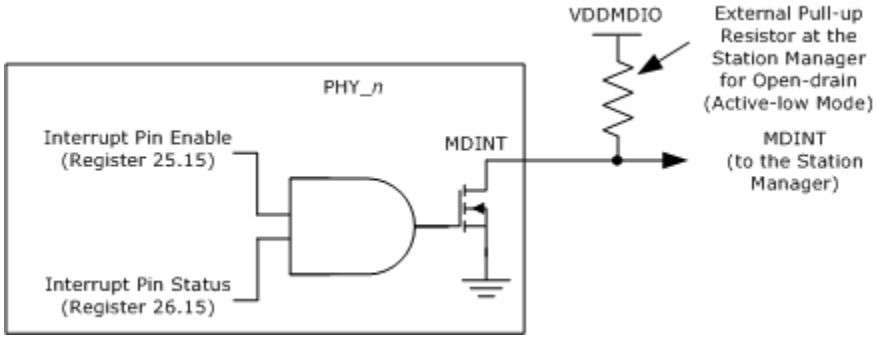
- **Idle** During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode does not contain any transitions on MDIO, the number of bits is undefined during idle.
- **Preamble** By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least 1 bit; otherwise, it can be of an arbitrary length.
- **Start of Frame Delimiter (SFD)** A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.
- **Read or Write Opcode** A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.
- **PHY Address** The particular F104S8A device responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).
- **Register Address** The next five bits are the register address.
- **Turnaround** The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the device drives the second TA bit, a logical 0.
- **Data** The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.
- **Idle** The sequence is repeated.

2.8.2 SMI Interrupt

The SMI includes an output interrupt signal, MDINT, for signaling the station manager when certain events occur in the F104S8A device.

When a PHY generates an interrupt, the MDINT pin is asserted if the interrupt pin enable bit (MII register 25.15) is set. The MDINT pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

Figure 10. MDINT Configured as an Open-Drain (Active-Low) Pin



2.9 LED Interface

The LED interface supports the following configurations: direct drive, basic serial LED mode, and enhanced serial LED mode. The polarity of the LED outputs is programmable and can be changed using register 17E2, bits 13:10. The default polarity is active low.

Direct drive mode provides four LED signals per port, LED0_[0:3] through LED3_[0:3]. The mode and function of each LED signal can be configured independently. When serial LED mode is enabled, the direct drive pins not used by the serial LED interface remain available.

In basic serial LED mode, all signals that can be displayed on LEDs are sent as LED_Data and LED_CLK for external processing.

In enhanced serial LED mode, up to four LED signals per port can be sent as LED_Data, LED_CLK, LED_LD, and LED_Pulse. The following sections provide detailed information about the various LED modes.

Note LED number is listed using the convention, LED<LED#>_<Port#>.

The following table shows the bit 9 settings for register 14G that are used to control the LED behavior for all the LEDs in the F104S8A device.

Table 3. LED Drive State

Setting	Active	Not Active
14G[9: 1] (default)	Ground	Tristate
14G[9: 0] (alternate setting)	Ground	Vdd

2.9.1 LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The default LED state is active low but can be changed by modifying the value in register 17E2, bits 13:10. The blink/pulse stretch is dependent on the LED behavior setting in register 30.

The following table provides a summary of the LED modes and functions. The modes listed are equivalent to the setting used in register 29 to configure each LED pin.

Table 4. LED Mode and Function Summary

Mode	Function Name	LED State and Description
0	Link/Activity	1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1: No link in 1000BASE-T. 0: Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.
2	Link100/Activity	1: No link in 100BASE-TX. 0: Valid 100BASE-TX. Blink or pulse-stretch = Valid 100BASE-TX link with activity present.
3	Link10/Activity	1: No link in 10BASE-T. 0: Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1: No link in 100BASE-TX or 1000BASE-T. 0: Valid 100BASE-TX or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1: No link in 10BASE-T or 1000BASE-T. 0: Valid 10BASE-T or 1000BASE-T link. Blink or pulse-stretch = Valid 10BASE-T or 1000BASE-T link with activity present.
6	Link10/100/Activity	1: No link in 10BASE-T or 100BASE-TX. 0: Valid 10BASE-T or 100BASE-TX, link. Blink or pulse-stretch = Valid 10BASE-T or 100BASE-TX link with activity present.
7	Reserved	Reserved
8	Duplex/Collision	1: Link established in half-duplex mode, or no link established. 0: Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1: No collision detected. Blink or pulse-stretch = Collision detected.
10	Activity	1: No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present when register bit 30.14 is set to 1).
11	Reserved	Reserved