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F1975 Datasheet

6-Bit, 75 Ω, Digital Step Attenuator — 5 to 3000 MHz

General Description

This document describes the specification for the IDT F1975 Digital Step Attenuator. The F1975 is part of a family of *Glitch-Free™* DSAs optimized for the demanding requirements of CATV and Satellite systems. This device is offered in a compact 4 mm x 4 mm 20 pin Thin QFN package with 75 Ω impedance for ease of integration.

Competitive Advantage

Digital step attenuators are used in Receivers and Transmitters to provide gain control. The F1975 is a 6-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (+64 dBm IIP3). The device has pinpoint attenuation accuracy. Most importantly, the F1975 includes IDT's *Glitch-Free™* technology which results in low overshoot & ringing during MSB transitions.

- ✓ *Glitch-Free™* Technology protects PA or ADC from damage during transitions between attenuation states.
- ✓ Extremely accurate attenuation levels
- ✓ Ultra low distortion
- ✓ Lowest insertion loss for best SNR

Applications

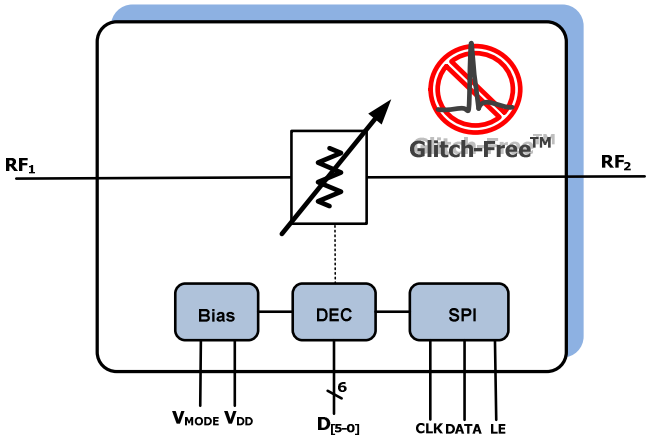
- CATV Infrastructure
- CATV Set-Top Boxes
- CATV Satellite Modems
- Data Network Equipment
- Fiber Networks

Ordering Information

Features

- Serial & 6-Bit Parallel Interface
- 31.5 dB Control Range
- 0.5 dB step
- *Glitch-Free™*, low transient overshoot
- 3.0 V to 5.25 V supply
- 1.8 V or 3.3 V control logic
- Attenuator Step Error: 0.1 dB @ 1 GHz
- Low Insertion Loss: 1.2 dB @ 1 GHz
- Ultra linear IIP3: +64 dBm
- IIP2: +125 dBm typical
- Stable Integral Non-Linearity over temperature
- Low Current Consumption: 550 µA typical
- Bi-Directional
- -40 °C to +105 °C Operating Temperature
- 4 mm x 4 mm Thin QFN 20 pin package

Functional Block Diagram



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
V_{DD} to GND	V_{DD}	-0.3	+5.5	V
DATA, LE, CLK, D[5:0]	V_{Logic}	-0.3	Min (V_{DD}+0.3, 3.6)	V
RF1, RF2	V_{RF}	-0.3	+0.3	V
Maximum Input Power applied to RF1 or RF2 (>100 MHz)	P_{RF}		+34	dBm
Maximum Junction Temperature	T_{Jmax}		+140	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10 s)			260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		2000 (Class 2)	Volts
ESD Voltage – CDM (Per JESD22-C101F)	V_{ESDCDM}		250 (Class C1)	Volts

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	50 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	3 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

F1975 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{DD}		3.00		5.25	V
Frequency Range	F_{RF}		5		3000	MHz
Operating Temperature Range	T_{CASE}	Exposed Paddle	-40		105	°C
RF CW Input Power	PCW	RF1 or RF2			See Figure 1	dBm
RF1 Impedance	Z_{RF1}	Single Ended		75		Ω
RF2 Impedance	Z_{RF2}	Single Ended		75		Ω

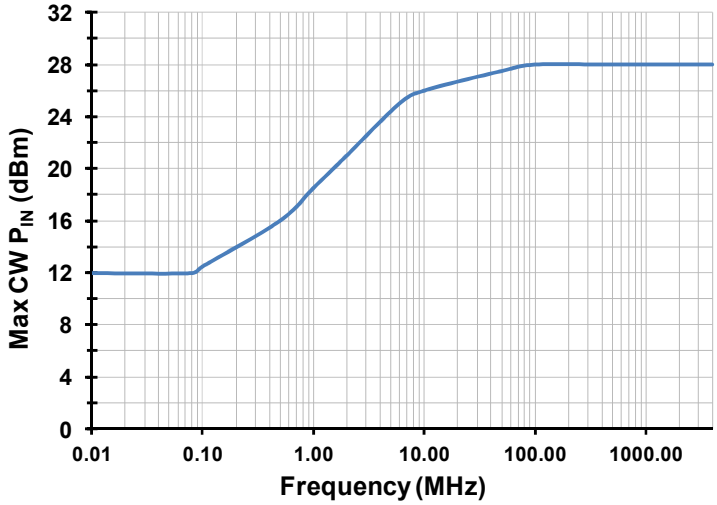


Figure 1 Maximum Continuous Operating RF input power versus Input Frequency

F1975 SPECIFICATION

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25 °C, F_{RF} = 1000 MHz, P_{in} = 0 dBm, Serial Mode, $Z_{RF1} = Z_{RF2}$ = 75 Ω, unless otherwise noted. EvKit losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High	V_{IH}	All Control Pins				
		V_{DD} > 3.6 V	***1.17***		***3.6***	V
		3.0 ≤ V_{DD} ≤ 3.6 V	***1.17***		V_{DD}	V
Logic Input Low	V_{IL}	All Control Pins			***0.63***	V
Logic Current	I_{IH}, I_{IL}	All Control Pins	***-35***		***+35***	µA
Supply Current	I_{DD}	V_{DD} = 3.3 V		550	***830***[1]	µA
		V_{DD} = 5.0 V		620	***900***	
RF1 Return Loss	S_{11}			18		dB
RF2 Return Loss	S_{22}			18		dB
Attenuation Step	LSB	Least Significant Bit		0.5		dB
Insertion Loss (Minimum Attenuation)	A_{MIN}	D[5:0]=[000000] (IL State)		1.2	***2.0***	dB
Attenuation Range	A_{RANGE}	D[5:0]=[111111]=31.5 dB	30.5[2]	31.1	31.7	dB
Step Error	DNL			0.1		dB
Absolute Error	INL	D[5:0]=[100111]= 19.5 dB	***-0.7***		***+0.5***	dB
Insertion Phase Delta	Φ_{Δ}	At 0.5 GHz (A_{MAX} to A_{MIN})		10		degrees
		At 1.0 GHz (A_{MAX} to A_{MIN})		20		
Input IP3	IIP3	P_{IN} = +10 dBm/tone, F1 = 900 MHz, F2 = 950 MHz				dBm
		Attn = 0.0 dB, RF_{IN} = RF1	60	64		
		Attn =15.5 dB, RF_{IN} = RF1	59	62		
Input IP2	IIP2	P_{IN} = +12 dBm/tone, F1= 945 MHz, F2 = 949 MHz F1+F2 = 1894 MHz RF_{IN}= RF1		125		dBm
Second Harmonic	H2	P_{IN} = +15 dBm, RF_{IN} = 945 MHz RF_{OUT} = 1890 MHz RF_{IN} Port = RF1		108		dBc
0.1dB Compression[3]	$P_{0.1}$	D[5:0] = [000000] = A_{MIN}, RF_{IN} = RF1		30.5		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 0.1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power. Measured in a 50 ohm system.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.
Note 5: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).

F1975 SPECIFICATION (CONTINUED)

Specifications apply at V_{DD} = +3.3 V, T_{CASE} = +25 °C, F_{RF} = 1000 MHz, P_{in} = 0 dBm, Serial Mode, Z_{RF1} = Z_{RF2} = 75 Ω, unless otherwise noted. EvKit losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MSB Step Time	T_{LSB}	Start at LE rising edge End ±0.10 dB Pout settling for 15.5 dB to 16.0 dB transition		500		ns
Maximum spurious level on any RF port[4]	$Spur_{MAX}$			-130		dBm
Maximum Switching Rate	SW_{RATE}			25		kHz
DSA Settling time[5]	τ_{SET}	Max to Min Attenuation to settle to within 0.5 dB of final value		0.9		µs
		Min to Max Attenuation to settle to within 0.5 dB of final value		1.8		
Control Interface	SPI_{BIT}			6		bit
Serial Clock Speed	SPI_{CLK}			10	***25***	MHz

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: The input 0.1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.
Note 5: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).

PROGRAMMING OPTIONS

F1975 can be programmed using either the parallel or serial interface which is selectable via V_{MODE} (pin 13). Serial Mode is selected by floating V_{MODE} or pulling it to a logic high and parallel mode is selected by setting V_{MODE} to a logic low.

SERIAL CONTROL MODE

F1975 Serial Mode is selected by floating V_{MODE} (pin 13) or pulling it to a logic high. The serial interface is a 6-bit shift register and shifts in the MSB (D5) first. When serial programming is used, all the parallel control input pins (1, 15, 16, 17, 19, 20) must be grounded.

Table 1 - 6 Bit SPI Word Sequence

D5	Attenuation 16 dB Control Bit
D4	Attenuator 8 dB Control Bit
D3	Attenuator 4 dB Control Bit
D2	Attenuator 2 dB Control Bit
D1	Attenuator 1 dB Control Bit
D0	Attenuator 0.5 dB Control Bit

Table 2 - Truth Table for Serial Control Word

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

Serial Mode Register Timing Diagram: (Note the Timing Spec Intervals in Blue)

The F1975 can be programmed via the serial port on the rising edge of Latch Enable (LE). Refer to Figure 2.

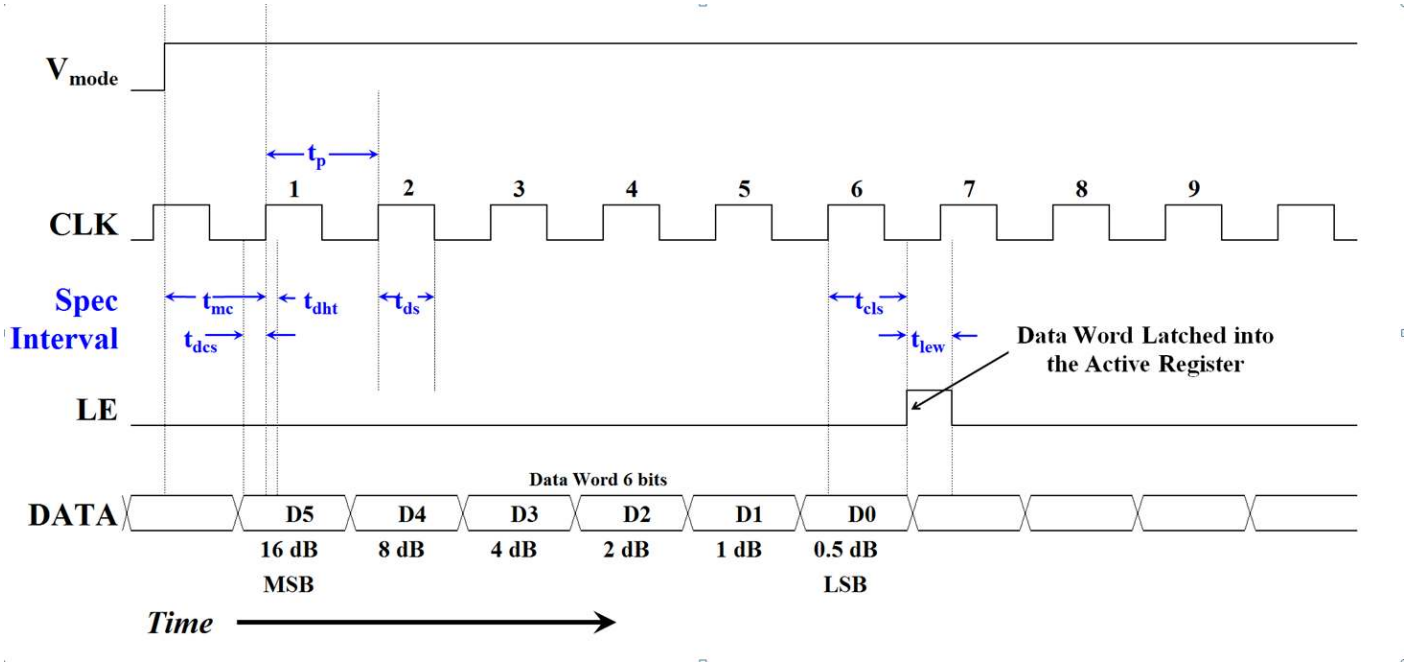


Figure 2 - Serial Register Timing Diagram

***Note** - When Latch enable is high, the shift register is disabled and DATA is NOT continuously clocked into the shift register which minimizes noise. It is recommended that Latch Enable be left high when the device is not being programmed.*

Table 3 - Serial Mode Timing Table

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{mc}	Parallel to Serial Setup Time - From rising edge of V_{MODE} to rising edge of CLK for D5	***100***		ns
t_{ds}	Clock high pulse width	***10***		ns
t_{cls}	LE Setup Time - From the rising edge of CLK pulse for D0 to LE rising edge minus half the clock period.	***10***		ns
t_{lew}	LE pulse width	***30***		ns
t_{dsc}	Data Setup Time - From the starting edge of Data bit to rising edge of CLK	***10***		ns
T_{dht}	Data Hold Time - From rising edge of CLK to falling edge of the Data bit.	***10***		ns

Serial Mode Default Startup Condition:

When the device is first powered up it will default to the Maximum Attenuation of 31.5 dB independent of the V_{MODE} and parallel pin [D5:D0] conditions.

Table 4 - Default Control Word for the Serial Mode

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
1	1	1	1	1	1	31.5

PARALLEL CONTROL MODE

For the F1975 the user has the option of running in one of two parallel modes: Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode:

Direct Parallel Mode is selected when V_{MODE} (pin 13) is set to a logic low and LE (pin 5) is set to a logic high. In this mode the device will immediately react to any voltage changes to the parallel control pins (1, 15, 16, 17, 19, 20). Use direct parallel mode for the fastest settling time.

Direct Parallel Default Startup Condition:

Attenuation value using Direct Parallel Mode is determined by logic condition of the parallel pins (1, 15, 16, 17, 19, 20) at the time of start up.

Latched Parallel Mode:

Latched Parallel Mode is selected when V_{MODE} is set to a logic low and LE (pin 5) is toggled from a logic low to a logic high. To utilize Latched Parallel Mode:

- Set LE to a logic low.
- Set pins (1, 15, 16, 17, 19, 20) for desired attenuation setting. (While LE is set to a logic low, the attenuation state will not change.)
- Toggle LE to a logic high. The device will then transition to the attenuation settings reflected by pins D5 – D0.

Latched Parallel Default Startup Condition:

Latched Parallel Mode establishes a default attenuation state when the device is first powered up. The default setting is MAXIMUM Attenuation.

Table 5 - Truth Table for the Parallel Pins

D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

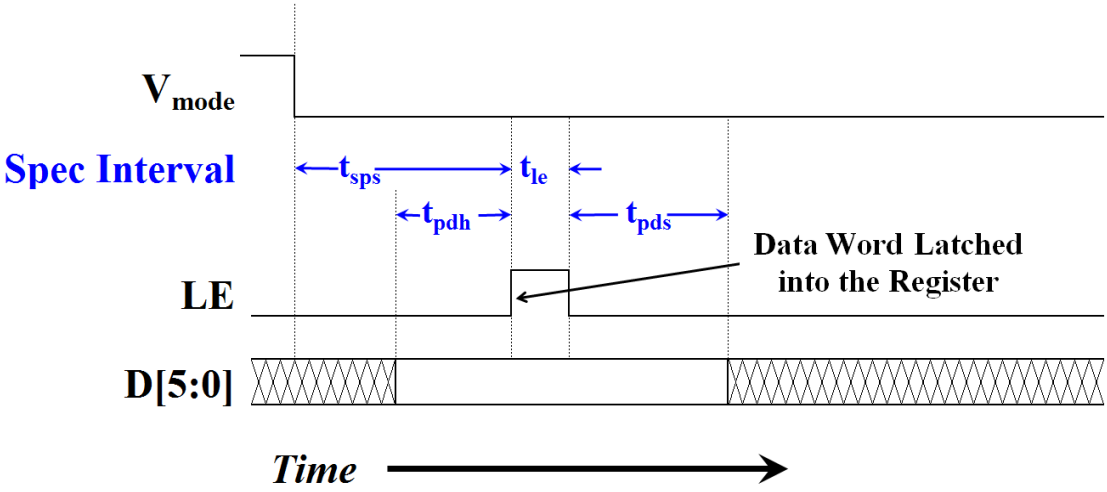


Figure 3 - Latched Parallel Mode Timing Diagram

Table 6 - Latched Parallel Mode Timing

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{sps}	Serial to Parallel Mode Setup Time	100		ns
t_{pdh}	Parallel Data Hold Time	10		ns
t_{pds}	LE minimum pulse width	10		ns
t_{le}	Parallel Data Setup Time	10		ns

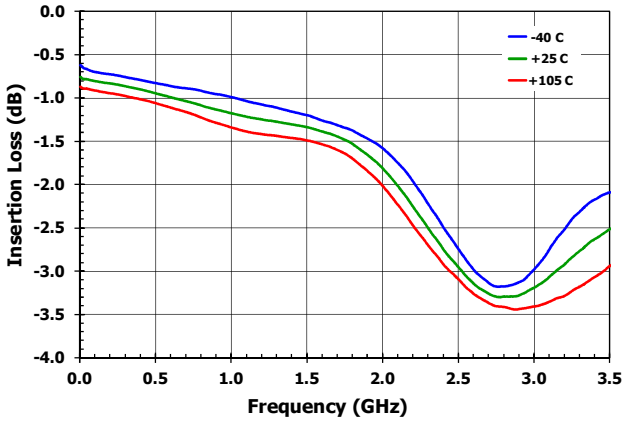
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

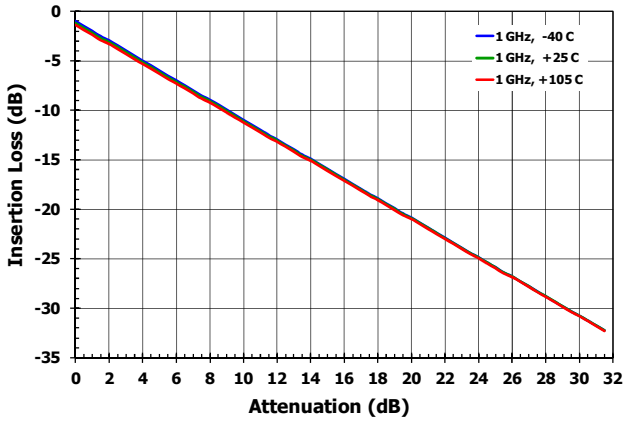
- **V_{DD} = +3.30 V**
- **T_{CASE} = +25 °C**
- **F_{RF} = 1 GHz**
- **P_{IN} = 0 dBm for single tone measurements**
- **P_{IN} = +10 dBm/tone for multi-tone measurements**
- **Tone Spacing = 50 MHz**
- **EVKit connector and board losses are de-embedded**
- **Measured in a 75 ohm system unless otherwise specified**

TYPICAL OPERATING CONDITIONS (- 1 -)

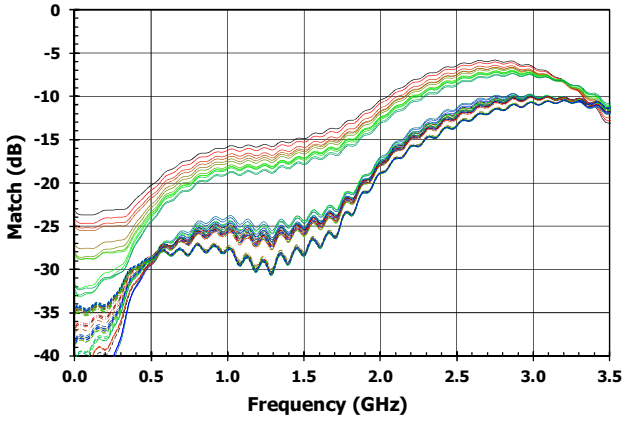
Insertion Loss vs Frequency



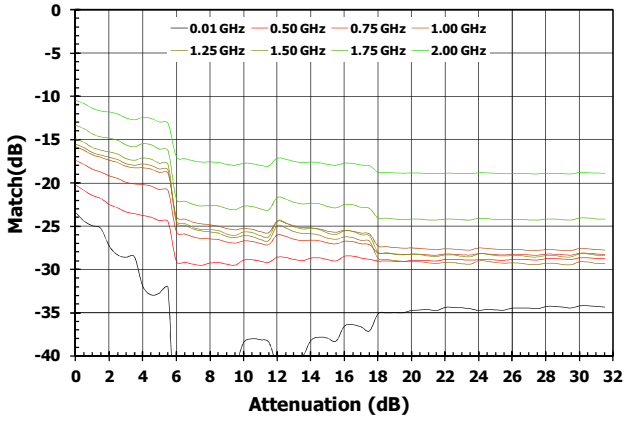
Insertion Loss vs Attenuation State



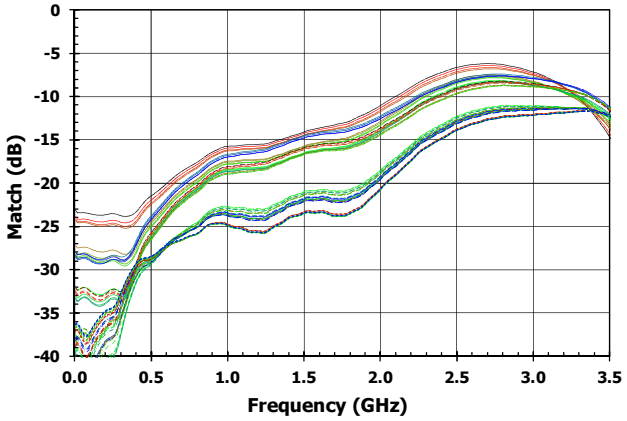
RF1 Return Loss vs Frequency (All States)



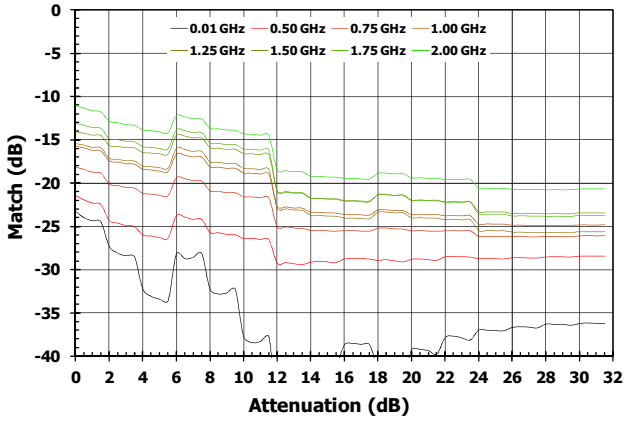
RF1 Return Loss vs Attenuation State



RF2 Return Loss vs Frequency (All States)

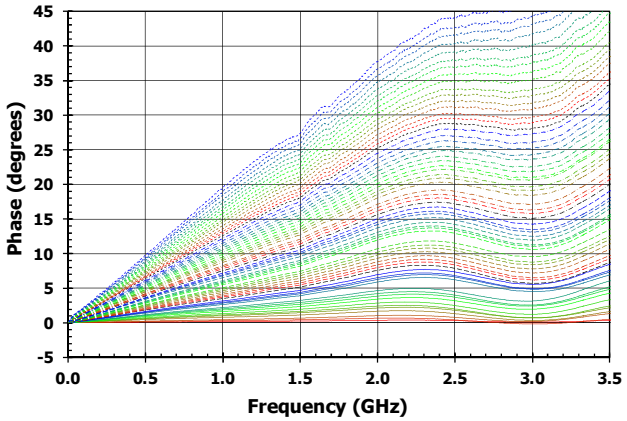


RF2 Return Loss vs Attenuation State

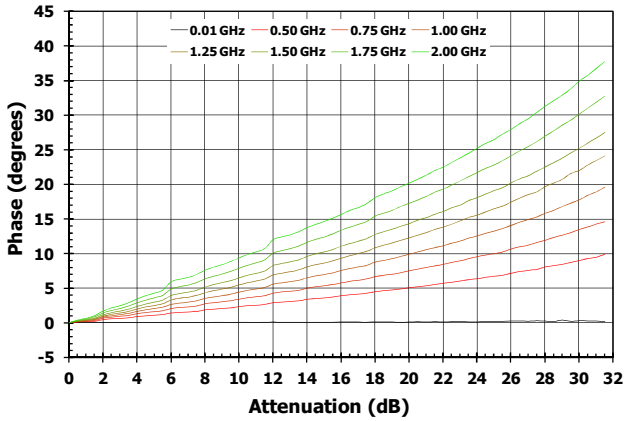


TYPICAL OPERATING CONDITIONS (- 2 -)

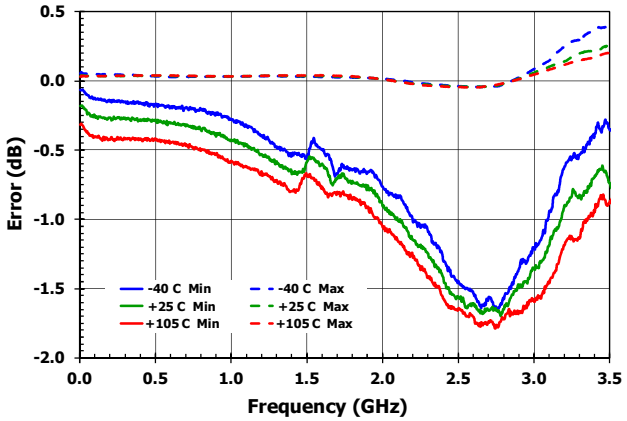
Relative Insertion Phase vs Frequency (All States)



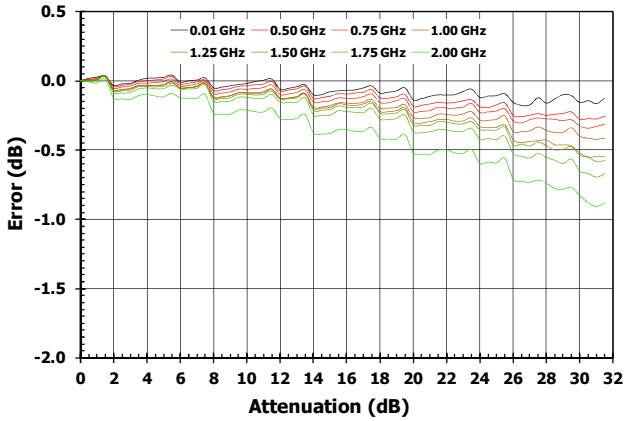
Relative Insertion Phase vs Attenuation



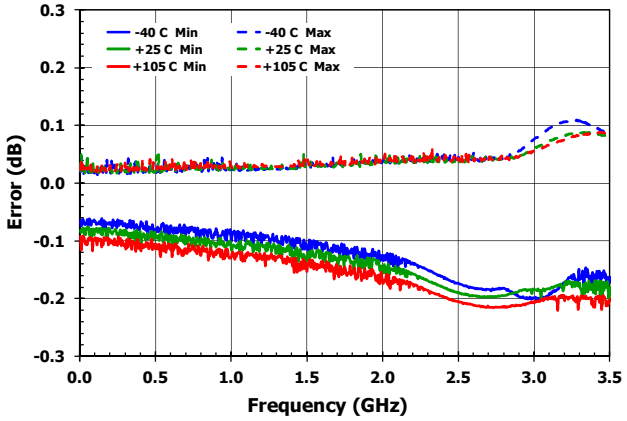
Worst Case Absolute Accuracy Error



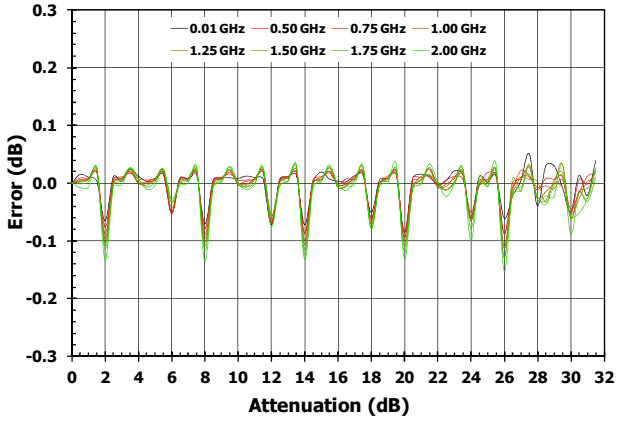
Accuracy Error vs Attenuation



Worst Case Step Accuracy

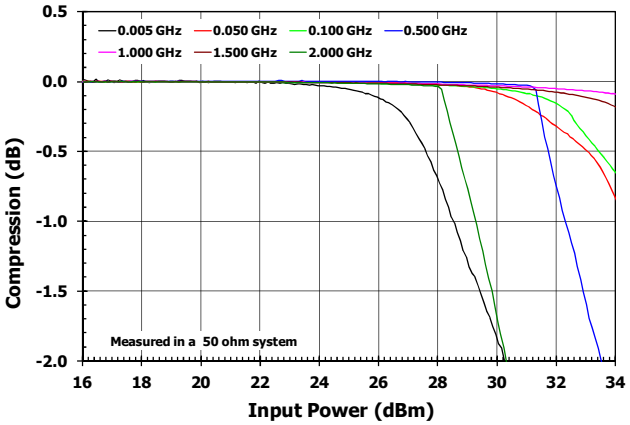


Step Error vs Attenuation

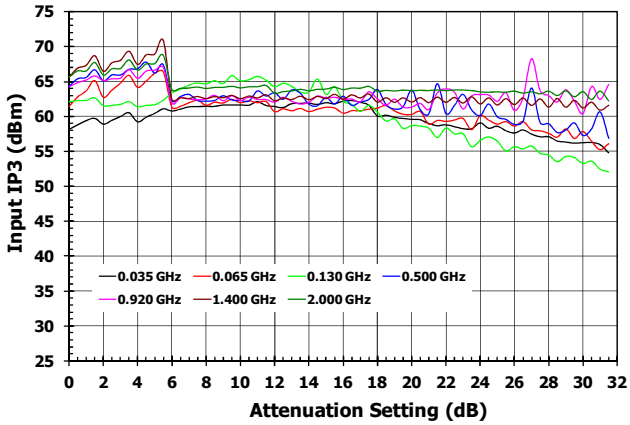


TYPICAL OPERATING CONDITIONS (- 3 -)

Compression [Attenuation = 0.0 dB]

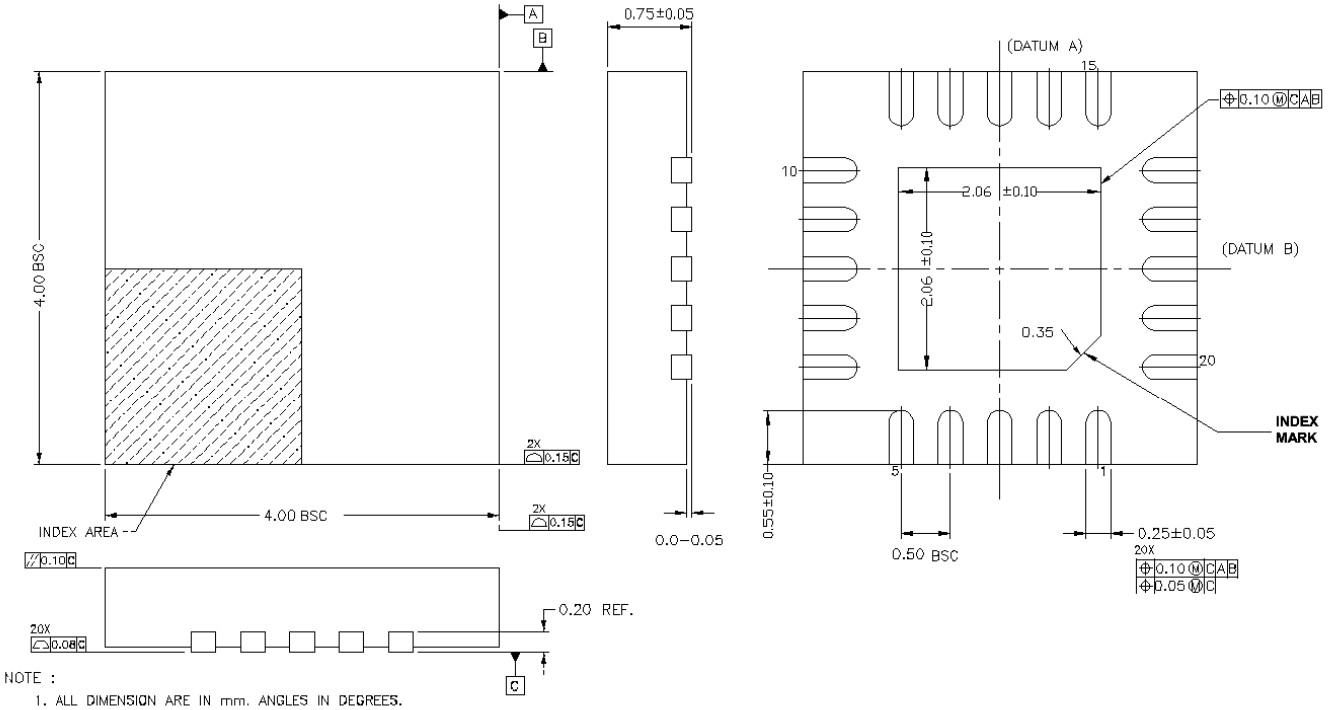


Input IP3



PACKAGE DRAWING

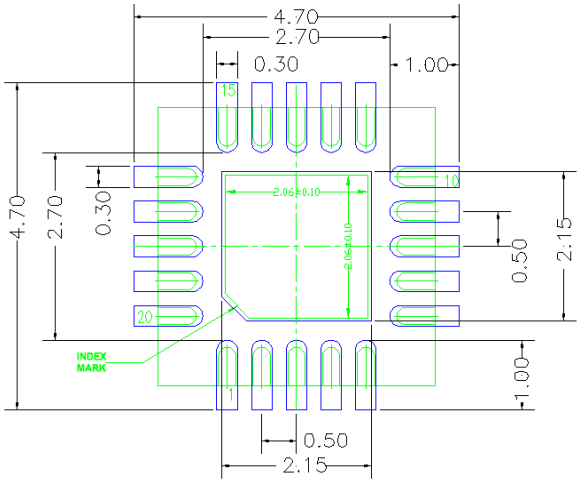
(4 mm x 4 mm 24-pin TQFN), **NCG20**



NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. REFER JEDEC MO-220.

LAND PATTERN DIMENSION



RECOMMENDED LAND PATTERN DIMENSION

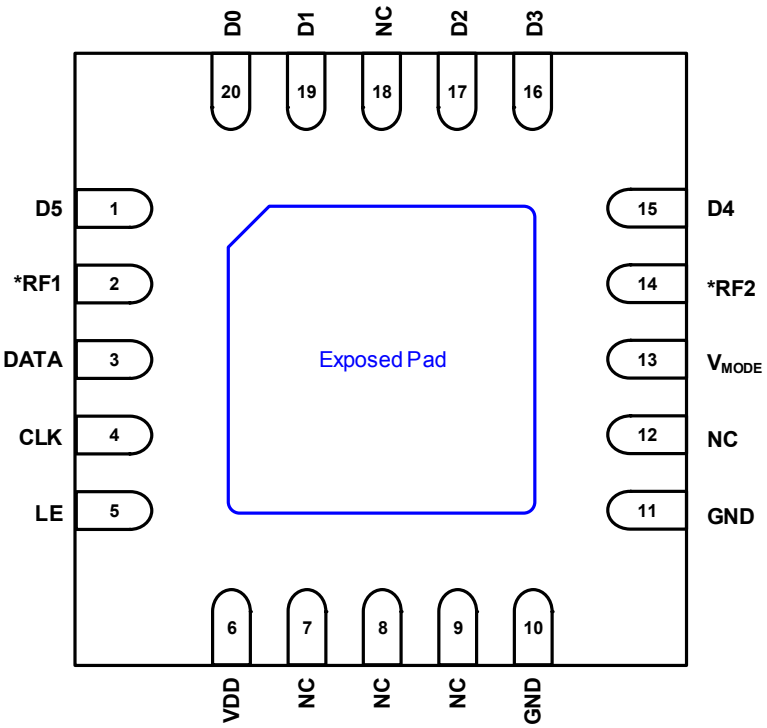
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

PIN DIAGRAM

TOP View

(looking through the top of the package)

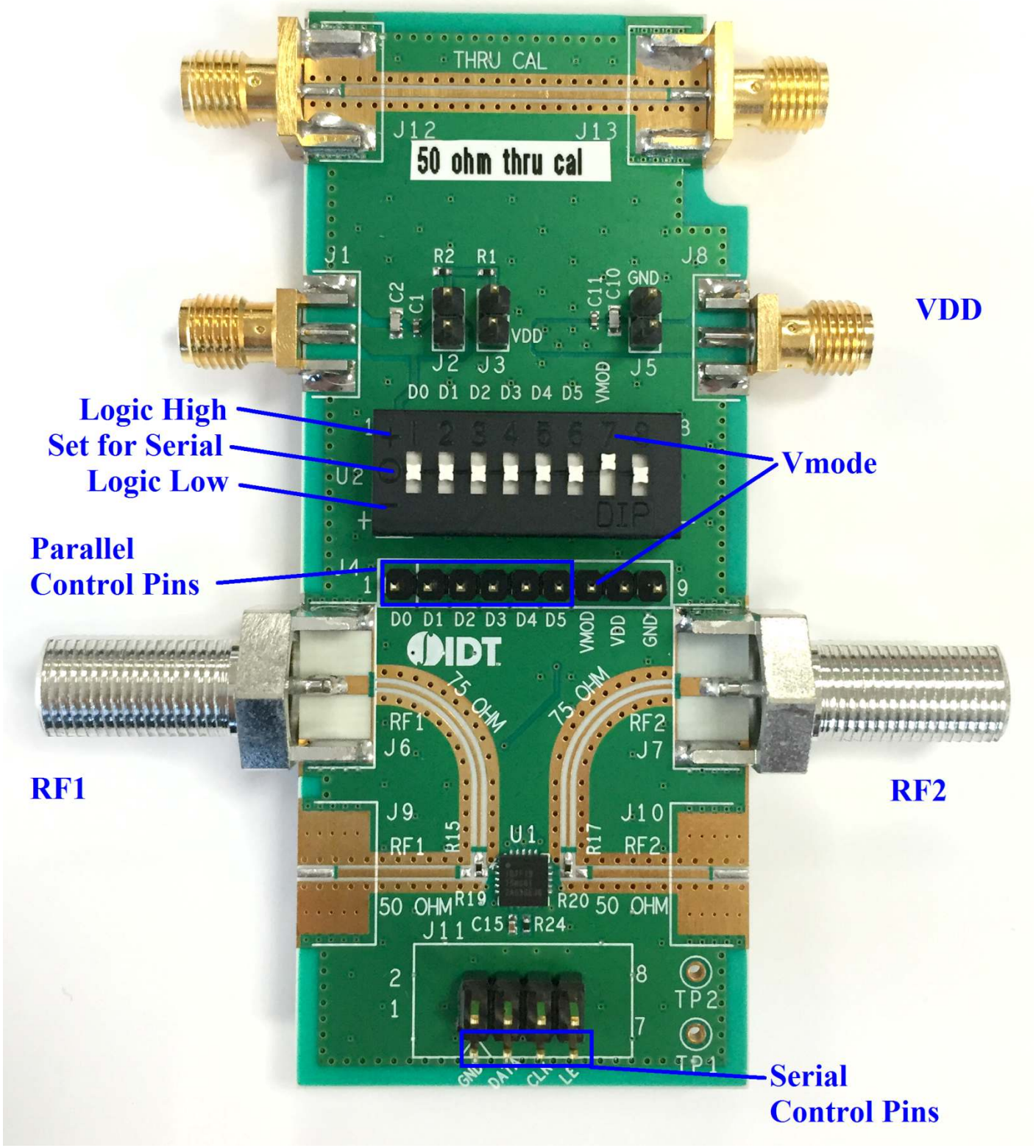


** Device is RF Bi-Directional*

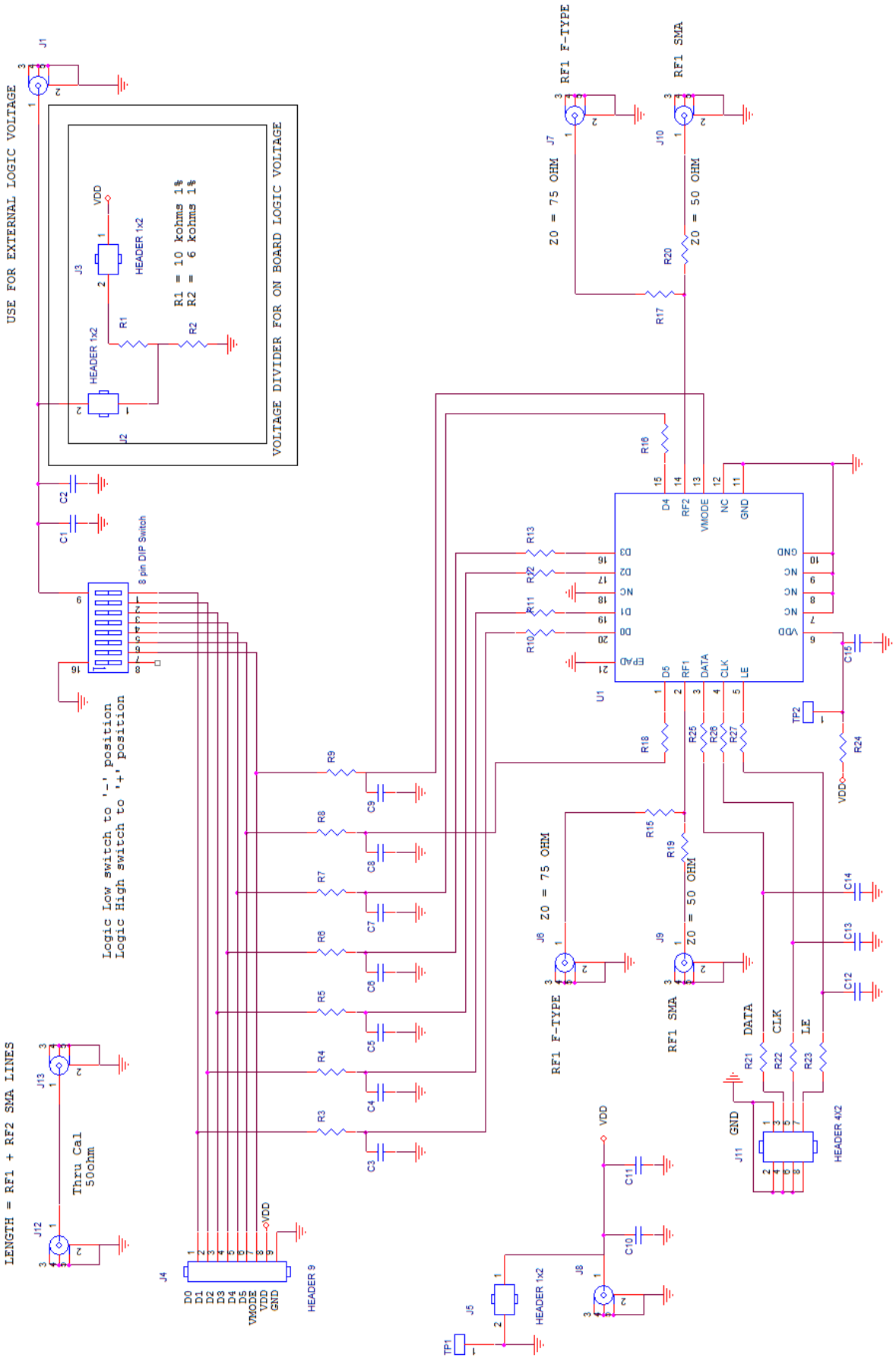
PIN DESCRIPTION

PIN	NAME	FUNCTION
1	D5	16 dB Attenuation Control Bit. Activated by Logic High (see page 8)
2	RF1	Device RF input or output (bi-directional).
3	DATA	Serial interface Data Input
4	CLK	Serial interface Clock Input
5	LE	Serial interface Latch Enable Input. Internal pullup (100 kohm)
6	VDD	Power supply pin
7	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended)
8	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended)
9	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended)
10	GND	Connect to Ground. This pin is internally connected to the exposed paddle
11	GND	Connect to Ground. This pin is internally connected to the exposed paddle
12	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended)
13	VMODE	Pull high for serial control mode. Ground for parallel control mode.
14	RF2	Device RF input or output (bi-directional).
15	D4	8 dB Attenuation Control Bit. Activated by Logic High (see page 8)
16	D3	4 dB Attenuation Control Bit. Activated by Logic High (see page 8)
17	D2	2 dB Attenuation Control Bit. Activated by Logic High (see page 8)
18	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
19	D1	1 dB Attenuation Control Bit. Activated by Logic High (see page 8)
20	D0	0.5 dB Attenuation Control Bit. Activated by Logic High (see page 8)
EP	Exposed Paddle	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

EVKIT PICTURE



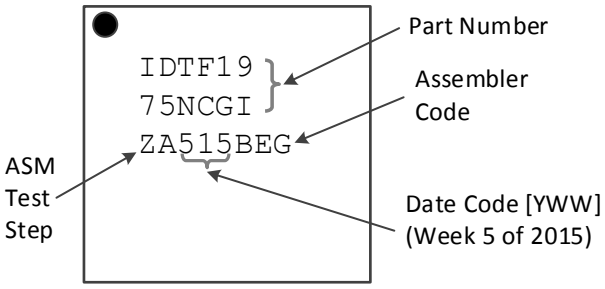
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM (REV 1)

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C1, C11, C15	3	100nF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	MURATA
2	C2, C10	2	10nF ±5%, 50V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	MURATA
3	C3, C4, C5, C6, C7, C8, C9, C12, C13, C14	10	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
4	R3, R4, R5, R6, R7, R8, R9	7	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
5	R10-R13, R15-R18, R24-R27	12	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
6	R21, R22, R23	3	3kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3001X	PANASONIC
7	R1	1	100kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	PANASONIC
8	R2	1	267kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2673X	PANASONIC
9	J2, J3, J5	3	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
10	J11	1	CONN HEADER VERT DBL 4 X 2 POS GOLD	67997-108HLF	FCI
11	J4	1	CONN HEADER VERT SGL 9 X 1 POS GOLD	961109-6404-AR	3M
12	J1, J8	2	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
13	J6, J7	2	Edge Launch F TYPE 75 ohm	222181	Amphenol
14	U2	1	SWITCH 8 POSITION DIP SWITCH	KAT1108E	E-Switch
15	U1	1	DSA	F1975	IDT
16		1	Printed Circuit Board	F1975 Evkit Rev 01	IDT

TOP MARKINGS



APPLICATIONS INFORMATION

F1975 Digital Pin Voltage & Resistance Values (pins not connected)

The following table lists the resistance between various pins and ground when no DC power is applied. When the device is powered up with +5 Volts DC, these pins will exhibit a voltage to ground as indicated.

Pin	Name	DC voltage (volts)	Resistance (ohms)
13	V_{MODE}	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V
3, 4, 5	DATA, CLK, LE	2.5 V	100 kΩ pullup resistor to internally regulated 2.5 V

REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
O	2016-01-15		Initial Release

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