



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



GENERAL DESCRIPTION

The F2923 is a low insertion loss 50Ω SP2T absorptive RF Switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 300 kHz to 8000 MHz. In addition to providing low insertion loss, industry leading isolation at 2 GHz and excellent linearity, the F2923 also includes a patent pending constant impedance (K_z) feature. K_z minimizes LO pulling in VCOs and reduces phase and amplitude variations in distribution networks. It is also ideal for dynamic switching/selection between two or more amplifiers while avoiding damage to upstream/downstream sensitive devices such as PAs and ADCs.

The F2923 uses a single positive supply voltage of 3.3 V supporting three states using either 3.3 V or 1.8 V control logic. An added feature includes a ModeCTL pin allowing the user to control the device with either 1-pin or 2-pin control.

COMPETITIVE ADVANTAGE

The F2923 provides constant impedance on all ports during transitions without compromising isolation, linearity, or insertion loss.

- ✓ Constant impedance $K_{|z|}$ during switching transition
 - ✓ VSWR RF_Com port 1.4:1 vs. 9:1 for Standard Switch
 - ✓ Insertion Loss = 0.48 dB*
 - ✓ IIP3: +66 dBm*
 - ✓ RF1/RF2 to RF_COM Isolation = 74 dB*
 - ✓ Extended temperature: -55 °C to +105 °C
 - ✓ Negative supply voltage not required
- *2 GHz

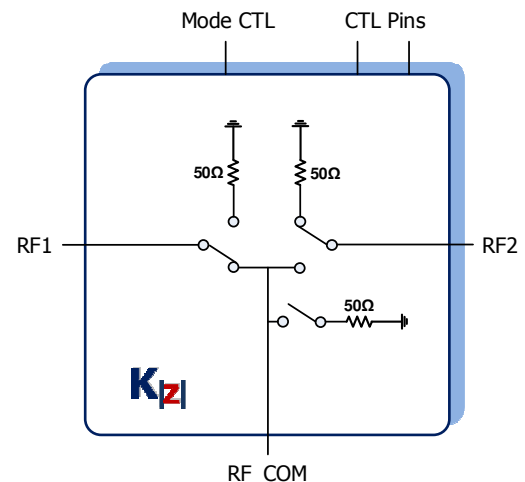
APPLICATIONS

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

FEATURES

- Constant Impedance $K_{|z|}$ during transition
- Very low insertion loss: 0.48 dB @ 2 GHz
- High Input IP3: 66 dB @ 2 GHz
- RF1/RF2 to RF_Com Isolation: 74 dB @ 2 GHz
- 1-pin or 2-pin device control option
- Low DC current: 127 μA using 3.3 V logic
- Supply voltage: 3.3 V
- Supports 1.8 V and 3.3 V control logic
- Extended temperature: -55 °C to +105 °C
- 4 mm x 4 mm, 20-pin TQFN package
- Pin compatible with F2912

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

| Parameter / Condition | Symbol | Min | Max | Unit |
|-------------------------------------|---------------------|------|-----------------------|------|
| V _{CC} to GND | V _{CC} | -0.3 | +3.9 | V |
| CTL1, CTL2 | V _{CNTL} | -0.3 | V _{CC} + 0.3 | V |
| ModeCTL to GND | V _{MODE} | -0.3 | V _{CC} + 0.3 | V |
| RF1, RF2, RF_COM | V _{RF} | -0.3 | +0.3 | V |
| Maximum Junction Temperature | T _{Jmax} | | +140 | °C |
| Storage Temperature Range | T _{ST} | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | T _{LEAD} | | +260 | °C |
| ESD Voltage– HBM (Per JESD22-A114) | V _{ESDHBM} | | Class 2 | |
| ESD Voltage – CDM (Per JESD22-C101) | V _{ESDCDM} | | Class III | |

ABS MAX RF POWER AT 2 GHz WITH T_c = +85 °C *

| | |
|---|--------|
| RF1, RF2, RF_COM (RF1 or RF2 is connected to RF_COM, IL States) | +33dBm |
| RF1, RF2, RF_COM (When port is internally terminated) | +24dBm |

ABS MAX RF POWER AT 2 GHz WITH T_c = +105 °C *

| | |
|---|--------|
| RF1, RF2, RF_COM (RF1 or RF2 is connected to RF_COM, IL States) | +33dBm |
| RF1, RF2, RF_COM (When port is internally terminated) | +21dBm |

* Temperature of exposed paddle

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

| | |
|---|----------|
| θ _{JA} (Junction – Ambient) | 60 °C/W |
| θ _{JC} (Junction – Case) The Case is defined as the exposed paddle | 3.9 °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | MSL1 |

F2923 RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---------------|---|-----|-----|------|-------------|
| Supply Voltage | V_{CC} | | 3.1 | | 3.5 | V |
| Operating Temperature Range | T_{CASE} | Case Temperature | -55 | | +105 | $^{\circ}C$ |
| RF Frequency Range | F_{RF} | | 0.3 | | 8000 | MHz |
| RF Continuous Input Power (CW) ¹ | P_{RF} | Selected Port (I.L. State) | | | 27 | dBm |
| | | Unselected Port ² (Term State) | | | 18 | |
| RF1 Port Impedance | Z_{RF1} | | | 50 | | Ω |
| RF2 Port Impedance | Z_{RF2} | | | 50 | | |
| RF_COM Port Impedance | Z_{RF_COM} | | | 50 | | |

Note 1– See Figure 1 below for RF power handling levels for various conditions.

Note 2– States 1, 2, or 3.

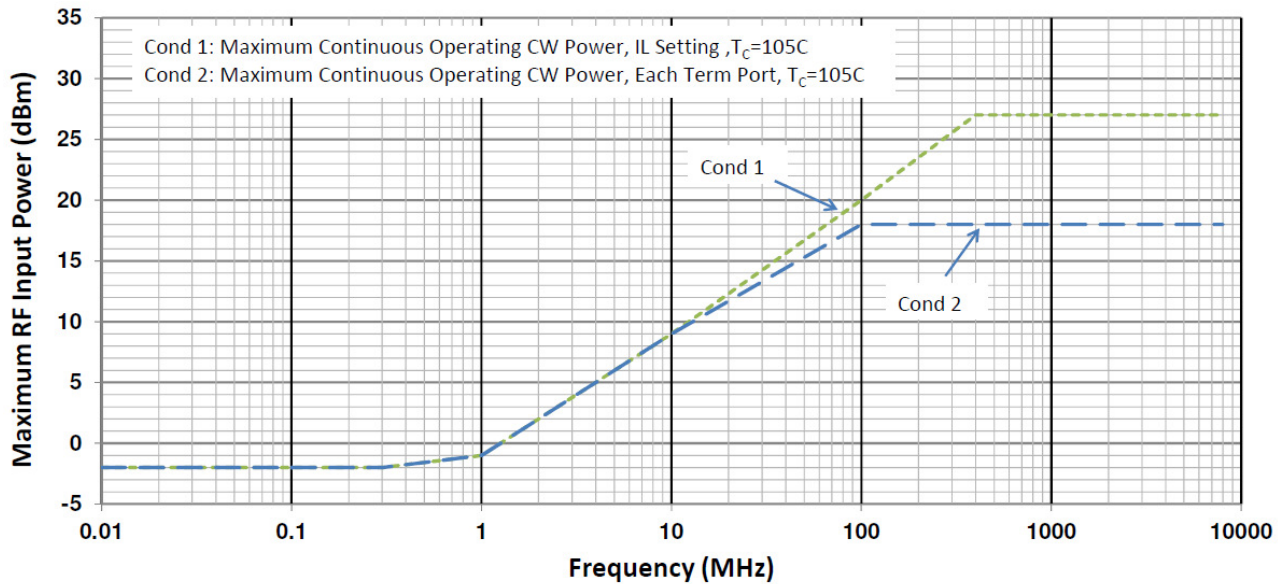


FIGURE 1: MAXIMUM OPERATING RF INPUT POWER VS. RF FREQUENCY

F2923 SPECIFICATION

Typical Application Circuit, $V_{CC} = +3.3\text{ V}$, $T_C = +25\text{ }^\circ\text{C}$, $F_{RF} = 2\text{ GHz}$, input power = 0 dBm unless otherwise stated. PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|------------------|--------------------------|-----------------------|----------|------------------------|---------------|
| Logic Input High Threshold | V_{IH} | CTL1 and CTL2 pins | 1.1 | | 3.6 | V |
| Logic Input Low Threshold | V_{IL} | CTL1 and CTL2 pins | | | 0.6 | V |
| ModeCTL Input High | | | | V_{CC} | | V |
| ModeCTL Input Low | | | | GND | | V |
| Logic Current | I_{IH}, I_{IL} | CTL1, CTL2, ModeCTL pins | | | 1000 | nA |
| DC Current (V_{CC}) | I_{CC} | State 2 or State 3 | | 127 | 150 | μA |
| VSWR during transition | $VSWR_T$ | RF1/RF2 to RF_COM | | 1.4:1 | | - |
| Insertion Loss RF1/RF2 to RF_COM (State 2 or 3) | IL | RF = 1 GHz | | 0.43 | | dB |
| | | RF = 2 GHz | | 0.48 | 0.8¹ | |
| | | RF = 4 GHz | | 0.63 | | |
| | | RF = 6 GHz | | 0.89 | | |
| | | RF = 8 GHz | | 1.12 | | |
| Isolation RF1 / RF2 to RF_COM (State 2 or 3) | ISO1 | RF = 1 GHz | | 77 | | dB |
| | | RF = 2 GHz | 71² | 74 | | |
| | | RF = 4 GHz | | 51 | | |
| | | RF = 6 GHz | | 40 | | |
| | | RF = 8 GHz | | 37 | | |
| Isolation RF1 to RF2 (State 2 or 3) | ISO2 | RF = 1 GHz | | 73 | | dB |
| | | RF = 2 GHz | 61 | 63 | | |
| | | RF = 4 GHz | | 51 | | |
| | | RF = 6 GHz | | 35 | | |
| | | RF = 8 GHz | | 29 | | |
| Return Loss RF_COM (State 1) | RL1 | RF = 1 GHz | | 23.8 | | dB |
| | | RF = 2 GHz | | 25.2 | | |
| | | RF = 4 GHz | | 26.7 | | |
| | | RF = 6 GHz | | 18.4 | | |
| | | RF = 8 GHz | | 16.6 | | |
| Return Loss RF_COM (State 2 or 3) | RL2 | RF = 1 GHz | | 29.6 | | dB |
| | | RF = 2 GHz | | 25.4 | | |
| | | RF = 4 GHz | | 26.1 | | |
| | | RF = 6 GHz | | 17.6 | | |
| | | RF = 8 GHz | | 14.1 | | |

Note 1– Items in min/max columns in **bold italics** are Guaranteed by Test.

Note 2– Items in min/max columns NOT in bold italics are Guaranteed by Design Characterization.

F2923 SPECIFICATION (CONT.)

Typical Application Circuit, $V_{CC} = +3.3\text{ V}$, $T_C = +25\text{ }^\circ\text{C}$, $F_{RF} = 2\text{ GHz}$, input power = 0 dBm unless otherwise stated. PCB board trace and connector losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | |
|--|--------------|---|------------|-------|-----|---------------|--|
| Return Loss RF1, RF2 (State 1) | RL3 | RF = 1 GHz | | 22.6 | | dB | |
| | | RF = 2 GHz | | 23.4 | | | |
| | | RF = 4 GHz | | 25.2 | | | |
| | | RF = 6 GHz | | 19.9 | | | |
| | | RF = 8 GHz | | 11.2 | | | |
| Return Loss RF1, RF2 when selected (State 2 or 3) | RL4 | RF = 1 GHz | | 33.7 | | dB | |
| | | RF = 2 GHz | | 28.4 | | | |
| | | RF = 4 GHz | | 28.0 | | | |
| | | RF = 6 GHz | | 17.7 | | | |
| | | RF = 8 GHz | | 15.0 | | | |
| Input IP2 RF1 / RF2 (State 2 or 3) | IIP2 | $P_{IN} = +13\text{ dBm}$ per tone | RF = 1 GHz | | 116 | dBm | |
| | | | RF = 2 GHz | | 106 | | |
| | | | RF = 3 GHz | | 105 | | |
| Input IP3 RF1 / RF2 (State 2 or 3) | IIP3 | $P_{IN} = +13\text{ dBm}$ per tone | RF = 1 GHz | | 66 | dBm | |
| | | | RF = 2 GHz | | 66 | | |
| | | | RF = 3 GHz | | 65 | | |
| | | | RF = 4 GHz | | 65 | | |
| | | | RF = 6 GHz | | 52 | | |
| Input 1dB compression RF1 / RF2 (State 2 or 3) ³ | IP1dB | RF = 2 GHz | | 32 | | dBm | |
| Switching Time ⁴ | T_{SW} | 50% control to 90% RF | | 0.6 | | μs | |
| | | 50% control to 10% RF | | 0.5 | | | |
| | | 50% control to RF settled to within +/- 0.1 dB of I.L. value. | | 0.675 | | | |
| Maximum Switching Rate | SW_{RATE} | | | 25 | | kHz | |
| Maximum spurious level on any RF port ⁵ | $Spur_{MAX}$ | RF ports terminated into 50 Ω | | -137 | | dBm | |

Note 1– Items in min/max columns in ***bold italics*** are Guaranteed by Test.

Note 2– Items in min/max columns NOT in bold italics are Guaranteed by Design Characterization.

Note 3– The input 1dB compression point is a linearity figure of merit. Refer to Figure 1 above and Recommended Operating Conditions sections for the maximum RF input powers.

Note 4– $F_{RF} = 2\text{ GHz}$.

Note 5– Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.

Table 1 includes 3 states and provides the truth table for 2-pin control input.

Table 1 - Switch Control Truth Table for 3 states using 2 control pins; pin 16 and pin 17

| State | Control pin input | | RF1, RF2 input / output | |
|-------|-------------------|------------------|-------------------------|---------------|
| | CTL1 (Pin 17) | CTL2 (Pin 16) | RF1 to RF Com | RF2 to RF Com |
| 1 | Low | Low | OFF | OFF |
| 2 | Low | High | OFF | ON |
| 3 | High | Low | ON | OFF |
| 4 | High | High | N/A | N/A |

Table 2 includes 2 states and provides the truth table for 1-pin control input.

Table 2 - Switch Control Truth Table for 2 states using a single control pin 16

| State | Control pin input | | RF1, RF2 input / output | |
|-------|-------------------|------------------|-------------------------|---------------|
| | CTL1 (Pin 17) | CTL2 (Pin 16) | RF1 to RF Com | RF2 to RF Com |
| 2 | don't care | High | OFF | ON |
| 3 | don't care | Low | ON | OFF |

Table 3 provides the truth table for selecting the use of either 1 or 2 control pins.

Table 3 - Mode Control (pin 19) Truth table to use either 1 or 2 control pins

| Pin Control Mode | ModeCTL (Pin 19) |
|------------------------------|------------------|
| 2-pin control: CTL1 and CTL2 | GND |
| 1-pin control: CTL2 | VCC |

Notes:

1. When RF1 and RF2 ports are both open (State 1), all 3 RF ports are terminated to an internal 50 Ω termination resistor.
2. When RF1 or RF2 port is open (State 2 or State 3 OFF condition), the open port is connected to an internal 50 Ω termination resistor.
3. When RF1 or RF2 port is closed (State 2 or State 3 ON condition), the closed port is connected to the RF_COM port.

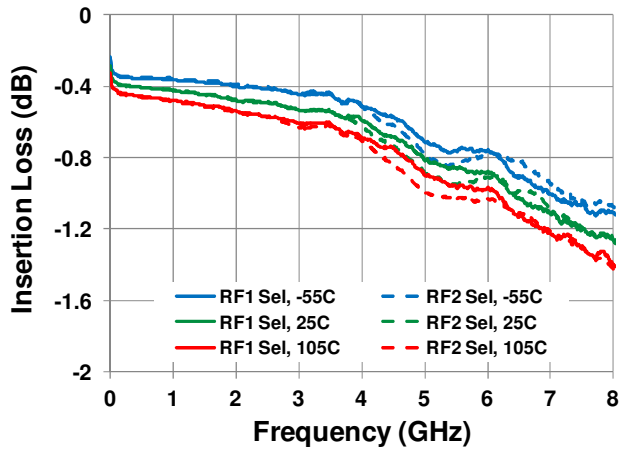
TYPICAL OPERATING CURVE CONDITIONS

Unless otherwise noted, the following conditions apply:

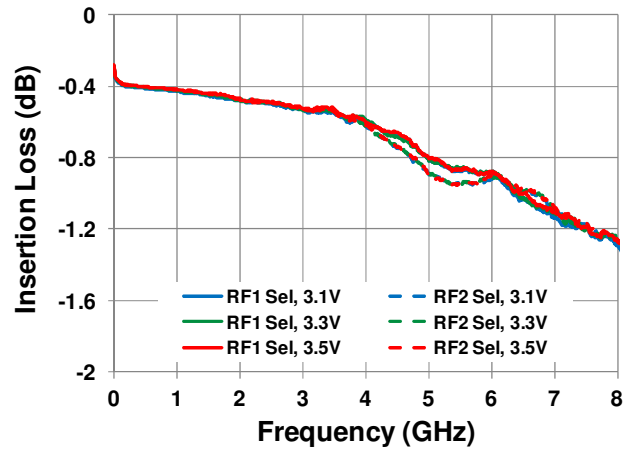
- EVKit loss de-embedded for only insertion loss plots.
- Vcc = 3.3 V
- $F_{RF} = 2$ GHz
- $T_{AMB} = 25$ °C
- Small signal parameters measured with $P_{IN} = 0$ dBm.
- Two tone tests $P_{IN} = +13$ dBm/tone with 50 MHz tone spacing.

TYPICAL OPERATING CONDITIONS (- 1 -)

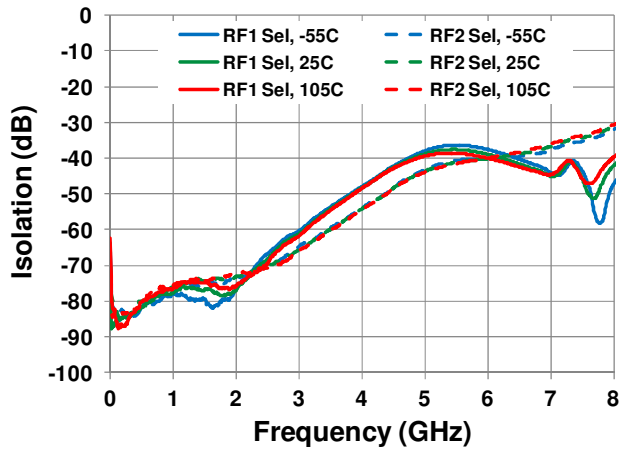
Insertion Loss vs. Temperature



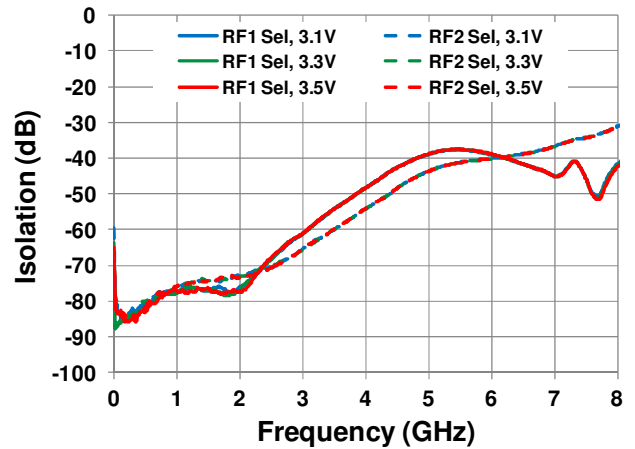
Insertion Loss vs. Voltage



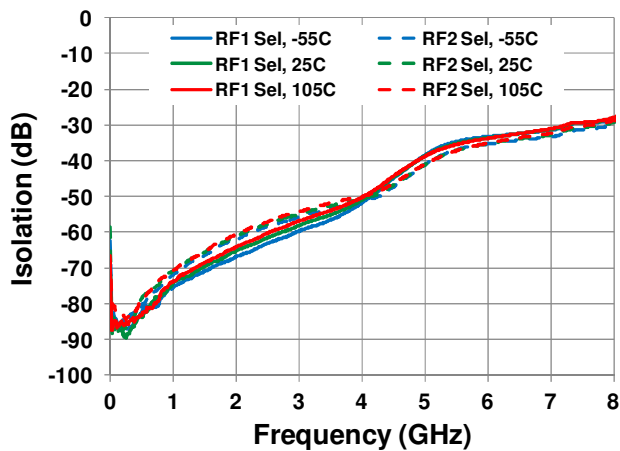
Isolation vs. Temp [RF_COM → RF1 / RF2]



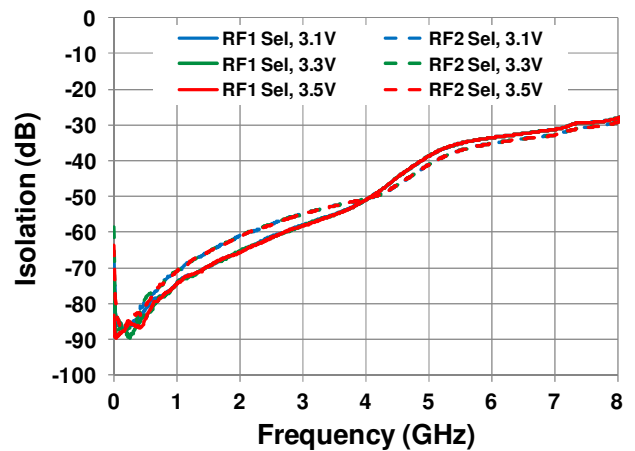
Isolation vs. Voltage [RF_COM → RF1 / RF2]



Isolation vs. Temp [RF1 → RF2, RF2 → RF1]

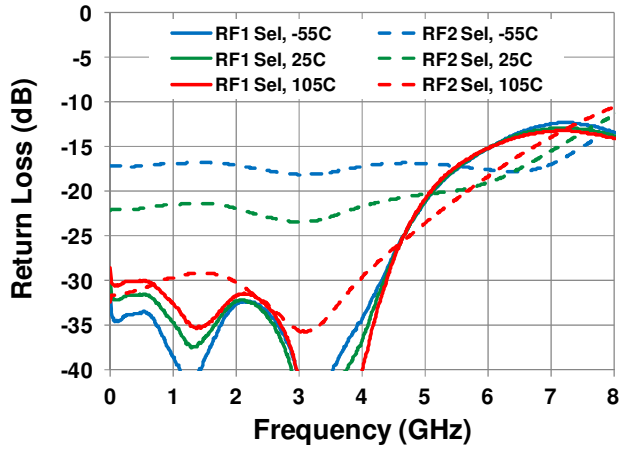


Isolation vs. Voltage [RF1 → RF2, RF2 → RF1]

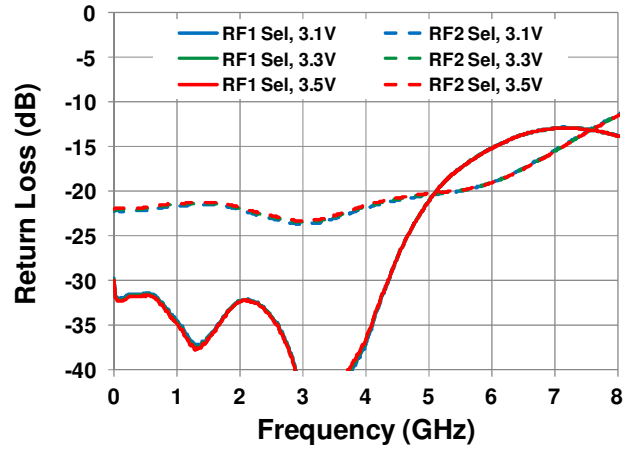


TYPICAL OPERATING CONDITIONS (- 2 -)

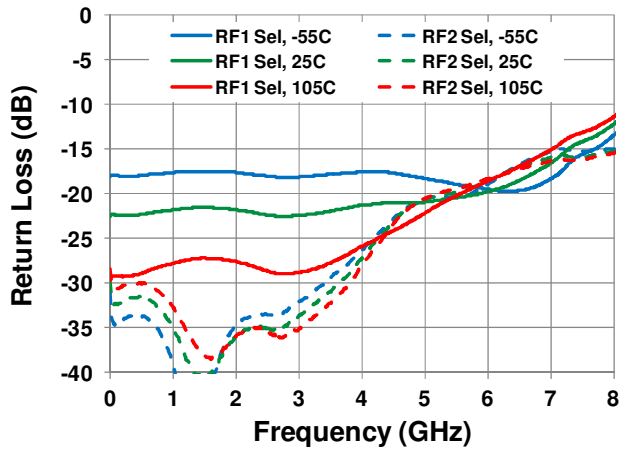
RF1 Return Loss vs. Temperature



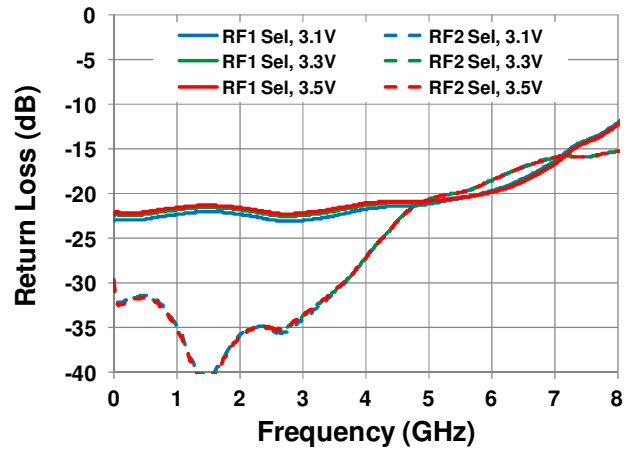
RF1 Return Loss vs. Voltage



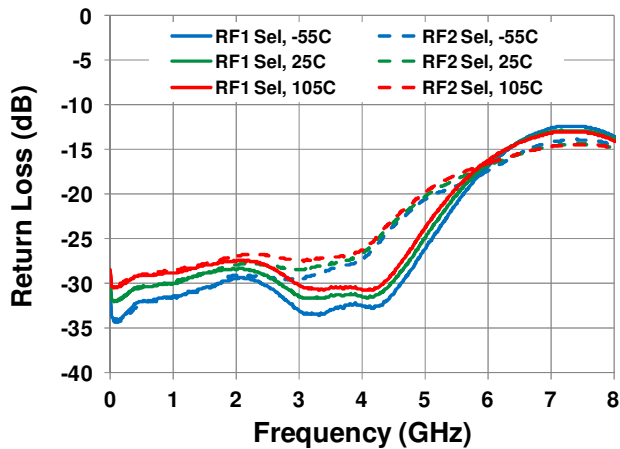
RF2 Return Loss vs. Temperature



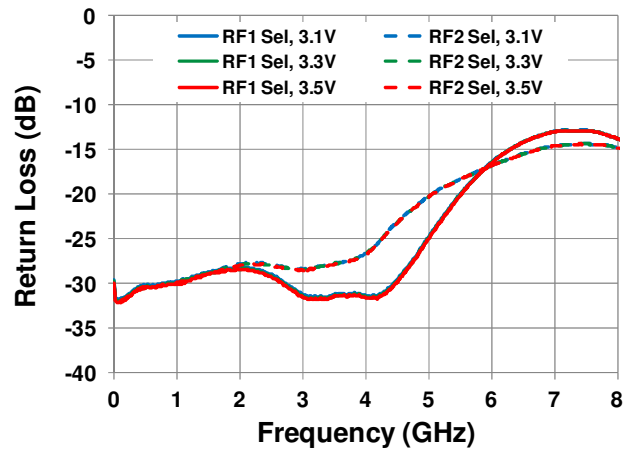
RF2 Return Loss vs. Voltage



RF_COM Return Loss vs. Temperature

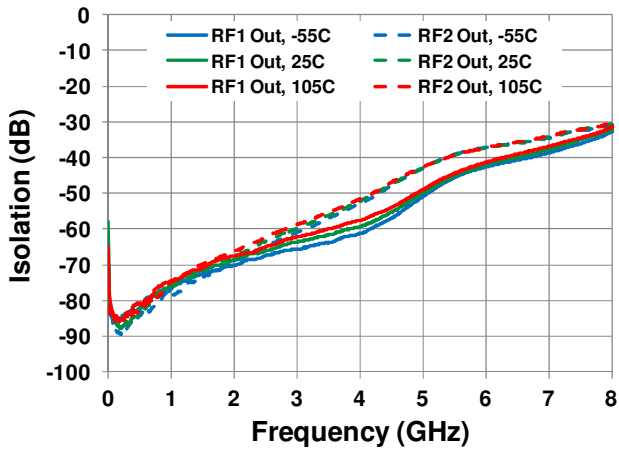


RF_COM Return Loss vs. Voltage

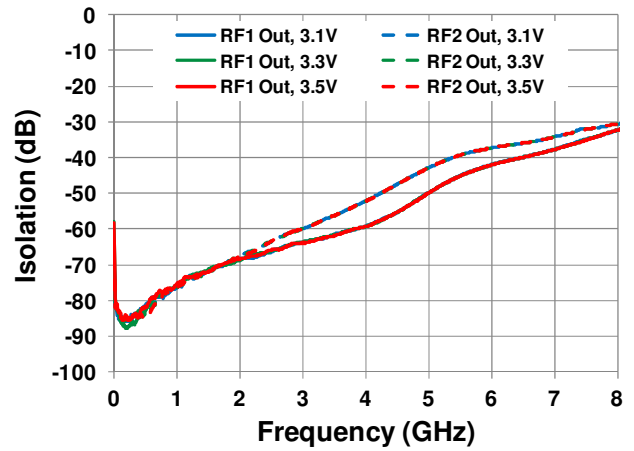


TYPICAL OPERATING CONDITIONS (- 3 -)

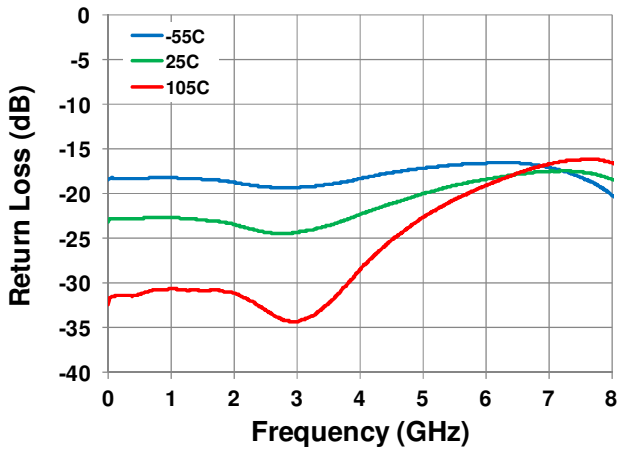
Isolation vs. Temp [All Off State, RF_COM Driven]



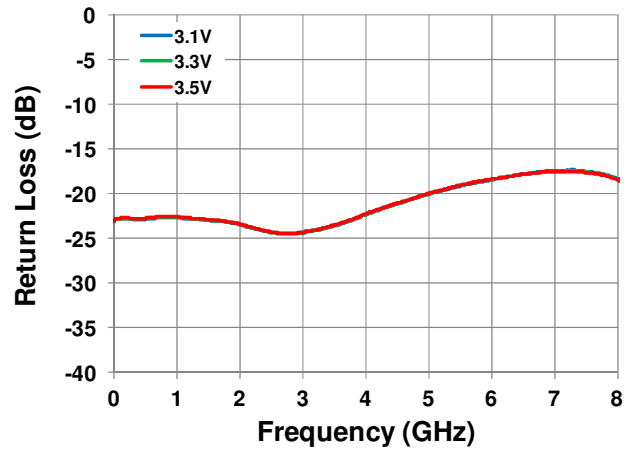
Isolation vs. Voltage [All Off State, RF_COM Driven]



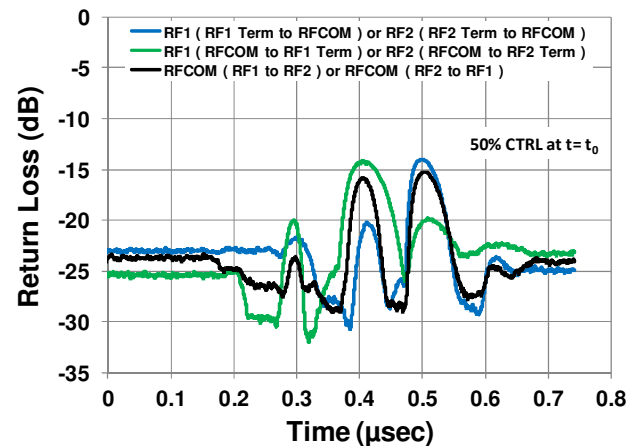
RF_COM Return Loss [All Off State] vs. Temp



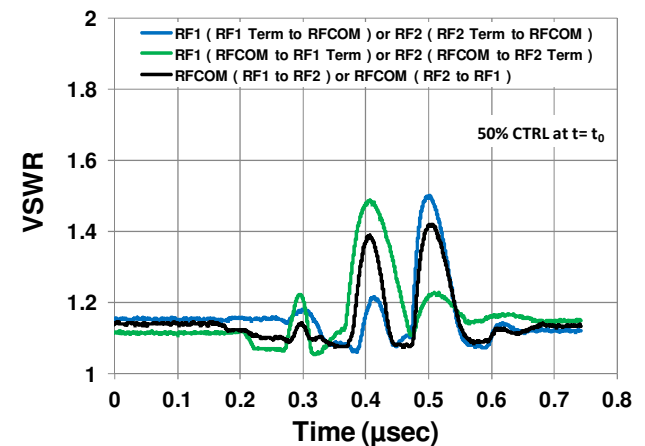
RF_COM Return Loss [All Off State] vs. Voltage



Return Loss (During Switching) vs. Time

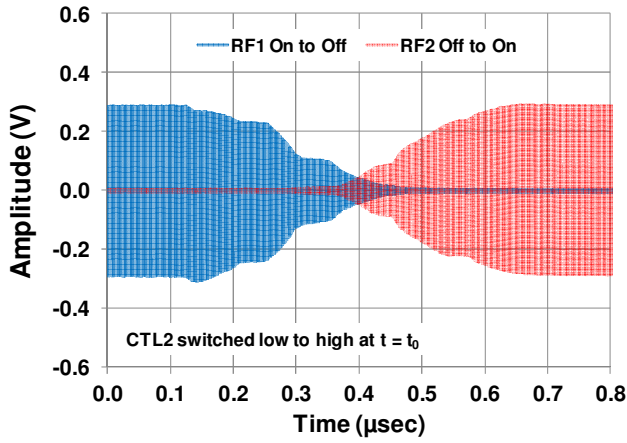


VSWR (During Switching) vs. Time

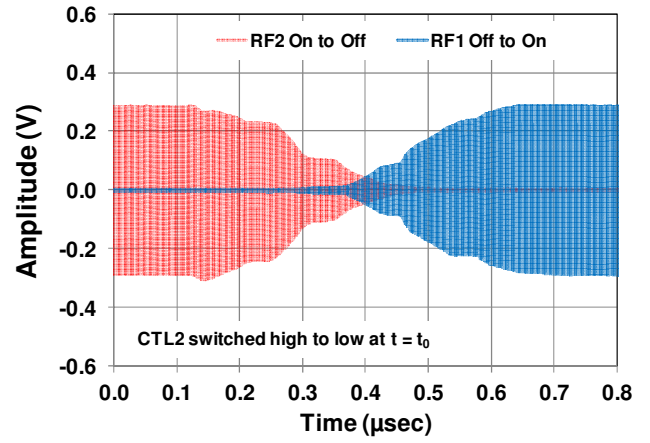


TYPICAL OPERATING CONDITIONS (- 4 -)

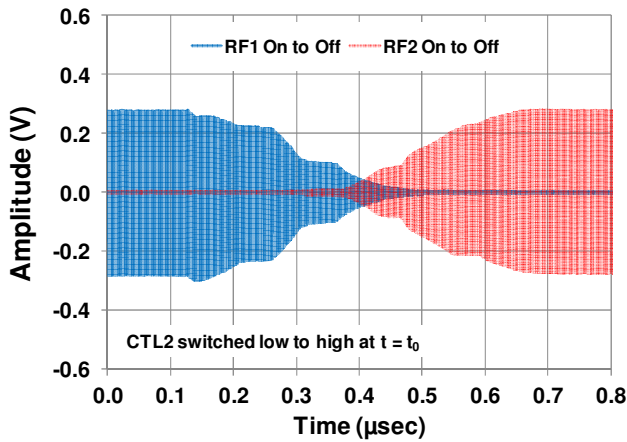
Switching Time $T_c=25C$ [RF_COM Driven, RF1 to RF2]



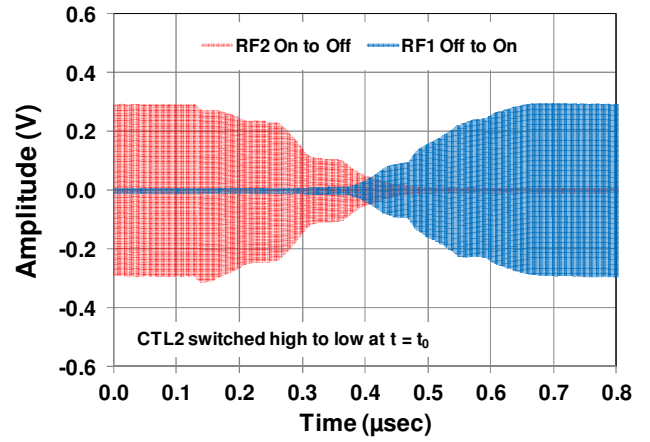
Switching Time $T_c=25C$ [RF_COM Driven, RF2 to RF1]



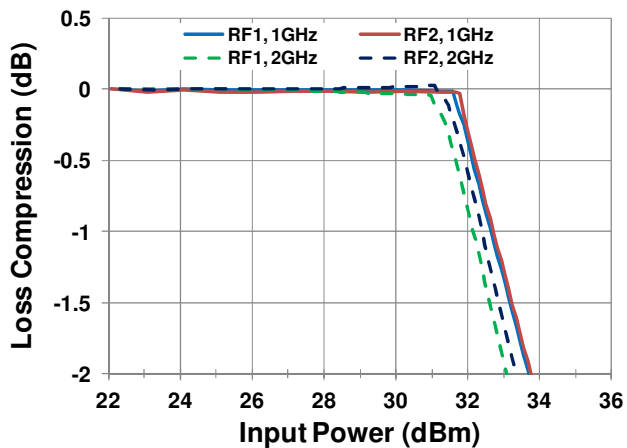
Switching Time $T_c=-40C$ [RF_COM Driven, RF1 to RF2]



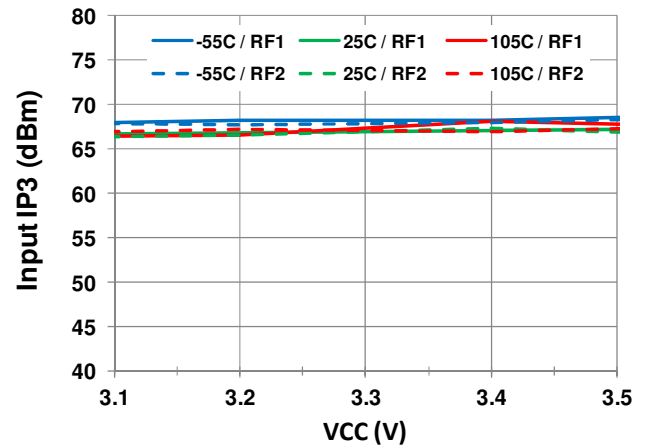
Switching Time $T_c=-40C$ [RF_COM Driven, RF2 to RF1]



Compression [1 GHz, 2 GHz, RF1, RF2]

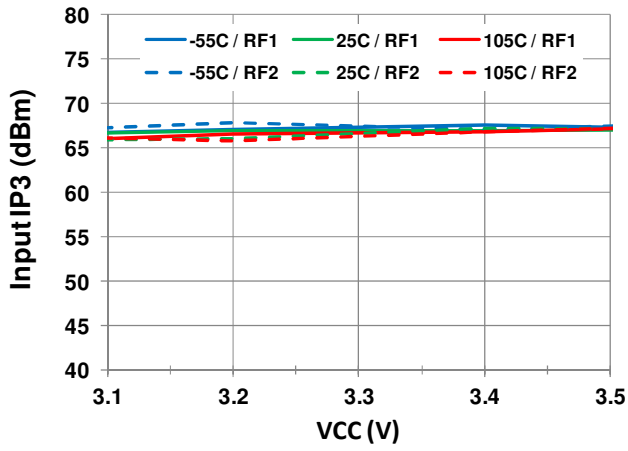


Input IP3 [1 GHz]

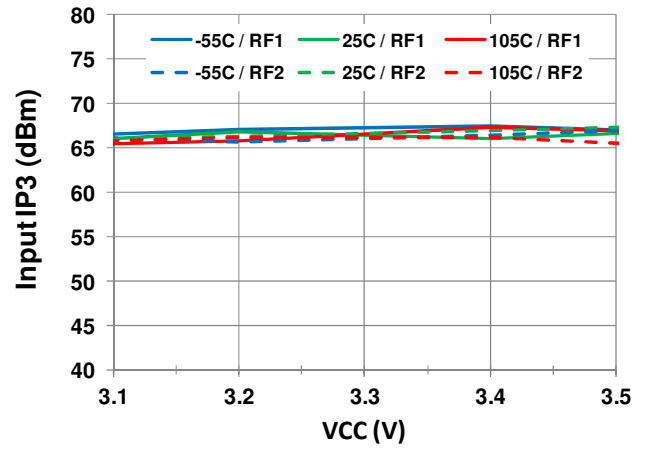


TYPICAL OPERATING CONDITIONS (- 5 -)

Input IP3 [2 GHz]

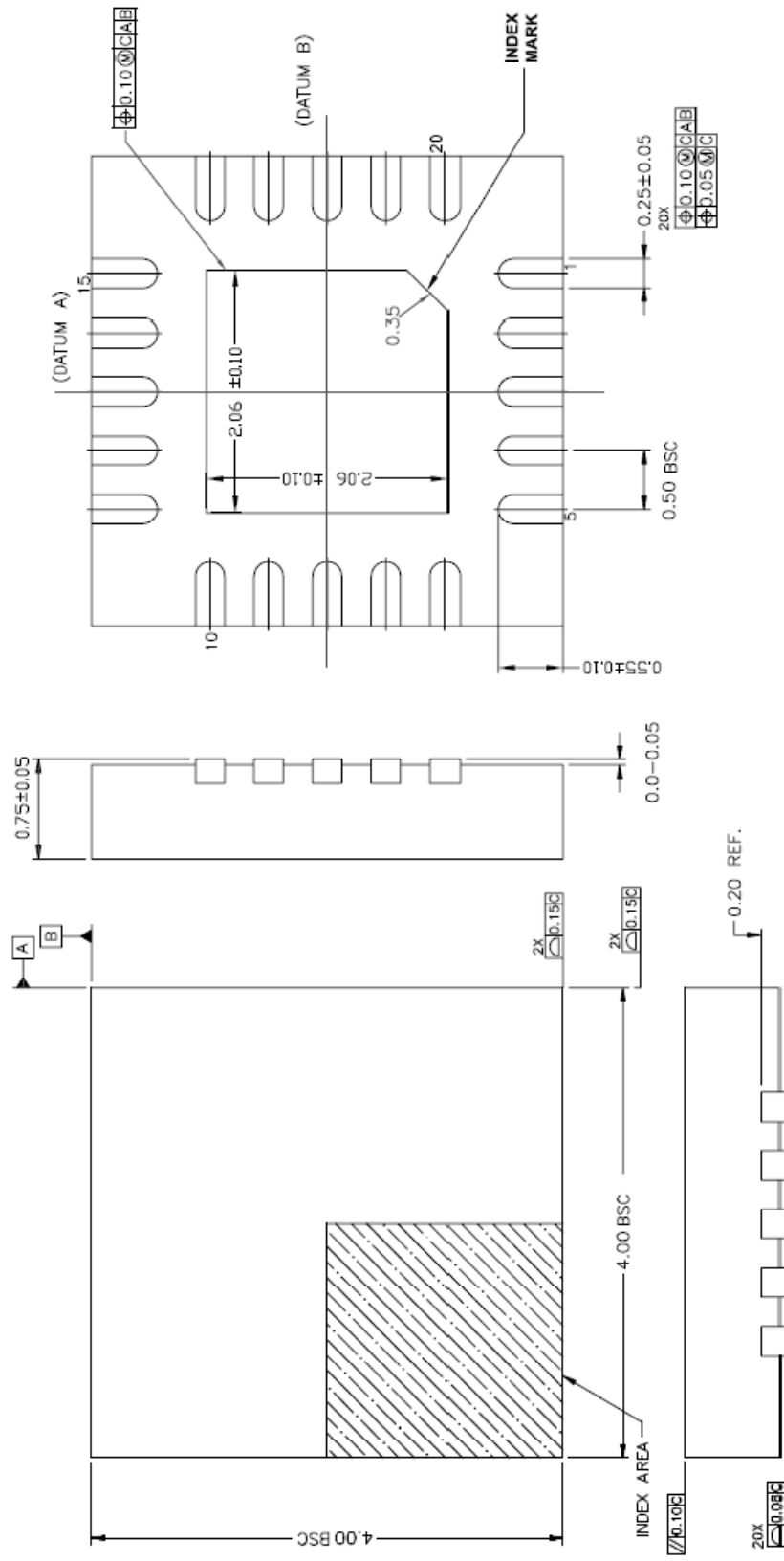


Input IP3 [3 GHz]



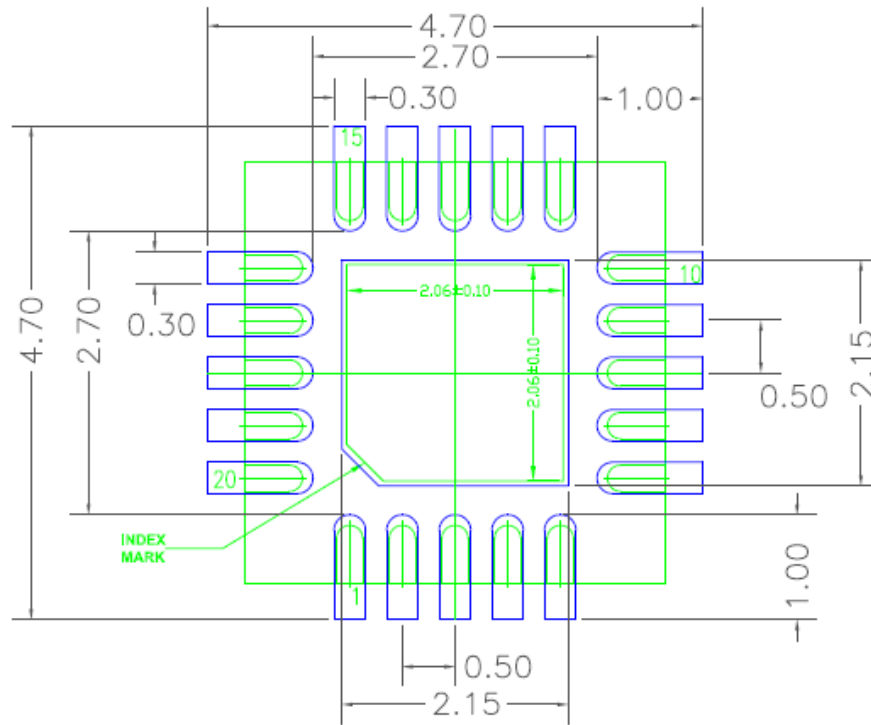
PACKAGE DRAWING

(4 mm x 4 mm 20-pin TQFN), NCG20



- NOTE :
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
COPLANARITY SHALL NOT EXCEED 0.08 mm.
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.
 4. REFER JEDEC MO-220.

LAND PATTERN DIMENSION

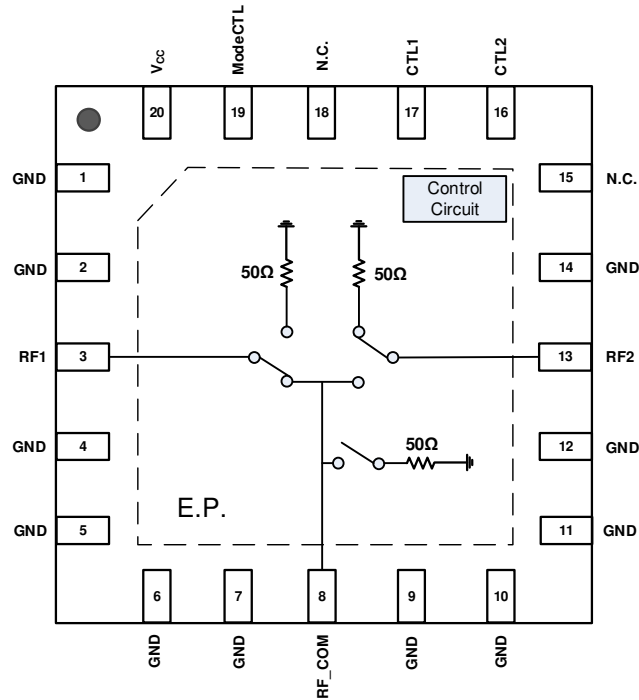


RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

PIN DIAGRAM



PIN DESCRIPTION

| Pin | Name | Function |
|-------------------------------------|---------|--|
| 1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14 | GND | Ground these pins. |
| 3 | RF1 | RF1 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 8 | RF_COM | RF Common Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 13 | RF2 | RF2 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used. |
| 15 | N.C. | No internal connection. This pin can be left open or connected to ground. |
| 16 | CTL2 | Control 2 – See Table 1 and Table 2 Switch Control Truth Tables for proper logic setting. |
| 17 | CTL1 | Control 1 – See Table 1 and Table 2 Switch Control Truth Tables for proper logic setting. |
| 18 | N.C. | No internal connection. |
| 19 | ModeCTL | Mode Control – See Table 3 Mode Control Truth Table. Apply VCC to select 1-pin control or GND for 2-pin control. |
| 20 | Vcc | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin. |
| 21 | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

APPLICATIONS INFORMATION

Default Start-up

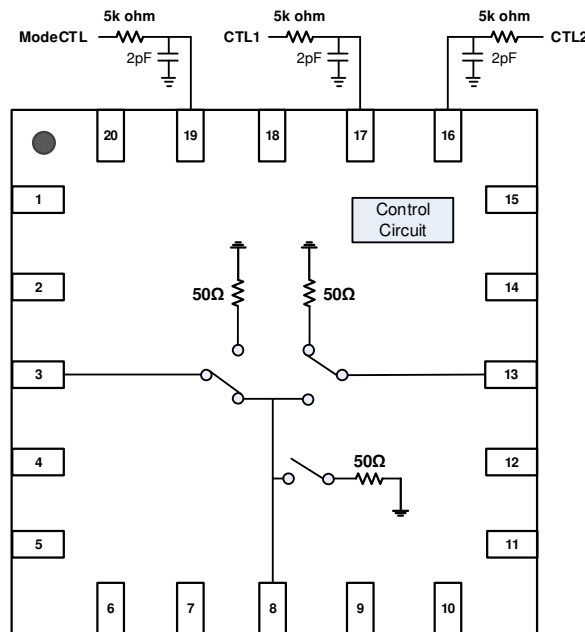
Control pins include no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH. Upon start-up, all control pins should be set to logic LOW (0) thereby enabling 2-pin switch control, opening both RF1 and RF2 paths, and setting logic control voltage to 3.3 V (see above tables for LOW logic states).

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 μ S. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

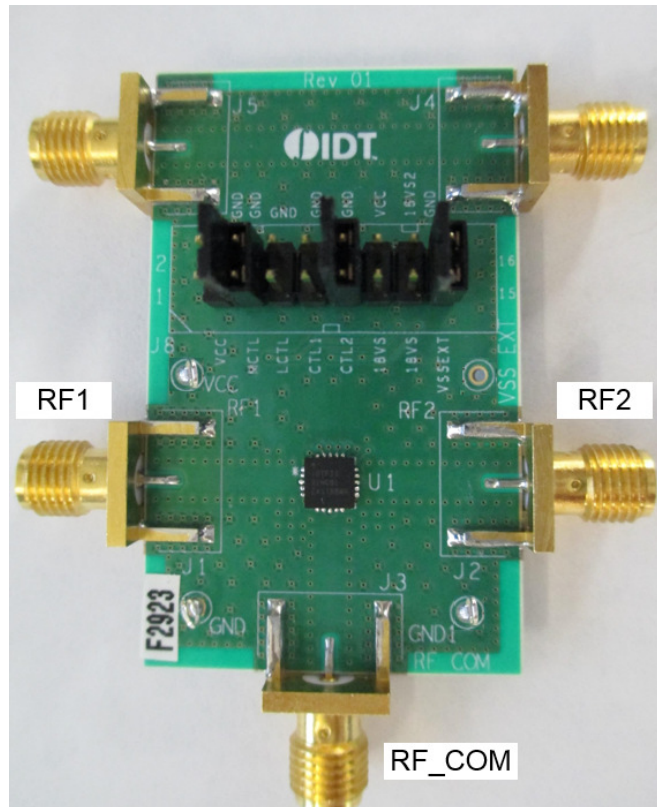
Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 16, 17, and 19 as shown below.

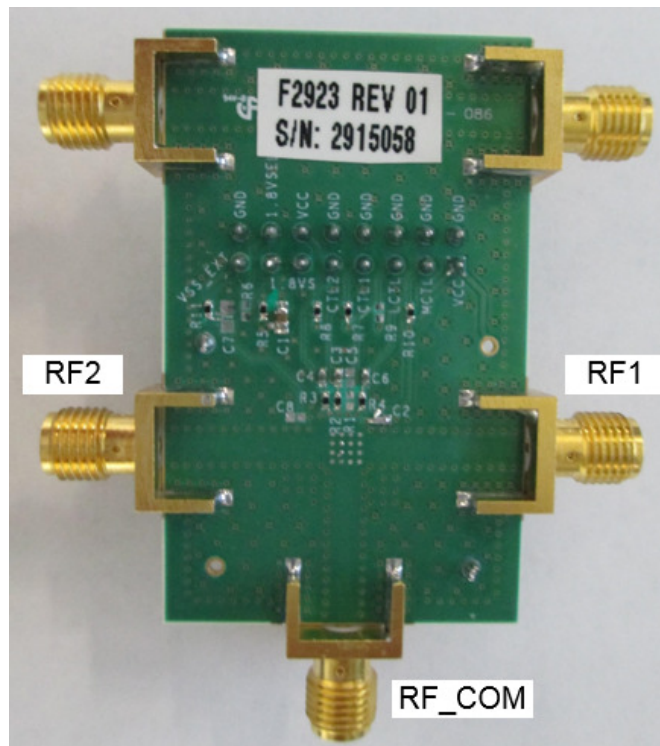


EVKIT PICTURE

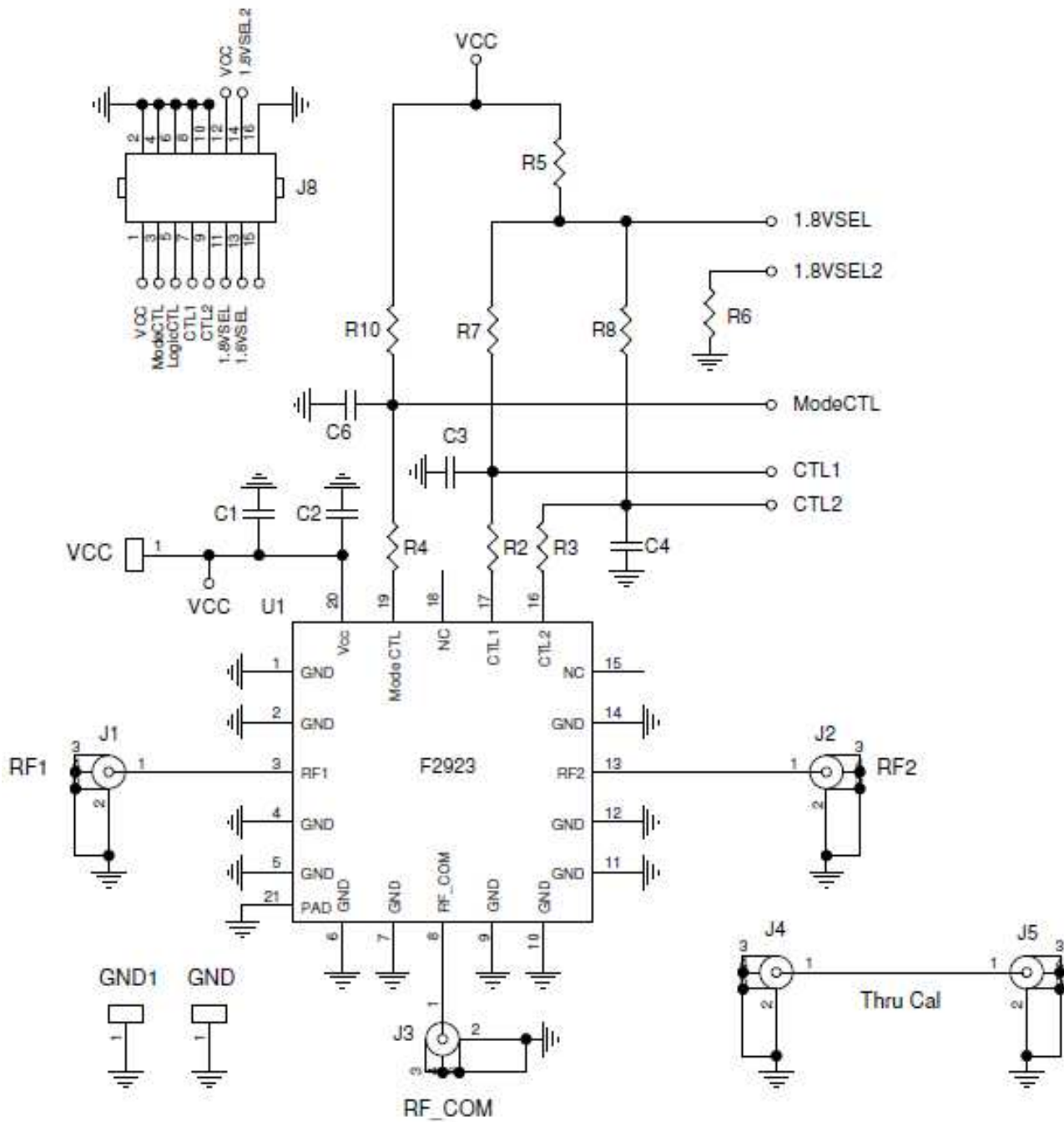
Top View



Bottom View



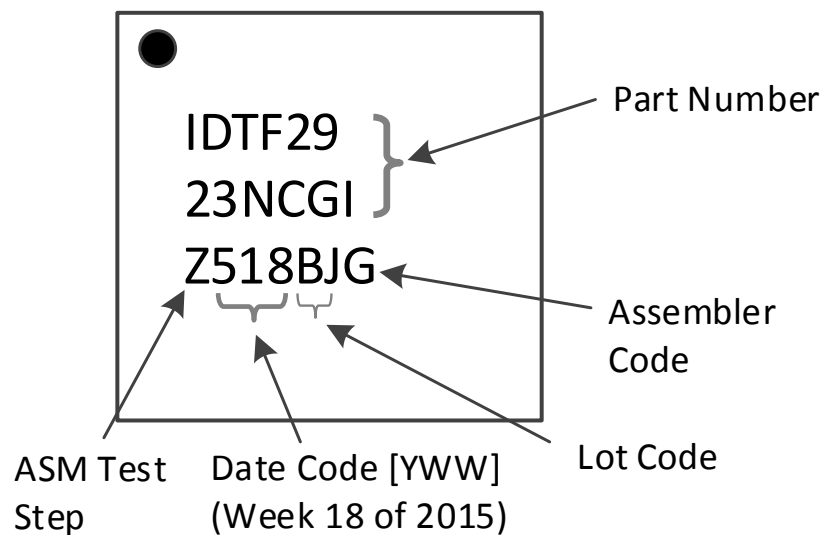
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM

| Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|----------------|-----|---|--------------------|----------------------|
| C1 | 1 | 100 nF ±10%, 50V, X7R Ceramic Capacitor (0603) | GRM188R71H104K | Murata |
| C2 | 1 | 1000 pF ±5%, 50V, C0G, Ceramic Capacitor (0402) | GRM1555C1H102J | Murata |
| C3, C4, C6 | 3 | 100 pF ±5%, 50V, C0G, Ceramic Capacitor (0402) | GRM1555C1H101J | Murata |
| R2, R3, R4, R5 | 4 | 0 Ω, 1/10W, Resistor (0402) | ERJ-2GE0R00X | Panasonic |
| R6 | 0 | Not Installed (0402) | | |
| R7, R8, R10 | 3 | 100k Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF1003X | Panasonic |
| J1-J5 | 5 | Edge Launch SMA (0.375 inch pitch ground tabs) | 142-0701-851 | Emerson Johnson |
| J8 | 1 | CONN HEADER VERT DBL 8 X 2 POS GOLD | 67997-116HLF | FCI |
| VCC, GND, GND1 | 3 | Test Point | 5021 | Keystone Electronics |
| U1 | 1 | SP2T Switch 4 mm x 4 mm QFN20-EP | F2923NCGI | IDT |
| | 1 | Printed Circuit Board | F2923 EVKIT Rev 01 | IDT |

TOP MARKINGS



EVKIT OPERATION

PCB RF Connectors

The F2923 EVkit is a thin multilayer board (0.032" total thickness) designed using Rogers' 4350 high RF performance material. Since this substrate is not as rigid as standard FR4, one must take care when making connections to the board to avoid physically damaging the board. It is suggested that the body of the connector be restrained while tightening the RF connectors so to not put stress on the PCB material.

External Supply Setup

Set up a VCC power supply in the voltage range of 3.1 V to 3.5 V and disable the power supply output.

Logic Control Setup

Using the EVKIT to manually set the Control Logic:

To setup the part for two pin logic control connect a 2-pin shunt from pin 3 (ModeCTL) to pin 4 (GND) on connector J8.

For one pin logic control leave J8 pin 3 open. An on-board pull-up resistor R10 will connect the ModeCTL pin to Vcc to provide the logic high for one pin control.

The PCB includes 2 pull-up resistors (R7, R8) to Vcc to provide a logic high for CTL1 and CTL2 respectively. Installing a 2-pin shunt from pin 7 (CTL1) to pin 8 (GND) of J8 will provide a logic low for manual control of the CTL1 pin. Placing a 2-pin shunt from pin 9 (CTL2) to pin 10 (GND) of J8 will result in a logic low for the CTL2 pin. See Tables 1, 2 and 3 for control details.

Resistor R6 along with the 1.8VSEL, 1.8VSEL2, and LogicCTL pins are not used on the F2923 EVKIT.

Using External Control Logic:

To setup the part for two pin logic control connect a 2-pin shunt from pin 3 (ModeCTL) to pin 4 (GND) on connector J8.

For one pin control leave pin 3 (ModeCTL) of J8 open. In this configuration the ModeCTL pin will be pulled up to Vcc on the PCB through resistor R10.

Turn on Procedure

Setup the supplies and Eval Board as noted in the **External Supply Setup** and **Logic Control Setup** sections above.

Connect the preset/ disabled VCC power supply to the VCC and GND loops on the PCB. If controlling CTL1 and CTL2 with external logic then set these to logic low.

Enable the VCC supply.

Set the desired logic setting using CTL1, and CTL2 Table 1 or Table 2 setting. Note that external control logic should not be applied without VCC being applied first.

For manual logic control the J8 connector CTL1 and CTL2 pins can be grounded to a neighboring ground for a logic low or left open for a logic high.

Turn off Procedure

If using external control logic for CTL1, CTL2 then set them to a logic low. Disable the VCC supply.

REVISION HISTORY SHEET

| Rev | Date | Page | Description of Change |
|------------|-------------|-------------|------------------------------|
| 0 | 2015-Nov-9 | | Initial Release |



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.idt.com

Tech Support
<http://www.idt.com/support/technical-support>

DISCLAIMER Integrated Device Technology, Inc. (IDT) reserves the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners.

Copyright ©2015. Integrated Device Technology, Inc. All rights reserved.