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November 2012

FAB2210 — Audio Subsystem with Class-G Headphone and 3.3W Mono Class-D Speaker with Dynamic Range Compression

Features

- High-Efficiency Stereo Class-G Headphone
 - 100 dB SNR Headphone Amplifier
 - Capacitor-Free Outputs for High-Frequency Response
- Mono Filterless Class-D Speaker Amplifier
 91% Efficiency for Extended Battery Runtime
 - DRC for Louder SPL and Speaker Protection
 - 3.3 W into 4 Ω at 5.0 V, THD+N < 10%
 - 1.27 W into 8 Ω at 4.2 V, THD+N < 10%
 - Low EMI Edge-Rate Controlled output
 - 97 dB Signal-to-Noise Ratio (SNR)
- Click and Pop Suppression
- Selectable Single-Ended or Differential Audio Inputs for High Common-Mode Rejection
- High Power Supply Rejection Ration (PSRR) Rejects 217 Hz GSM Noise
- Highly Configurable using I²C Control
- Low-Power, Software Standby Mode

Description

The FAB2210 combines a Class-G stereo capacitorfree headphone amplifier with a mono Class-D speaker amplifier into one IC package.

The headphone and speaker amplifiers incorporate Class-G and Class-D topologies, respectively, for low power dissipation, which extends battery runtime.

The Class-G headphone amplifier incorporates an integrated charge pump that generates a negative supply rail for ground-centered headphone outputs.

The Class-D amplifier includes programmable Dynamic Range Compression (DRC) that maximizes Sound Pressure Level (SPL) for maximum loudness, while protecting the speaker from damage.

The noise gate can automatically mute the speaker or headphone amplifiers to reduce noise when input signals are LOW.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAB2210UCX	-40°C to +85°C	20-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch	3000 Units on Tape & Reel

Typical Application Circuit







Pin Definitions

Pin Configuration

Pin #	Name	Туре	Description			
A2	SVDD	Power Input	ower supply for Class-D amplifier			
C1	SGND	Power Input	Class-D amplifier ground			
C2	DVDD	Power Input	Power supply for charge pump			
A3	DGND	Power Input	Headphone amplifier ground			
C3	HVDD	Power Output	narge pump output; positive power supply for headphone amplifier, input eamplifiers, and mixers			
C4	HVSS	Power Output	Charge pump output; negative mirror of HVDD			
B4	CP+	Power	Charge pump flying capacitor positive terminal			
A4	CP-	Power	Charge pump flying capacitor negative terminal			
E3	NC	No Connect	No connect can be tied to SGND for additional thermal dissipation			
D1	INA1	Input	Single-ended line level audio input A1 (or non-inverting differential input INA+)			
E1	INA2	Input	Single-ended line level audio input A2 (or inverting differential input INA-)			
D2	INB1	Input	Single-ended line level audio input B1 (or non-inverting differential input INB+)			
E2	INB2	Input	Single-ended line level audio input B2 (or inverting differential input INB-)			
E4	HOUTL	Output	Left headphone amplifier output			
D4	HOUTR	Output	Right headphone amplifier output			
D3	HSENSE	Input	Sense ground; connect to DGND close to shield terminal of headphone jack			
A1	SOUT+	Output	Positive Class-D amplifier output			
B1	SOUT-	Output	Negative Class-D amplifier output			
B3	SCL	Input	I ² C clock input			
B2	SDA	Bidirectional	² C data I/O			

FAB2210 — Audio Subsystem with Class-G Headphone and 3.3W Mono Class-D Speaker with Dynamic Range Compression

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltages are referenced to GND.

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Voltage on SVDD Pin	-0.3	6.0	V
V _{DVDD}	Voltage on DVDD Pin	-0.3	3.2	V
V _{SVDD}	Voltage on SVDD + DVDD Pins		8	V
V _{IN}	Voltage on INA1, INA2, INB1, INB2 Pins	V _{HVSS} -0.3	V_{DVDD} +0.3 or 2.1 ⁽¹⁾	V
V _{HOUT}	Voltage on HOUTL, HOUTR Pins	V _{HVSS} -0.3	V _{DVDD} +0.3	V
V _{SENSE}	Voltage on HSENSE Pin	-0.3	0.3	V
VD	Voltage on SDA, SCL Pins	-0.3	V _{SVDD}	V
V _{SOUT}	Voltage on SOUT+, SOUT- Pins	-0.3	V _{SVDD} +0.3	V
R _{HP}	Headphone Impedance	12.8		Ω

Note:

1. Whichever is less.

Reliability Information

Symbol	Parameter	Min.	Тур.	Max.	Unit
TJ	Junction Temperature			150	°C
T _{STG}	Storage Temperature Range	-65		150	°C
TL	Lead Temperature (Soldering, 10 Seconds)			300	°C
θ _{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		66		°C/W
TSD	Thermal Shutdown Threshold		150		°C
T _{HYS}	Thermal Shutdown Hysteresis		15		°C

Electrostatic Discharge Protection

Symbol	Parameter	Min.	Unit
ESD	Human Body Model; JESD22-A114 Level 2; Compatible with IEC61340-3-1: 2002 Level 2 or ESD-STM5.1-2001 Level 2 or MIL-STD-883E 3015.7 Level 2	±2.00	kV
	Charged Device Model; JESD22-C101 Level III Compatible with IEC61340-3-3 level C4 or ESD-STM5.3.1-1999 Level C4	±1.25	kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Тур.	Max.	Unit
T _A	Operating Temperature Range	-40		85	°C
V _{SVDD}	Speaker Supply Voltage Range ^(2,3)	2.80	3.60	5.25	V
V _{DVDD}	Headphone Supply Voltage Range ^(2,3)	1.6	1.8	2.8	V

Notes:

2. V_{SVDD} must be greater than or equal to V_{DVDD} at all times.

3. V_{SVDD} and V_{DVDD} slew rates must be less than 1 V / μ s.

Electrical Characteristics

Unless otherwise noted: audio BW=22 Hz to 20 kHz, f_{IN} =1 kHz, DIFA=1, DIFB=0, HP_AMIX=0, HP_BMIX=1, SP_AMIX=1, SP_BMIX=0, unused inputs are AC grounded, DRC is off, preamplifier gains=0 dB, headphone volume=0 dB, headphone amplifier gain=0 dB, speaker volume=0 dB, SP_GAIN=00, edge-rate control is on, spread spectrum is on, HP_NG_RAT=100, SP_NG_RAT=001, SRST=0, SDA and SCL pull-up voltage=DV_{DD}, $Z_{SPK} = 8 \ \Omega + 33 \ \mu$ H, $R_{HP} = 32 \ \Omega$, HP_HIZ=0, SV_{DD} = 3.6 V, DV_{DD} = 1.8 V, and T_A =25°C.

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
I _{STBY}	Standby Current (SRST=1)	SVDD + DVDD		2		μA
t _{on}	Turn-On Time	Time from Standby to Full Speaker and Headphone Operation, ZCD and Ramps Disabled		1.6		ms
		Preamplifier Gain=12.0 dB		7.7		
	Input Resistance	Preamplifier Gain=6.0 dB		12.8		
		Preamplifier Gain=4.5 dB		14.3		
Р		Preamplifier Gain=3.0 dB		15.9		kO
RIN		Preamplifier Gain=1.5 dB		17.5		K12
		Preamplifier Gain=0.0 dB		19.2		
		Preamplifier Gain=-1.5 dB		20.8		
		Preamplifier Gain=-3.0 dB		22.4		· · · ·
	Maximum Input Signal Swing	Preamplifier Gain=0 dB		V _{DVDD}		V _{pk-pk}
	Single-Ended Input)	Preamplifier Gain=12 dB		V _{DVDD} ÷ 4		V _{pk-pk}

Electrical Characteristics (Speaker Amplifier)

Unless otherwise noted: audio BW=22 Hz to 20 kHz, f_{IN} =1 kHz, DIFA=1, DIFB=0, HP_AMIX=0, HP_BMIX=0, SP_AMIX=1, SP_BMIX=0, unused inputs are AC grounded, DRC is off, preamplifier gains=0 dB, headphone volume=0 dB, headphone amplifier gain=0 dB, speaker volume=0 dB, SP_GAIN=00, edge-rate control is on, spread spectrum is on, HP_NG_RAT=000, SP_NG_RAT=000, SRST=0, SDA and SCL pull-up voltage=DV_{DD}, Z_{SPK} = 8 Ω + 33 µH, R_{HP} =32 Ω , HP_HIZ=0, SV_{DD}=3.6 V, DV_{DD}=1.8 V, and T_A=25°C.

Symbol	Parameter	Condition	Condition		Тур.	Max.	Unit
	Current Consumption		SV _{DD}		2.7		•
Icc		SP_NG_RAT=001	DV _{DD}		1.6		mΑ
Vos	Output Offset Voltage	Volume=0dB			±0.4		mV
		200 mV _{ek ek} Ripple on	f=217 Hz		70		
		SV _{DD} ,	f=1 kHz		70		
	Power-Supply Rejection	SP_NG_RAT=001	f=20 kHz		63		٩D
PORK	Ratio		f=217 Hz		74		uБ
		200 mV _{pk-pk} Ripple on	f=1 kHz		70		
			f=20 kHz		44		
		THD+N < 10%, SV _{DD} =5 Z _{SPK} =4 Ω + 33 μH	5.0 V,		3.3		
		THD+N < 1%, SV _{DD} =5. Z _{SPK} =4 Ω + 33 μH	0 V,		2.6		
Pout	Output Power	THD+N < 10%, SV _{DD} =4		1.27		W	
		THD+N < 1%, SV _{DD} =4.		1.00			
		THD+N < 10%, SV _{DD} =3		0.92	2		
		THD+N < 1%, SV _{DD} =3.		0.73			
	Total Harmonic Distortion	P _{OUT} =0.7 W, SV _{DD} =4.2 V			0.04		0/
THD+N	Plus Noise	P _{OUT} =0.7 W, SV _{DD} =3.6 V			0.17		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
	Oine al ta Naisa Datia	A-wt, P _{OUT} =700 mW			97		9
SINK	Signal-to-Noise Ratio	A-wt, P _{OUT} =700 mW, SV _{DD} =4.2 V			97		aв
		Spread Spectrum			300		ku -
	Class-D Frequency	Fixed Frequency	Fixed Frequency		300		KITZ
	Efficiency	P _{OUT} =720 mW			91		%
	DC Detect Voltage	Absolute Value, Measu Differentially Across SC SOUT-	red)UT+ and		1.5		V _{pk}
		DCERR_TIME=10			15		
t _{DCERR}	DC Detect Time	DCERR_TIME=01			5		ms
		DCERR_TIME=00			2		
		Amp. Off, SP_HIZ=0, f	< 40 kHz		2		$\sum_{i=1}^{n}$
		OTP_ERR=1, f < 40 kH	łz		2		
	Single-Ended Output	DC_ERR=1, f < 40 kHz	2		2		kΩ
		Amp. Off, SP_HIZ=1, f	< 40 kHz		35		1
		OCP_ERR=1, f < 40 kH		2			

Electrical Characteristics (Headphone Amplifiers)

Unless otherwise noted: audio BW=22 Hz to 20 kHz, f_{IN} =1 kHz, DIFA=1, DIFB=0, HP_AMIX=0, HP_BMIX=1, SP_AMIX=0, SP_BMIX=0, unused inputs are AC grounded, DRC is off, preamplifier gains=0 dB, headphone volume=0 dB, headphone amplifier gain=0 dB, speaker volume=0 dB, SP_GAIN=00, edge-rate control is on, spread spectrum is on, HP_NG_RAT=000, SP_NG_RAT=000, SRST=0, SDA and SCL pull-up voltage=DV_DD, $Z_{SPK} = 8 \ \Omega + 33 \ \mu$ H, R_{HP} =32 Ω , HP_HIZ=0, SV_{DD}=3.6 V, DV_DD=1.8 V, and T_A =25°C.

Symbol	Parameter		Conditi	on	Min.	Тур.	Max.	Unit
-	Current Consumption		400	SVDD		0.8		
ICC		HP_NG_RAT=100 DVDD		DVDD		1.9		mA
V _{OS}	Output Offset Voltage	Volume=Mute				±0.1		mV
		200 mV _{ok-ok} Rij	pole on	f=217 Hz		93		
		SVDD,		f=1 kHz		94		dB
DCDD	Power-Supply Rejection	HP_NG_RAT=	=100	f=20 kHz		97		
FORK	Ratio			f=217 Hz		93		
		SVDD	ppie on	f=1 kHz		93		dB
				f=20 kHz		97		
		THD+N < 0.1%	6			27		
Pout	Output Power	THD+N < 1%, Gain=6dB	Headpho	ne Amplifier		29		mW
		THD+N < 1%, Gain=6 dB, SV	Headpho / _{DD} =4.2 V	ne Amplifier		29		
		P _{OUT} =10 mW				0.01		
THD+N	Total Harmonic	P _{OUT} =10 mW, SV _{DD} =4.2 V			0.01		%	
	Distortion r las relise	P _{OUT} =20 mW			0.01			
	Signal-to-Noise Ratio	A-wt.	P _{OUT} =10	mW, SV _{DD} = 3.6 V		102.5		
		HP_NG_RAT	P_NG_RAT POUT=10 mW, SVDD=4.2 V			102.5		
SND		=100	P _{OUT} =20	mW		105.5		dB
SINIX		A-wt, HP_NG_RAT	P _{OUT} =10	mW, SV _{DD} = 3.6 V		97.0		uв
			P _{OUT} =10	mW, SV _{DD} =4.2 V		97.0		
		=000	P _{OUT} =20 mW			100.0		
CL	Capacitive Drive					100		pF
		P _{OUT} =10 mW,	f=100 Hz			-96		
		P _{OUT} =20 mW,	f=100 Hz			-95		
		P _{OUT} =10 mW,	f=1 kHz			-93		
Xtak	Crosstalk	P _{OUT} =20 mW,	f=1 kHz			-92		40
Λίακ	Crosstait	P _{OUT} =10 mW,	f=10 kHz			-79		ub
		P _{OUT} =20 mW, f=10 kHz			-79			
		Headphone to Speaker, P _{OUT} =10 mWx2		P _{OUT} =10 mWx2		-91		\sim J
		Speaker to He	adphone,	P _{OUT} =700 mW		-106		
		Amp. Off, HP	HIZ=0			130		Ω
	Output Impedance	OTP_ERR=1				170		Ω
		Amplifier Off, HP_HIZ=1			15		kΩ	

I²C DC Electrical Characteristics

Unless otherwise noted, SV_{DD}=2.8 V to 5.25 V, DV_{DD}=1.6 V to 2.8 V, T_A=-40 ^{\circ}C to $85^{\circ}C$.

Symbol	Parameter		Fast Mode (400 kHz)				
Symbol			Max.	Unit			
VIL	Low-Level Input Voltage	-0.3	0.6	V			
V _{IH}	High-Level Input Voltage	1.3		V			
V _{OL}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain or Open-Collector)	0	0.4	V			
I _{IH}	High-Level Input Current of Each I/O Pin, Input Voltage=V _{SVDD}	-1	1	μA			
IIL	Low-Level Input Current of Each I/O Pin, Input Voltage=0V	-1	1	μA			

I²C AC Electrical Characteristics

Unless otherwise noted, SV_{DD} =2.8 V to 5.25 V, DV_{DD} =1.6 V to 2.8 V, T_A =-40°C to 85°C.

Symbol	Deveneter		Fast Mode (400 kHz)			
Symbol	Parameter	Min.	Max.	Unit		
f _{SCL}	SCL Clock Frequency	0	400	kHz		
t _{HD;STA}	Hold Time (Repeated) START Condition	0.6		μs		
t _{LOW}	Low Period of SCL Clock	1.3		μs		
t _{HIGH}	High Period of SCL Clock	0.6		μs		
t _{su;sta}	Set-up Time for Repeated START Condition	0.6		μs		
t _{HD;DAT}	Data Hold Time	0	0.9	μs		
t _{su;dat}	Data Set-up Time ⁽⁴⁾	100		ns		
tr	Rise Time of SDA and SCL Signals ⁽⁵⁾	20+0.1C _b	300	ns		
t _f	Fall Time of SDA and SCL Signals ⁽⁵⁾	20+0.1Cb	300	ns		
t _{su;sto}	Set-up Time for STOP Condition	0.6		μs		
t _{BUF}	Bus-Free Time between STOP and START Conditions	1.3		μs		
t _{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns		

Notes:

4. A Fast-Mode I²C Bus® device can be used in a Standard-Mode I²C Bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the Serial Data (SDA) line t_{r_max} + t_{SU;DAT}=1000 + 250=1250 ns (according to the Standard-Mode I²C Bus specification) before the SCL line is released.

 C_b equals the total capacitance of one bus line in pf. If mixed with High-Speed Mode devices, faster fall times are allowed according to the I²C specification.



Typical Performance Characteristics

System

Unless otherwise noted: audio BW=22 Hz to 20 kHz, f_{IN}=1 kHz, DIFA=1, DIFB=0, HP AMIX=0, HP BMIX=1, SP AMIX=1, SP BMIX=0, unused inputs are AC grounded, DRC is off, preamplifier gains=0 dB, headphone volume=0 dB, headphone amplifier gain=0 dB, speaker volume=0 dB, SP GAIN=00, edge-rate control is on, spread spectrum is on, HP NG RAT=100, SP NG RAT=001, SRST=0, SDA and SCL pull-up voltage=DV_{DD}, Z_{SPK} = 8 Ω + 33 µH, R_{HP}=32 $\overline{\Omega}$, HP HIZ=0, SV_{DD}=3.6 V, DV_{DD}=1.8 V, and T_A=25°C.



Typical Performance Characteristics

Speaker Amplifier

Unless otherwise noted: audio BW=22 Hz to 20 kHz, f_{IN} =1 kHz, DIFA=1, DIFB=0, HP_AMIX=0, HP_BMIX=0, SP_AMIX=1, SP_BMIX=0, unused inputs are AC grounded, DRC is off, preamplifier gains=0 dB, headphone volume=0 dB, headphone amplifier gain=0 dB, speaker volume=0 dB, SP_GAIN=00, edge-rate control is on, spread spectrum is on, HP_NG_RAT=000, SP_NG_RAT=000, SRST=0, SDA and SCL pull-up voltage=DV_{DD}, Z_{SPK} =8 Ω + 33 µH, R_{HP} =32 Ω , HP_HIZ=0, SV_{DD}=3.6 V, DV_{DD}=1.8 V, and T_{A} =25°C.



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Headphone Amplifiers

Unless otherwise noted: audio BW=22 Hz to 20 kHz, f_{IN} =1 kHz, DIFA=1, DIFB=0, HP_AMIX=0, HP_BMIX=1, SP_AMIX=0, SP_BMIX=0, unused inputs are AC grounded, DRC is off, preamplifier gains=0 dB, headphone volume=0 dB, headphone amplifier gain=0 dB, speaker volume=0 dB, SP_GAIN=00, edge-rate control is on, spread spectrum is on, HP_NG_RAT=000, SP_NG_RAT=000, SRST=0, SDA and SCL pull-up voltage=DV_{DD}, Z_{SPK} = 8 Ω + 33 µH, R_{HP} =32 Ω , HP_HIZ=0, SV_{DD}=3.6 V, DV_{DD}=1.8 V, and T_{A} =25°C.





Detailed Description

Shutdown Modes

Standby

When the SRST bit is set to 1, the FAB2210 enters a low-power Standby Mode.

While SRST=1, I^2C communications are available and I^2C values are reset to default values. Any values written to the I^2C registers (except SRST) while in Standby Mode are ignored and default values is preserved.

To achieve low supply current during Standby Mode, all inputs must be DC. Audio inputs must be AC grounded. V_{SVDD} and V_{DVDD} must be within recommended operating conditions. I²C pins must be grounded or pulled HIGH with no toggling. If AC is presented to the inputs during Standby Mode, standby current may increase slightly, but there are no other negative effects.

Thermal Shutdown Protection (TSP)

If the junction temperature of the device exceeds the thermal shutdown threshold of $150^{\circ}C$ (see the Electrical *Characteristics table*), the device protects itself by turning off the amplifiers. The I²C port remains functional and the OTP_ERR bit is set to 1. Other bits retain their values and are not reset. See the Electrical *Characteristics table for output impedances*. The amplifiers remain off until the junction temperature falls below the thermal shutdown recovery point and SRST is cycled or power is cycled.

Over-Current Protection (OCP)

If the speaker amplifier's output current limit of 1.3 A_{PEAK} is exceeded (see the Electrical Characteristics table), the amplifier turns off. During current-limit shutdown, the I²C port remains functional and the OCP_ERR bit is set to 1. Other bits retain their values and are not reset. The speaker amplifier remains off and the OCP_ERR remains HIGH until SRST is cycled or power is cycled.

DC Output Protection

If the magnitude of the speaker amplifier output voltage across SOUT+ and SOUT- exceeds the DC detect voltage of 1.5 V_{pk} for more than t_{DCERR} (see the *Electrical Characteristics table*), the speaker amplifier turns off. This protects the loudspeaker from damage due to DC signals. Low-frequency audio input signals may trigger unintentional DC output shutdown. Set the input DC coupling capacitor value small enough to avoid a DC output shutdown caused by a low-frequency audio signal. For the default t_{DCERR} setting of 2 ms, the input DC-coupling capacitor value must be 0.1 μ F or lower.

During DC output shutdown, the I^2C port remains functional and the DC_ERR bit is set to 1. Other bits retain their values and are not reset. The speaker amplifier remains off and the DC_ERR bit remains HIGH until SRST is cycled or power is cycled.

Signal Path

Audio signals pass from the input pins through a preamplifier, a mixer, a volume control, and finally through an amplifier. The preamplifiers can be set to -3 dB to 18 dB of gain. The headphone and speaker paths have volume controls that range from -64 dB to 0dB. The headphone amplifier has gain settings of 0 dB, 1.5 dB, 3 dB, and 6 dB. The speaker amplifier has gain settings of 16 dB, 20 dB, and 24 dB.

A variety of combinations of the input signals can be routed from the preamplifiers to the headphone and speaker volume blocks. Routing is controlled by the HP_AMIX, HP_BMIX, SP_AMIX, SP_BMIX, DIFA, DIFB, and MONO bits.

For example, to connect the left headphone amplifier channel to INA1 and the right headphone amplifier channel to INA2, set HP_AMIX to 1. HP_BMIX, DIFA, and MONO should be set to 0.

To configure INB1 and INB2 as a differential input and route the signal to the speaker amplifier, set DIFB and SP_BMIX to 1. SP_AMIX should be set to 0.

When HP_AMIX and HP_BMIX are both 0, the headphone amplifier is off. When SP_AMIX and SP BMIX are both 0, the speaker amplifier is off.

Unused audio input pins must be grounded either directly or through a DC-blocking capacitor.

To prevent internal clipping in the headphone amplifier path, internal signal amplitudes from the preamplifier outputs to the headphone amplifier input should not exceed a peak-to-peak voltage equivalent to V_{DVDD} - 0.2 V. If HP_MONO = 1, the peak-to-peak voltage can be as high as (V_{DVDD} * 2) - 0.2 V. Extra caution should be taken if mixing signals together.

To prevent internal clipping in the speaker amplifier path, internal signal amplitudes from the preamplifier outputs to the speaker amplifier input should not exceed a peak-to-peak voltage equivalent to V_{DVDD} - 0.2 V. Extra caution should be taken if mixing signals together.

Charge Pump

The FAB2210 includes an inverting charge pump that generates HVDD and HVSS (the headphone amplifier power supplies) from the DVDD power supply input. The HVSS rail is a negative mirror of HVDD and allows the headphone amplifier to be ground referenced. The ground-referenced biasing scheme allows the headphone amplifier outputs to be biased at ground while operating from a single external supply. This eliminates the need for the large, expensive, DC-coupling capacitors between the headphone amplifier output and load that are required on traditional, single-supply, $V_{DD}/2$, biased headphone amplifiers.

The negative HVSS rail allows the input preamplifiers to be ground referenced. Input DC-blocking capacitors are still required at INA1, INA2, INB1, and INB2 if the audio source driving the input preamplifiers is biased above ground. The input DC-blocking capacitors are not required if the audio source driving the input preamplifiers is also ground referenced and does not present any DC offset to the FAB2210.

Class-G Operation

Compared with a traditional Class-AB amplifier, the FAB2210's Class-G architecture reduces power consumption and extends battery life during headphone playback. The power supply rails (HVDD and HVSS) of the Class-G headphone amplifier adapt to the level of audio signal present at the output. The adaptive nature of the power supply rails ensures that energy is not wasted during quiet passages of music or when the volume of the headphone path is reduced.

During stereo headphone playback, when the headphone output amplitude is below the V_{TH} threshold level of 250 mV_{pk} (typical); the charge pump efficiently divides V_{DVDD} so that V_{HVSS} = -V_{DVDD}/2 and V_{HVDD} = V_{DVDD}/2. When the headphone output amplitude exceeds 250 mV_{pk} (typical), the charge pump generates higher magnitude rails, where V_{HVSS}=-V_{DVDD} and V_{HVDD} = V_{DVDD} to allow for higher output amplitudes. Due to the high crest factor of music and speech, a significant portion of the audio content is below the V_{TH} threshold, even at typical volume level settings for headphone playback. When operating at the lower magnitude rails, less power is dissipated within the headphone amplifier.

The transition from the lower magnitude rails to the higher magnitude rails occurs fast enough to prevent audible artifacts during headphone playback. The transition from the higher magnitude rails to the lower magnitude rails occurs 15 ms (typical) from the last threshold crossing (low to high) and only after the headphone output amplitude has stayed below the threshold level. The 15 ms (typical) hysteresis prevents the headphone amplifier power rails from bouncing between high and low rails when the audio signal approaches the threshold level.

Due to the flexible input to output routing capabilities of the FAB2210, additional logic added to the Class-G audio-level-detection circuit ensures that enough headroom is available to avoid saturating the audio input signals at the INA1, INA2, INB1, and INB2 preamplifiers. This is especially useful in cases where both the Class-D amplifier path and/or mono headphone path are selected for playback.



Figure 24. Class-G Headphone Amplifier Power Supply Rail Operation

Headphone Amplifier High-Impedance Mode

The FAB2210 headphone outputs are placed in a High-Impedance Mode by setting the HP_HIZ bit to 1 and turning off the headphone amplifier. This can be useful if the system's headphone jack is shared with other devices. For proper high-impedance operation, SRST must be set to 0 and the headphone amplifier must be off (see HP_MONO, HPAMIX, and HP_BMIX register definitions). Voltages on the HOUTL and HOUTR pins must not exceed DVDD and must not be below -DVDD.

Headphone Volume Ramp and Zero Crossing Detection

The HP_SVOFF and HP_ZCSOFF bits control the headphone volume when HP_ATT is changed.

HP_SVOFF and HP_ZCSOFF do not slow down turn-on or turn-off when using the HP_AMIX, HP_BMIX, or SRST bits. Thermal shutdown conditions are not slowed by HP_SVOFF or HP_ZCSOFF.

HP_SVOFF	HP_ZCSOFF	Behavior when HP_ATT is Changed
1	1	Volume changes immediately.
1	0	For each channel, wait until a zero crossing occurs in the input before changing volume. If a zero crossing does not occur within 200 μ s, volume is forced to the new setting.
0	1	Volume is ramped to the new setting at a rate of 200 μ s per step.
0	0	Volume is changed by one step when a zero crossing occurs. If a zero crossing does not occur within 200 μ s, a step is forced. Only the first zero crossing within 200 μ s triggers a volume change; volume does not change again until the next 200 μ s.

Table 1. Headphone Volume-Change Behavior

Headphone Amplifier Noise Gate

The headphone noise gate automatically reduces the headphone volume when its input amplitudes are low to reduce noise during inactivity. (This function is more useful for speech than music.) The amplitude is measured after input preamplifiers, but before the headphone volume control. The headphone noise gate's threshold level is set by the HP_NG_RAT register. The amplitudes of both channels must be less than the noise gate threshold for the hold-time determined by the NG_ATRT register.

The amount of volume reduction is set by the HP_NG_ATT register. The speed at which the volume is reduced is determined by the attack time setting in the NG_ATRT register. When the volume is reduced by the noise gate, the HP_ATT register's readback value remains unchanged. An internal register keeps track of the actual volume setting.

If either headphone channel's amplitude goes above the headphone noise gate threshold, headphone volume is raised back to the HP_ATT value at a rate determined by the release time setting in the NG_ATRT register. If HP_MONO=1, only left channel amplitude is monitored.

To avoid unpredictable behavior, noise gate settings should not change while the headphone amplifier is on.

Class-D Speaker Amplifier

The FAB2210 utilizes a "Filterless" modulation scheme to achieve 92% efficiency, extending battery life and reducing component count. The pulse-width modulated, differential outputs of the Class-D amplifier switch at 300 kHz. When an audio input signal is not present, the Class-D outputs switch in-phase at 50% duty cycle, minimizing idle current and saving power.

Programmable Spread Spectrum Modulation

Spread spectrum modulation is employed to reduce EMI generated at the Class-D amplifier outputs. Spread spectrum modulates the Class-D amplifier's switching frequency by a programmable percentage centered around the base switching frequency of 300 kHz, dispersing the spectral energy of the switching waveform over a wider band. This significantly reduces the amount of concentrated spectral energy at multiples of the switching frequency that fixed-frequency Class-D amplifiers emit. Spread spectrum modulation eliminates the need for output filters, as long as the distance from the Class-D amplifier outputs to the speaker transducer is kept short.

Edge Rate Control (ERC)

The Edge Rate Control (ERC) circuit minimizes EMI generated by the high-current switching waveform of the Class-D amplifier output. One of the main contributors to EMI generated by Class-D amplifiers is the high-frequency energy produced by rapid (large dV/dt) transitions at the edges of the switching waveform. The ERC circuit suppresses the high-frequency component of the switching waveform by extending the rise and fall times of the output FET transitions, without compromising efficiency and THD+N performance. Rise and fall times are set to approximately 20ns per transition at all power levels.

Dynamic Range Compression (DRC)

The speaker amplifier's DRC can be used to limit output amplitude and reduce clipping even as the supply voltage varies. The DRC allows high gain settings while preventing distortion and speaker damage. This results in louder speaker playback without increasing the maximum peak amplitude of the speaker signal path.

To avoid unpredictable behavior, DRC settings should not be changed while the speaker amplifier is on.

Figure 25 shows the speaker amplifier's target output amplitude with respect to the DRC's input amplitude when programmed at various Class-D output gain settings. The DRC's input amplitude is measured after the speaker volume control, but before the speaker amplifier block.

The DRC has three regions of operation: linear, compression, and limiter. When the output amplitude is initially low, the DRC operates in the linear region and does not apply any gain changes to the signal. The volume control remains fixed at the level defined in SP_ATT. When the output amplitude has increased above the dynamic range compression threshold, the DRC reduces the gain of SP_ATT, thereby applying compression to the output signal.

The compression region is defined by the compression ratio and the dynamic range compression threshold. The dynamic range compression threshold is set by the DPLT register. The dynamic range compression threshold is set 8 dB below the DPLT threshold level. The DRC applies a 2:1 compression ratio for output signals between the dynamic range compression threshold and limiter threshold. In the compression region; for every 2 dB rise of input amplitude, the target output amplitude only rises by 1 dB. This continues until the output amplitude has increased above the DRC limiter threshold.

The limiter region is defined by the DALC and DPLT registers. In the limiter region, the target output amplitude does not increase with the input amplitude. The DPLT register sets an output voltage limit independent of the battery voltage. This is useful for speaker protection. The DALC register defines an output voltage limit that is a percentage of the battery voltage. Since the battery voltage sets the maximum output amplitude, the DALC register is used as a distortion limiter by setting the allowed clipping amount.

The DRC limiter threshold is defined as the lower of the two limiter voltages set by the DPLT and DALC settings. For example, in Figure 27; if DPLT=111, DALC=001, and SV_{DD}=4.5 V_{pk}, the DRC limit is $3.79 V_{pk}$ as defined by DPLT. However, if SV_{DD} falls to 3.0 V, the DRC limiter threshold falls to $2.7 V_{pk}$, as defined by DALC.

The speed at which gain is changed is regulated by the attack and release settings in the DATRT register. Figure 28 shows DRC attack and release behavior.

DRC attack occurs when the DRC determines that, for given input amplitude, the actual output amplitude is higher than the target output amplitude and attack speed (defined in the DATRT register) is not to be exceeded. When these criteria are met, volume is reduced by one step.

DRC release occurs when the DRC determines that, for a given input amplitude, the actual output amplitude is lower than the target output amplitude and release speed (defined in the DATRT register) is not be exceeded. When these criteria are met, volume is increased by one step.

When the volume is changed by the DRC, the SP_ATT register readback value remains unchanged. An internal register keeps track of the actual volume setting.

When 2:1 compression is enabled, the overall gain of the speaker amplifier path is increased by 6 dB, as shown in Figure 26.



Figure 25. Dynamic Range Compression Response vs. Class-D Output Gain Settings







Speaker Amplifier Noise Gate

The speaker noise gate automatically mutes the speaker amplifier when its input amplitude is below a predetermined noise gate threshold to reduce noise during inactivity. (This function is more useful for speech than music.) The amplitude is measured after the speaker volume control, but before the speaker amplifier block. The speaker noise gate's threshold level is set by the SP_NG_RAT register. The amplitude must be less than the noise gate threshold for the hold time determined by the NG_ATRT register.

The speed at which the volume is reduced is determined by the attack time setting in the NG_ATRT register. When the volume is reduced by the noise gate, the SP_ATT register's readback value remains unchanged. An internal register keeps track of the actual volume setting.

If the speaker channel's amplitude goes above the speaker noise gate threshold, the speaker volume is raised back to the SP_ATT value at a rate determined by the release time setting in the NG_ATRT register.

To avoid unpredictable behavior, noise gate settings should not be changed while the speaker amplifier is on.

SP_SVOFF	SP_ZCSOFF	Behavior when SP_ATT is Changed
1	1	Volume changes immediately.
1	0	Wait until a zero crossing occurs in the input before changing volume. If a zero crossing does not occur within 200 μ s, volume is forced to the new setting.
0	1	Volume is ramped to the new setting at a rate of 200 µs per step.
0	0	Volume is changed by one step when a zero crossing occurs. If a zero crossing does not occur within 200 μ s, a step is forced. Only the first zero crossing within 200 μ s triggers a volume change; volume does not change again until the next 200 μ s.

Table 2. Speaker Volume Change Behavior

Speaker Volume Ramp and Zero-Crossing Detection

The SP_SVOFF and SP_ZCSOFF I²C bits control the speaker volume when SP_ATT is changed.

SP_SVOFF and SP_ZCSOFF do not slow down turn-on or turn-off when using the SP_AMIX, SP_BMIX, or SRST bits. Thermal, over-current, and DC offset shutdown conditions are not slowed by SP_SVOFF and SP_ZCSOFF.

SP_SVOFF and SP_ZCSOFF have no effect on DRC and noise gate timing. DRC and noise gate timing have no effect on speaker volume ramp and zero-crossing detection. In the event of a conflict between these systems, the lowest volume setting is chosen.

I²C Control

Writing to and reading from registers is accomplished via the l^2C interface. The l^2C protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the "master" device. The master device generates the SCL signal, which is the clock signal for all other devices on the bus. All other devices on the bus are called "slave" devices. The FAB2210 is a slave device. Both the master and slave devices can send and receive data on the bus.

During I^2C operations, one data bit is transmitted per clock cycle. All I^2C operations follow a repeating nine clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device.

Note that there are no unused clock cycles during any operation; therefore, there must be no breaks in the stream of data and ACKs/NACKs during data transfers.

For most operations, l^2C protocol requires the SDA line to remain stable (unmoving) whenever SCL is HIGH; i.e. transitions on the SDA line can only occur when SCL is LOW. The exceptions to this rule are when the master device issues a START or STOP condition. The slave device cannot issue a START or STOP condition.

START Condition: This condition occurs when the SDA line transitions from HIGH to LOW while SCL is HIGH. The master device uses this condition to indicate that a data transfer is about to begin.

STOP Condition: This condition occurs when the SDA line transitions from LOW to HIGH while SCL is HIGH. The master device uses this condition to signal the end of a data transfer.

Acknowledge and Not Acknowledge: When data is transferred to the slave device, the slave device sends an acknowledge (ACK) after receiving every byte of data. The receiving device sends an ACK by pulling SDA LOW for one clock cycle.

When the master device is reading data from the slave device, the master sends an ACK after receiving every byte of data. Following the last byte, a master device sends a "not acknowledge" (NACK) instead of an ACK, followed by a STOP condition. A NACK is indicated by leaving SDA HIGH during the clock after the last byte.

Slave Address

Each slave device on the bus must have a unique address so the master can identify which device is sending or receiving data. The FAB2210 slave address is 1001101X binary where "X" is the read/write bit. Master write operations are indicated when X=0. Master read operations are indicated when X=1.

Writing to and Reading from the FAB2210

All read and write operations must begin with a START condition generated by the master. After the START condition, the master must immediately send a slave address (7 bits), followed by a read/write bit. If the slave address matches the address of the FAB2210, the FAB2210 sends an ACK after receiving the read/write bit by pulling the SDA line LOW for one clock cycle.

Setting the Pointer

For all operations, the pointer stored in the command register must be pointing to the register that is going to be written or read. To change the pointer value in the command register, the read/write bit following the address must be 0. This indicates that the master writes new information into the command register.

After the FAB2210 sends an ACK in response to receiving the address and read/write bit, the master must transmit an appropriate 8-bit pointer value, as explained in the I^2C Registers section. The FAB2210 sends an ACK after receiving the new pointer data.

The pointer set operation is illustrated in Figure 31 and Figure 32. Any time a pointer set is performed, it must be immediately followed by a read or write operation. The command register retains the current pointer value between operations; therefore, once a register is indicated, subsequent read operations do not require a pointer set cycle. Write operations always require the pointer be reset.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the read/write bit (following the slave address) to 1. After sending an ACK, the FAB2210 begins transmitting data during the following clock cycle. The master should respond with a NACK, followed by a STOP condition (see Figure 29).

The master can read multiple bytes by responding to the data with an ACK instead of a NACK and continuing to send SCL pulses, as shown in Figure 30. The FAB2210 increments the pointer by one and sends the data from the next register. The master indicates the last data byte by responding with a NACK, followed by a STOP.

To read from a register other than the one currently indicated by the command register, a pointer to the desired register must be set. Immediately following the pointer set, the master must perform a REPEAT START condition *(see Figure 32)*, which indicates to the FAB2210 that a new operation is about to occur. If the REPEAT START condition does not occur, the FAB2210 assumes that a write is taking place and the selected register is overwritten by the upcoming data on the data bus. After the START condition, the master must again send the device address and read/write bit. This time, the read/write bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraphs for reading from a preset pointer location.

Writing

All writes must be preceded by a pointer set, even if the pointer is already pointing to the desired register.

Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the Serial Data (SDA) line for one clock cycle to allow the FAB2210 to acknowledge receiving the byte. The write operation should be terminated by a STOP condition from the master (see Figure 31).

As with reading, the master can write multiple bytes by continuing to send data. The FAB2210 increments the pointer by one and accepts data for the next register. The master indicates the last data byte by issuing a STOP condition.



Register Map

The I²C slave address is 1001101X, where X=0 for write operations and X=1 for read operations.

ADDR	B7	B6	B5	B4		B3	B2	B1	B0	
0x15	R	EVISION_ID	[2:0]	RSVD	F	RSVD	DCERR_1	TIME[1:0]	0	
0x1A	0	SOFTVOL		RSVD						
0x1B	0				DRO	CMIN[6:0]			
0x1D		MCSSMT[2:	0]	SSMT[2:0] ERC				0		
0x80	SRST	0	0	0		0	1	0	0	
0x81	DRC_M	ODE[1:0]	DATE	RT[1:0]		NG_A	TRT[1:0]	0	MODESEL	
0x82		DPLT[2:0]		н			:0]	HP_NG_ATT[1:0]		
0x83	0	0	NCLIP	S	SP_NG_RAT[2:0] SP_				_ATT[1:0]	
0x84		V	A[3:0]				VB[3:0]		
0x85	DIFA	DIFB	0	0	HP	SVOFF	HP_HIZ	SP_SVOFF	SP_HIZ	
0x86	0				SP	ATT[6:0]			
0x87	0				HP	ATT[6:0]			
0x88	OCP_ERR	OTP_ERR	DC_ERR	HP_MONO	HP	_AMIX	HP_BMIX	SP_AMIX	SP_BMIX	
0xC0	0	37	DALC[2:0]		HP_GAIN[1:0]			SP_G	_GAIN[1:0]	
0xC1	0	0	0	0		0	HP_ZCSOFF	0	SP_ZCSOFF	

Notes:

Bits labeled "0" are reserved. Only zeros should be written to these bits. 6.

7.

Bits labeled "1" are reserved. Only ones should be written to these bits. Bits labeled "RSVD" are for testing only. Writing to these bits has no effect. When read, they may return any value. 8. Bits and addresses not listed in the register map are for testing only. These bits should never be written. When 9.

read, they may return any value.

Register Descriptions

ADDR	B7	B6	B5	B4	B3	B2	B1	B0
0x15	REVISION_ID[2:0]			RSVD	RSVD	DCERR_	TIME[1:0]	0
Default	0	1	1			0	0	0

REVISION_ID[2:0]

(read only)

011 = Silicon revision 3.

DCERR_TIME[1:0]

DC error time control

11 = DC output detection disabled

10 = 15 ms

01 = 5 ms

00 = 2 ms

ADDR	B7	B6	B5	B4	B3	B2	B1	B0	
0x1A	0	SOFTVOL	RSVD						
Default	0	0							

SOFTVOL

Sets volume ramp speed; sets noise gate release speed when MODESEL=1.

1 = 2 ms / step

0 = 200 µs / step

ADDR	B7	B6	B5	B4	В3	B2	B1	B0		
0x1B	0		DRCMIN[6:0]							
default	0	0	0	0	0	0	0	0		

DRCMIN[6:0]

Sets the minimum gain that the DRC applies to a signal during attack.

DRCMIN [6:0]	Speaker Volume (dB)	DRCMIN [6:0]	Speaker Volume (dB)	DRCMIN [6:0]	Speaker Volume (dB)	DRCMIN [6:0]	Speaker Volume (dB)
1111111	0.00	1011111	-10.00	0111111	-36.00	0011111	Reserved
1111110	-0.25	1011110	-10.50	0111110	-37.00	0011110	Reserved
1111101	-0.50	1011101	-11.00	0111101	-38.00	0011101	Reserved
1111100	-0.75	1011100	-11.50	0111100	-39.00	0011100	Reserved
1111011	-1.00	1011011	-12.00	0111011	-40.00	0011011	Reserved
1111010	-1.25	1011010	-12.50	0111010	-41.00	0011010	Reserved
1111001	-1.50	1011001	-13.00	0111001	-42.00	0011001	Reserved
1111000	-1.75	1011000	-13.50	0111000	-43.00	0011000	Reserved
1110111	-2.00	1010111	-14.00	0110111	-44.00	0010111	Reserved
1110110	-2.25	1010110	-14.50	0110110	-45.00	0010110	Reserved
1110101	-2.50	1010101	-15.00	0110101	-46.00	0010101	Reserved
1110100	-2.75	1010100	-15.50	0110100	-47.00	0010100	Reserved
1110011	-3.00	1010011	-16.00	0110011	-48.00	0010011	Reserved
1110010	-3.25	1010010	-17.00	0110010	-49.00	0010010	Reserved
1110001	-3.50	1010001	-18.00	0110001	-50.00	0010001	Reserved
1110000	-3.75	1010000	-19.00	0110000	-51.00	0010000	Reserved
1101111	-4.00	1001111	-20.00	0101111	-52.00	0001111	Reserved
1101110	-4.25	1001110	-21.00	0101110	-53.00	0001110	Reserved
1101101	-4.50	1001101	-22.00	0101101	-54.00	0001101	Reserved
1101100	-4.75	1001100	-23.00	0101100	-55.00	0001100	Reserved
1101011	-5.00	1001011	-24.00	0101011	-56.00	0001011	Reserved
1101010	-5.25	1001010	-25.00	0101010	-57.00	0001010	Reserved
1101001	-5.50	1001001	-26.00	0101001	-58.00	0001001	Reserved
1101000	-5.75	1001000	-27.00	0101000	-59.00	0001000	Reserved
1100111	-6.00	1000111	-28.00	0100111	-60.00	0000111	Reserved
1100110	-6.50	1000110	-29.00	0100110	-61.00	0000110	Reserved
1100101	-7.00	1000101	-30.00	0100101	-62.00	0000101	Reserved
1100100	-7.50	1000100	-31.00	0100100	-63.00	0000100	Reserved
1100011	-8.00	1000011	-32.00	0100011	-64.00	0000011	Reserved
1100010	-8.50	1000010	-33.00	0100010	Reserved	0000010	Reserved
1100001	-9.00	1000001	-34.00	0100001	Reserved	0000001	Reserved
1100000	-9.50	1000000	-35.00	0100000	Reserved	0000000	Mute

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ADDR	B7	B6	B5	B4	B3	B2	B1	В0
0x1D		MCSSMT[2:0]		SSMT[2:0]		ERC	0
default	1	0	0	0	0	0	1	0

MCSSMT[2:0]

Sets the master clock spread spectrum modulation percentage. A setting of 000 results in a ±9.4% modulation. Modulating the master clock does not modulate the class-D output frequency because the triangle wave generator is PLL controlled.

MCSSMT[2:0]	± Modulation %
111	10.3
110	9.0
101	8.5
100	6.5
011	37.7
010	21.6
001	15.6
000	9.4

SSMT[2:0]

Sets the Class-D spread-spectrum modulation percentage. A setting of 000 results in ±9.4% modulation.

SSMT[2:0]	± Modulation %
111	10.3
110	9.0
101	8.5
100	6.5
011	37.7
010	21.6
001	15.6
000	9.4
111 110 101 100 011 010 001 000	10.3 9.0 8.5 6.5 37.7 21.6 15.6 9.4

ERC

1=Class-D edge rate control on. 0=Class-D edge rate control off.

ADDR	B7	B6	B5	B4	B3	B2	B1	B0
0x80	SRST	0	0	0	0	1	0	0
Default	1	0	0	0	0	1	0	0

SRST

1=Low-power Standby Mode. All registers are reset to their default values. All I²C write commands to bits other than SRST are ignored.

0=Normal operation.

ADDR	B7	B6	B5	B4	B3	B2	B1	B0
0x81	DRC_M	ODE[1:0]	DATRT[1:0]		NG_AT	RT[1:0]	0	MODESEL
default	0	0	0	1	1	1	0	0

DRC_MODE[1:0]

Sets the DRC's compression ratio.

DRC_MODE[1:0]	Compression Ratio		
11	Reserved		
10	Reserved		
01	2:1		
00	Off		

DATRT[1:0]

Sets the DRC's attack and release times. To avoid extraneous noise, do not change this setting while the speaker amplifier is on.

DATRT[1:0]	Attack Time (ms/step)	Release Time (ms/step)
11	1.0	200
10	0.5	200
01	0.1	200
00	0.1	20

NG_ATRT[1:0], MODESEL

Sets the noise gate attack, hold, and release times for the headphone and speaker amplifiers. To avoid extraneous noise, do not change this setting while the headphone or speaker amplifiers are on.

MODESEL	NG_ATRT[1:0]	Attack Time (ms/step)	Release Time (µs/step) SOFTVOL=0	Release Time (µs/step) SOFTVOL=1	Hold Time (ms)
1	11	800	200	2000	44
1	10	400	200	2000	44
1	01	100	200	2000	44
1	00	25	200	2000	44
0	11	800	1400	1400	44
0	10	400	1400	1400	44
0	01	100	1400	1400	44
0	00	25	1400	1400	44

ADDR	B7	B6	B5	B4	В3	B2	B1	В0
0x82	0x82 DPLT[2:0]		HP_NG_RAT[2:0]			HP_NG_ATT[1:0]		
Default	0	0	0	1	0	0	0	0

DPLT[2:0]

Sets the DRC's limiter value, regardless of SVDD supply voltage. Also sets dynamic range compression threshold. To avoid extraneous noise, do not change this setting while the speaker amplifier is on.

DPLT[2:0]	Limiter Voltage (V _{pk})	Maximum Power with Sine Wave and 8 Ω Load (mW)	DRC Threshold at Class-D Output (dB V _{pk})
111	3.79	900	-12.5
110	3.69	850	-12.7
101	3.58	800	-13.0
100	3.46	750	-13.3
011	3.35	700	-13.5
010	3.22	650	-13.8
001	3.10	600	-14.0
000	No Limit	No Limit	-12.5

HP_NG_RAT[2:0]

Sets the headphone noise gate threshold level. Detection is at the input to the headphone volume block.

HP_NG_RAT[2:0]	Threshold (mV _{pk})				
111	Reserved				
110	Reserved				
101	18				
100	12				
011	Noise Gate Disabled				
010	Noise Gate Disabled				
001	Noise Gate Disabled				
000	Noise Gate Disabled				

HP_NG_ATT[1:0]

Sets the headphone noise gate attenuation level.

HP_NG_ATT[1:0]	Attenuation Level (dB)		
11	-6.0		
10	-12.0		
01	-18.0		
00	Mute		

ADDR	B7	B6	B5	B4	B3	B2	B1	B0
0x83	0	0	NCLIP	SP_NG_RAT[2:0]		SP_NG	ATT[1:0]	
Default	0	0	0	1	0	0	0	0

NCLIP

1=Turns on the DRC's clip limiter. Amount of clipping is set by DALC. 0=DRC clip limiter is disabled.