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January 2013

FAN302HLMY_F117 PWM Controller for Low Standby Power Battery-Charger Applications — mWSaver™ Technology

Features

- mWSaver™ Technology Provides Industry's Best-in-Class Standby Power
  - Ultra Low Power Consumption at No Load (<10 mW at 230 V_{AC})
  - Proprietary 500V High-Voltage JFET Startup Reduces Startup Resistor Loss
  - Low Operation Current in Burst Mode: 350 µA Maximum
- Constant-Current (CC) Control without Secondary-Feedback Circuitry
- Fixed PWM Frequency at 85kHz with Frequency Hopping to Reduce EMI
- High-Voltage Startup
- Low Operating Current: 3.5 mA
- Peak-Current-Mode Control with Slope Compensation
- Cycle-by-Cycle Current Limiting
- V_{DD} Over-Voltage Protection (Auto-Restart)
- V_S Over-Voltage Protection (Latch Mode)
- V_{DD} Under-Voltage Lockout (UVLO)
- Gate Output Maximum Voltage Clamped at 15 V
- Fixed Over-Temperature Protection (Latch Mode)
- Available in an 8-Lead SOIC Package

Applications

- Battery Chargers for Cellular Phones, Cordless Phones, PDAs, Digital Cameras, and Power Tools
- Replaces Linear Regulators and RCC SMPS

Description

The FAN302HLMY_F117 advanced PWM controller significantly simplifies isolated power supply design that requires CC regulation of the output. The output current is precisely estimated with information in the primary side of the transformer and controlled with an internal compensation circuit. This removes the output current sensing loss and eliminates all external Control Circuitry (CC). The Green-Mode function, with an extremely low operating current (200 µA) in Burst Mode, maximizes the light-load efficiency, enabling conformance to worldwide Standby Mode efficiency guidelines.

Integrated protections include two-level pulse-by-pulse current limit, Over-Voltage Protection (OVP), brownout protection, and Over-Temperature Protection (OTP).

Compared with a conventional approach using an external control circuit in the secondary side for CC regulation, the FAN302HLMY_F117 can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability.

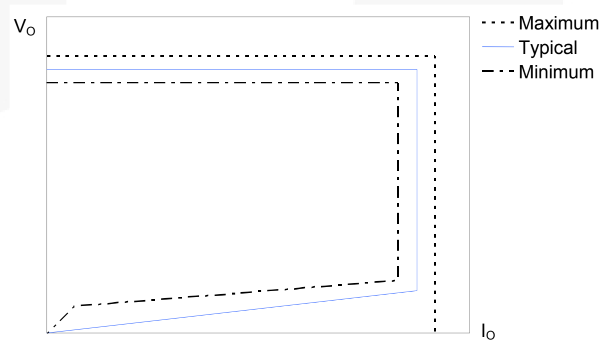


Figure 1. Typical Output V-I Characteristic

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN302HLMY_F117	-40°C to +105°C	8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel

Application Diagram

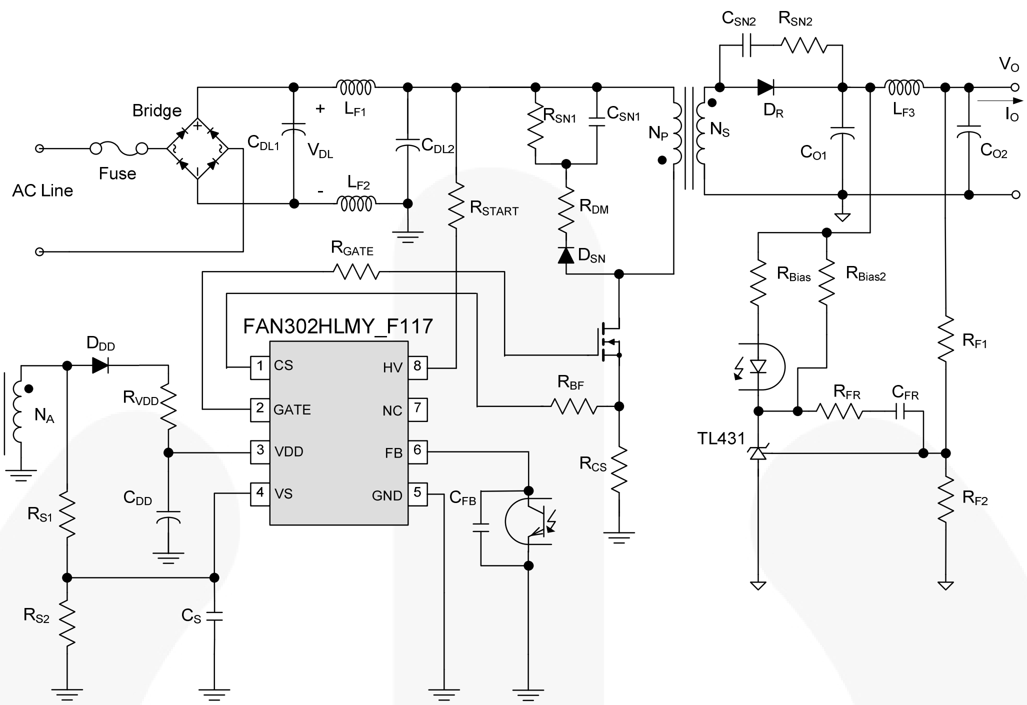


Figure 2. Typical Application

Internal Block Diagram

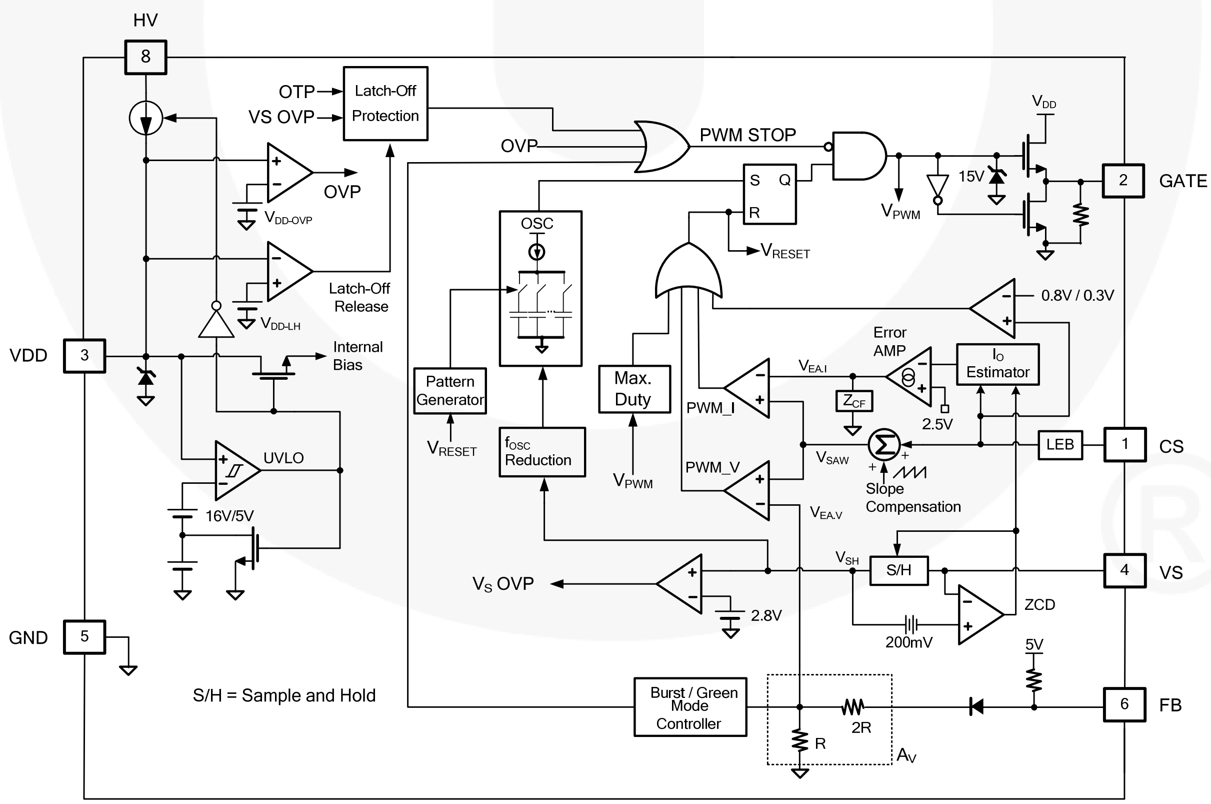
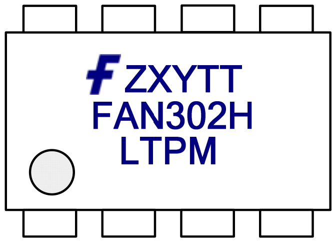


Figure 3. Functional Block Diagram

Marking Information



F- Fairchild Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: M=SOIC
P: Y= Green Package
M: Manufacture Flow Code

Figure 4.Top Mark

Pin Configuration

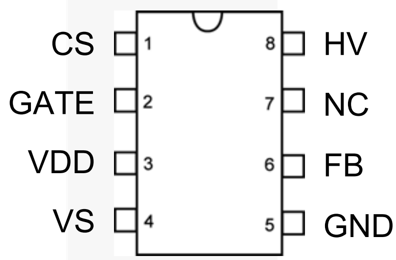


Figure 5. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	CS	**Current Sense**. This pin connects a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation. The current-sense information is also used to estimate the output current for CC regulation.
2	GATE	**PWM Signal Output**. This pin has an internal totem-pole output driver to drive the power MOSFET. It is internally clamped at 15 V.
3	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external V_{DD} capacitor.
4	VS	**Voltage Sense**. This pin detects the output voltage information and diode current discharge time based on the voltage of the auxiliary winding.
5	GND	**Ground**
6	FB	**Feedback**. Typically, an opto-coupler is connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.
7	NC	No Connect
8	HV	**High Voltage**. This pin connects to the DC bus for high-voltage startup.

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>V_{HV}</td><td colspan="2">HV Pin Input Voltage</td><td></td><td>500</td><td>V</td></tr>
<tr><td>V_{VDD}</td><td colspan="2">DC Supply Voltage[1,2]</td><td></td><td>30</td><td>V</td></tr>
<tr><td>V_{VS}</td><td colspan="2">VS Pin Input Voltage</td><td>-0.3</td><td>7.0</td><td>V</td></tr>
<tr><td>V_{CS}</td><td colspan="2">CS Pin Input Voltage</td><td>-0.3</td><td>7.0</td><td>V</td></tr>
<tr><td>V_{FB}</td><td colspan="2">FB Pin Input Voltage</td><td>-0.3</td><td>7.0</td><td>V</td></tr>
<tr><td>P_D</td><td colspan="2">Power Dissipation (T_A=25°C)</td><td></td><td>660</td><td>mW</td></tr>
<tr><td>θ_{JA}</td><td colspan="2">Thermal Resistance (Junction-to-Air)</td><td></td><td>150</td><td>°C/W</td></tr>
<tr><td>θ_{JC}</td><td colspan="2">Thermal Resistance (Junction-to-Case)</td><td></td><td>39</td><td>°C/W</td></tr>
<tr><td>T_J</td><td colspan="2">Operating Junction Temperature</td><td>-40</td><td>+150</td><td>°C</td></tr>
<tr><td>T_{STG}</td><td colspan="2">Storage Temperature Range</td><td>-55</td><td>+150</td><td>°C</td></tr>
<tr><td>T_L</td><td colspan="2">Lead Temperature, (Wave Soldering or IR, 10 Seconds)</td><td></td><td>+260</td><td>°C</td></tr>
<tr><td rowspan="2">ESD</td><td rowspan="2">Electrostatic Discharge Capability</td><td>Human Body Model, JEDEC:JESD22_A114 (Except HV Pin)[3]</td><td></td><td>5000</td><td rowspan="2">V</td></tr>
<tr><td>Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)[3]</td><td></td><td>1500</td></tr>
</table>

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD ratings including the HV pin: HBM=400 V, CDM=750 V.

Electrical Characteristics

V_{DD}=15 V and T_A=25°C unless noted.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
HV Section							
$V_{HV\text{-}MIN}$	Minimum Startup Voltage on HV Pin					50	V
I_{HV}	Supply Current Drawn from HV Pin		V_{HV}=100 V, V_{DD}=0 V, Controller Off	0.8	1.5	5.0	mA
$I_{HV\text{-}LC}$	Leakage Current Drawn from HV Pin		V_{HV}=500 V, V_{DD}=15 V (Controller On with Auxiliary Supply)		0.8	3.0	µA
V_{DD} Section							
V_{OP}	Continuous Operation Voltage		Limited by V_{DD} Over-Voltage Protection (OVP)			25	V
$V_{DD\text{-}ON}$	Turn-On Threshold Voltage		V_{DD} Rising	15	16	17	V
$V_{DD\text{-}OFF}$	Turn-Off Threshold Voltage		V_{DD} Falling	4.7	5.0	5.3	V
$V_{DD\text{-}LH}$	Threshold Voltage for Latch-Off Release		V_{DD} Falling		2.5		V
$I_{DD\text{-}ST}$	Startup Current		V_{DD}=$V_{DD\text{-}ON}$ – 0.16 V		400	450	µA
$I_{DD\text{-}OP}$	Operating Supply Current		V_{DD}=18 V, f=f_{OSC}, C_{GATE}=1 nF		3.5	4.0	mA
$I_{DD\text{-}BURST}$	Burst-Mode Operating Supply Current		V_{DD}=8 V, C_{GATE}=1 nF		200	350	µA
$V_{DD\text{-}OVP}$	V_{DD} Over-Voltage Protection Level			25.0	26.5	28.0	V
$t_{D\text{-}VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		f=85 kHz		100	180	µs
Oscillator Section							
f_{OSC}	Frequency	Center Frequency	V_{CS}=5 V, V_S=2.5 V, V_{FB}=5 V	82	85	88	kHz
		Hopping Range			±3		kHz
$f_{OSC\text{-}CM\text{-}MIN}$	Minimum Frequency for Continuous Conduction Mode (CCM) Prevention Circuit(4)			13	18	23	kHz
$f_{OSC\text{-}CCM}$	Minimum Frequency in Constant Current (CC) Regulation		V_{CS}=5 V, V_S=0 V	23	26	29	kHz
Feedback Input Section							
A_V	Internal Voltage Scale-Down Ratio of FB Pin(5)			1/3.5	1/3.0	1/2.5	V/V
Z_{FB}	FB Pin Input Impedance			38	42	44	kΩ
$V_{FB\text{-}OPEN}$	FB Pin Pull-Up Voltage		FB Pin Open		5.3		V
$V_{FB\text{-}L}$	FB Threshold to Disable Gate Drive in Burst Mode		V_{FB} Falling,V_{CS}=5 V, V_S=0 V	1.2	1.4	1.6	V
$V_{FB\text{-}H}$	FB Threshold to Enable Gate Drive in Burst Mode		V_{FB} Rising,V_{CS}=5 V, V_S=0 V	1.3	1.5	1.7	V
Over-Temperature Protection Section							
T_{OTP}	Threshold for Over-Temperature Protection (OVP)			+130	+140	+150	°C

Continued on the following page…

Electrical Characteristics (Continued)

V_{DD}=15 V and T_A=25°C unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Voltage-Sense Section						
I_{TC}	Bias Current	V_{CS}=5 V	8.75	10.00	11.25	µA
$V_{VS-CM-MIN}$	V_S Sampling Voltage to Switch to the Second Pulse-by-Pulse Current Limit in Power Limit Mode(6)			0.55		V
$V_{VS-CM-MAX}$	V_S Sampling Voltage to Switch Back to the Normal Pulse-by-Pulse Current Limit(6)			0.75		V
V_{SN-CC}	V_S Sampling Voltage to Start Frequency Decreasing in CC Mode	V_{CS}=5 V, f_{S1}=f_{OSC}-2 kHz	2.05	2.15	2.25	V
V_{SG-CC}	Vs Sampling Voltage to End Frequency Decreasing in CC Mode	V_{CS}=5 V, f_{S2}=$f_{OSC-CCM}$ +2 kHz	0.45	0.70	0.95	V
S_{G-CC}	Frequency Decreasing Slope of CC Regulation	S_{G-CC}= (f_{S1}-f_{S2}) / (V_{SN-CC}-V_{SG-CC})	30	38	46	kHz/V
$V_{VS-OFFSET}$	ZCD Comparator Internal Offset Voltage(6)			200		mV
V_{VS-OVP}	Output Over-Voltage Protection with V_S Sampling Voltage		2.70	2.80	2.85	V
t_{VS-OVP}	Output Over-Voltage Protection Debounce Time	f_{OSC}=85 kHz		8		cycles
Current-Sense Section						
V_{VR}	Internal Reference Voltage for CC Regulation		2.475	2.500	2.525	V
V_{CCR}	Variation Test Voltage on CS Pin for CC Output (Non-Inverting Input of Error Amplifier for CC Regulation)	V_{CS}=0.47 V	2.405	2.430	2.455	V
V_{STH}	Normal Current Limit Threshold Voltage			0.8		V
V_{STH-VA}	Second Current Limit Threshold Voltage, Power Limit Mode (V_S<$V_{VS-CM-MAX}$)	V_{VS}=0.3 V		0.30		V
t_{PD}	GATE Output Turn-Off Delay			100	150	ns
t_{MIN}	Minimum On Time	V_{CS}=5 V, V_{VS}=2.5 V, V_{FB}=5 V (Test Mode)	430	530	630	ns
t_{LEB}	Leading-Edge Blanking Time(6)		100	150	200	ns
V_{SLOPE}	Slope Compensation(6)	Maximum Duty Cycle		0.3		V
GATE Section						
D_{MAX}	Maximum Duty Cycle		64	67	70	%
V_{GATE-L}	Output Voltage Low	V_{DD}=25 V, I_O=10 mA	0		1.5	V
V_{GATE-H}	Output Voltage High	V_{DD}=8 V, I_O=1 mA	5		8	V
V_{GATE-H}	Output Voltage High	V_{DD}=5.5 V, I_O=1 mA	4.0		5.5	V
t_r	Rising Time	V_{DD}=15 V, C_{GATE}=1 nF	100	140	180	ns
t_f	Falling Time	V_{DD}=15 V, C_{GATE}=1 nF	30	50	70	ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=25 V	13	15	17	V

Notes:

4. $f_{OSC-CM-MIN}$ occurs when the power unit enters CCM operation.
5. A_V is a scale-down ratio of the internal voltage divider of the FB pin.
6. Guaranteed by design; not production tested.

Typical Performance Characteristics

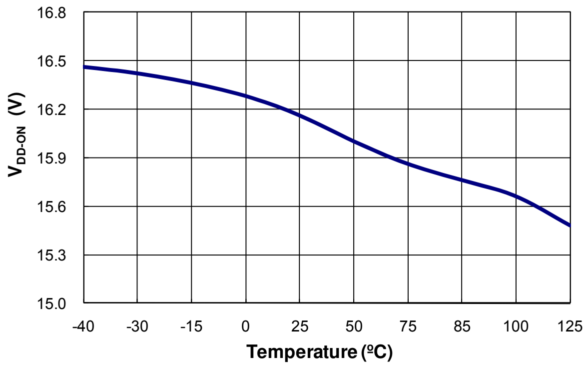


Figure 6. V_{DD} Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

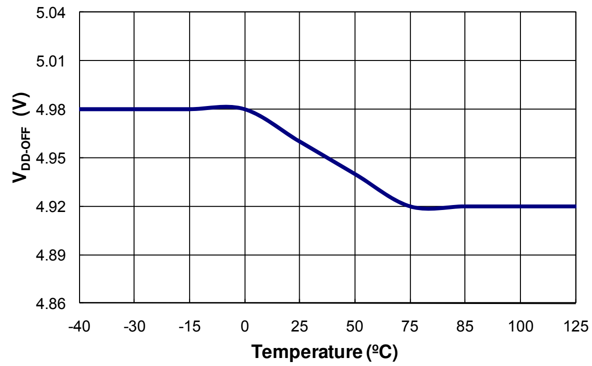


Figure 7. V_{DD} Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

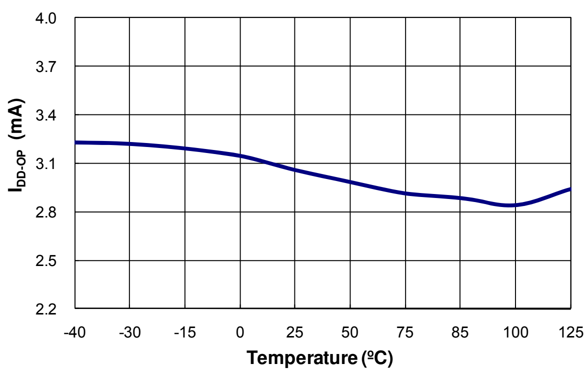


Figure 8. Operating Current (I_{DD-OP}) vs. Temperature

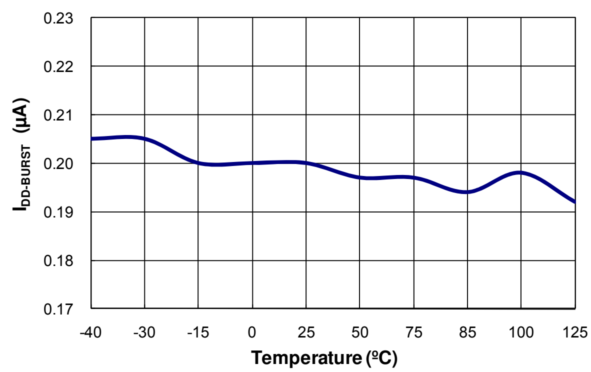


Figure 9. Burst Mode Operating Current ($I_{DD-BURST}$) vs. Temperature

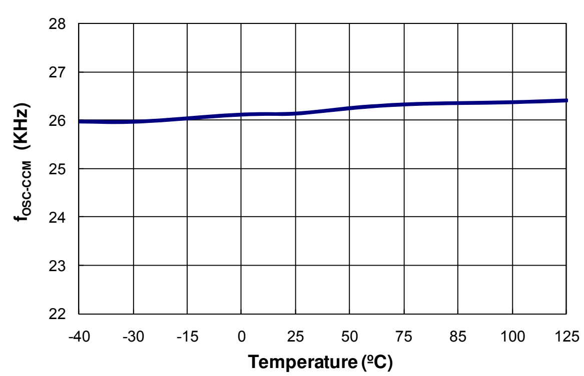


Figure 10. CC Regulation Minimum Frequency ($f_{OSC-CCM}$) vs. Temperature

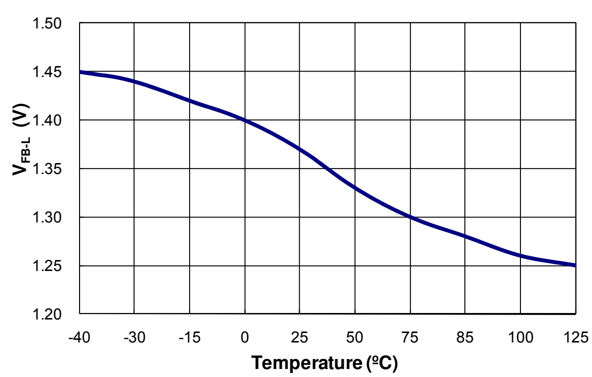


Figure 11. Enter Zero-Duty Cycle of FB Voltage (V_{FB-L}) vs. Temperature

Typical Performance Characteristics

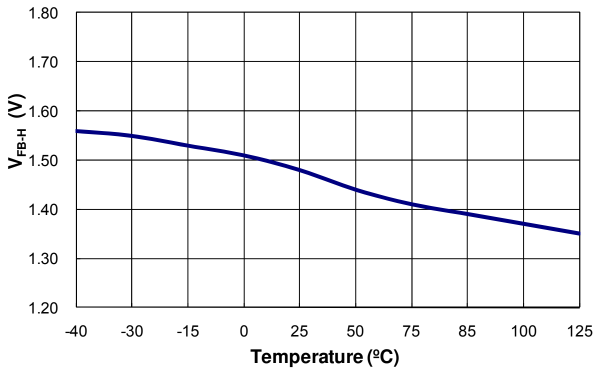


Figure 12. Leave Zero Duty Cycle of FB Voltage (V_{FB-H}) vs. Temperature

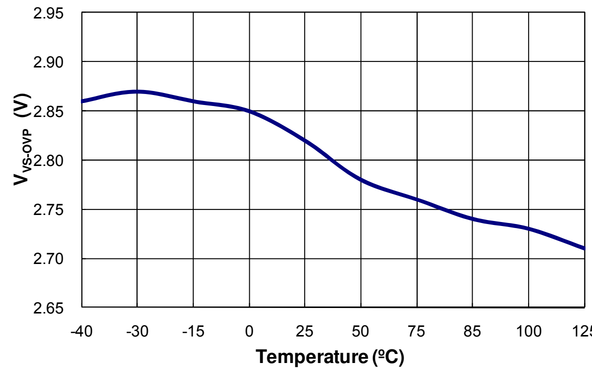


Figure 13. V_S Over-Voltage Protection (V_{VS-OVP}) vs. Temperature

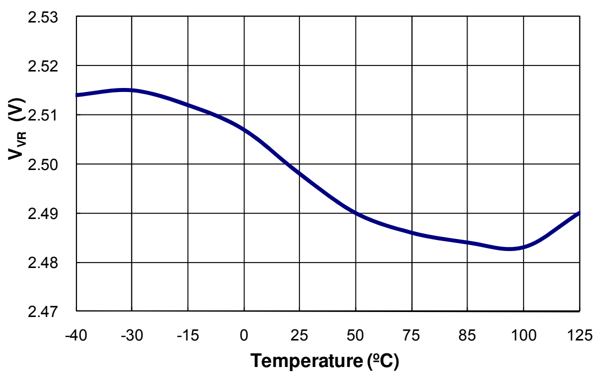


Figure 14. Reference Voltage of CS (V_{VR}) vs. Temperature

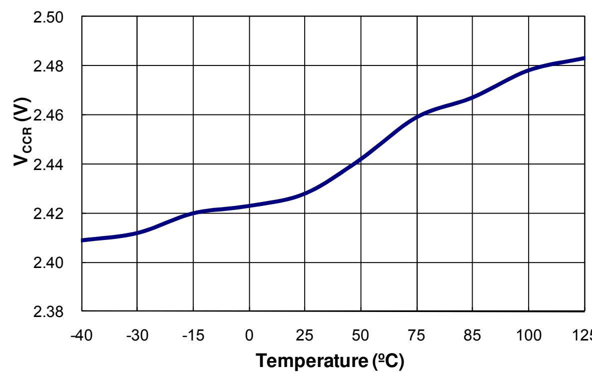


Figure 15.Variation Voltage on CS Pin for Constant-Current Regulation (V_{CCR}) vs. Temperature

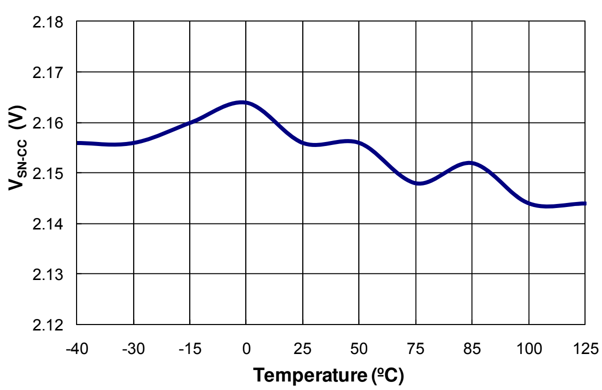


Figure 16. Starting Voltage of Frequency Decreasing of CC Regulation (V_{SN-CC}) vs. Temperature

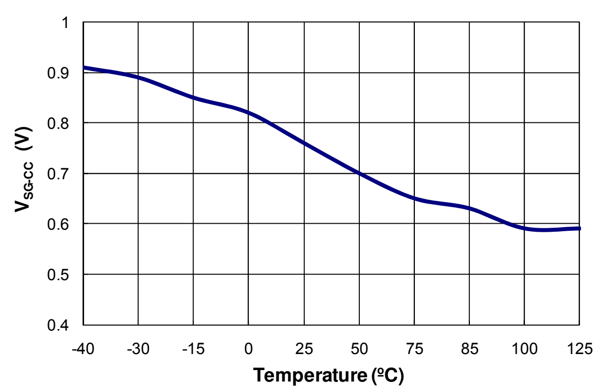


Figure 17. Ending Voltage of Frequency Decreasing of CC Regulation (V_{SG-CC}) vs. Temperature

Typical Performance Characteristics

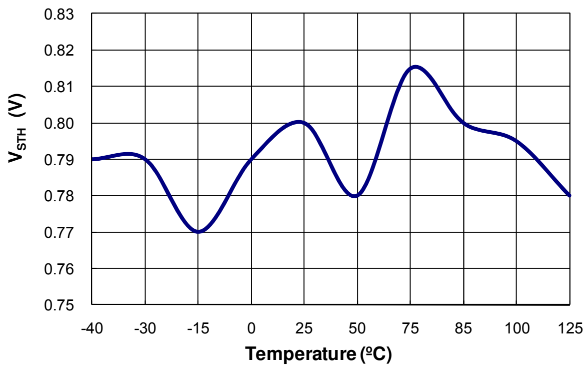


Figure 18. Threshold Voltage for Current Limit (V_{STH}) vs. Temperature

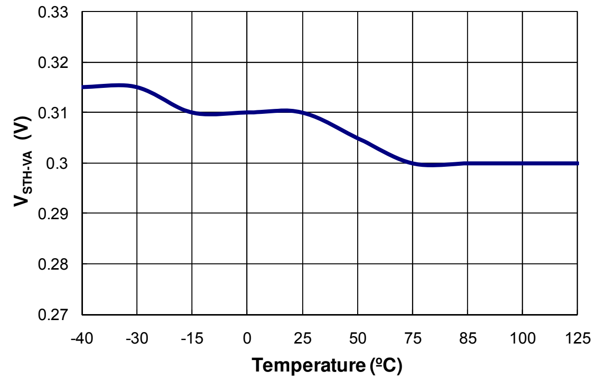


Figure 19. Threshold Voltage for Current Limit at Power Mode (V_{STH-VA}) vs. Temperature

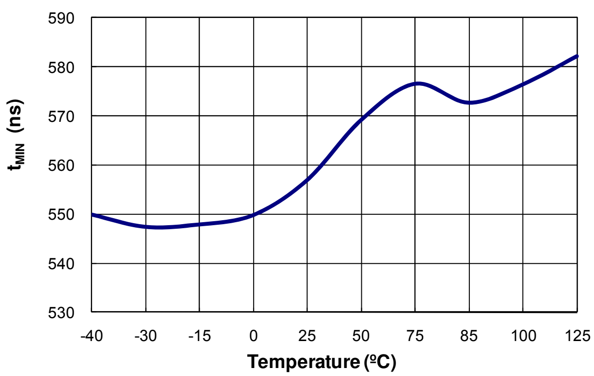


Figure 20. Minimum On Time (t_{MIN}) vs. Temperature

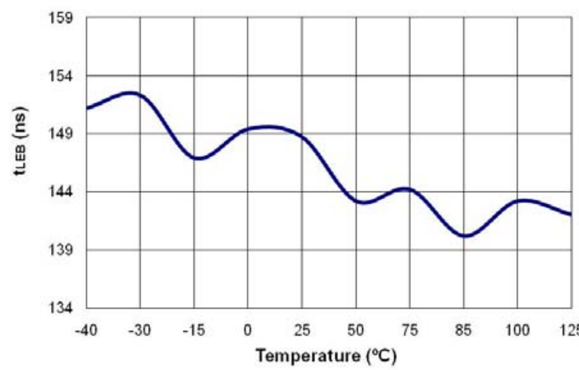


Figure 21.Leading-Edge Blanking Time (t_{LEB}) vs. Temperature

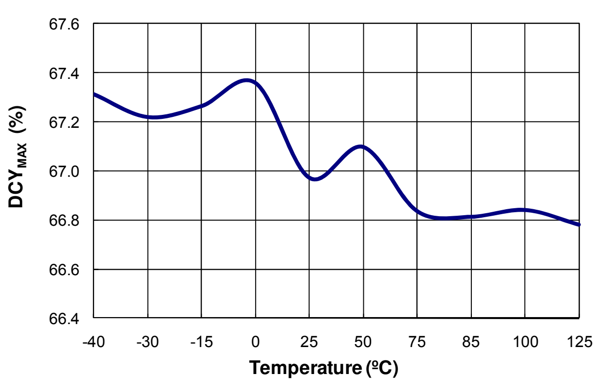


Figure 22. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

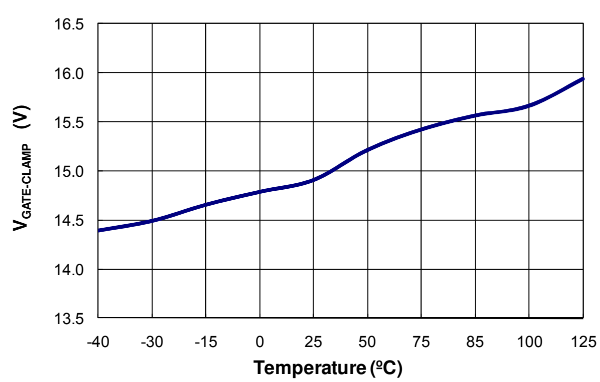


Figure 23. Gate Output Clamp Voltage ($V_{GATE-CLAMP}$) vs. Temperature

Operational Description

Basic Control Principle

Figure 24 shows the internal PWM control circuit. The constant voltage (CV) regulation is implemented in the same way as the conventional isolated power supply, where the output voltage is sensed using a voltage divider and compared with the internal 2.5 V reference of a shunt regulator (KA431) to generate a compensation signal. The compensation signal is transferred to the primary side using an opto-coupler and scaled down through attenuator Av, generating the $V_{EA.V}$ signal. Then the error signal $V_{EA.V}$ is applied to the PWM comparator (PWM.V) to determine the duty cycle.

Meanwhile, the CC regulation is implemented internally without directly sensing the output current. The output current estimator reconstructs output current information (V_{CCR}) using the transformer primary-side current and diode current discharge time. Then V_{CCR} is compared with a reference voltage (2.5 V) by an internal error amplifier, generating the $V_{EA.I}$ signal to determine the duty cycle.

The two error signals, $V_{EA.I}$ and $V_{EA.V}$, are compared with an internal sawtooth waveform (V_{SAW}) by PWM comparators PWM.I and PWM.V to determine the duty cycle. As shown in Figure 25, the outputs of two comparators (PWM.I and PWM.V) are combined with an OR gate and used as a reset signal of flip-flop to determine the MOSFET turn-off instant. The lower signal, $V_{EA.V}$ or $V_{EA.I}$, determines the duty cycle, as shown in Figure 25. During CV regulation, $V_{EA.V}$ determines the duty cycle while $V_{EA.I}$ is saturated to HIGH. During CC regulation, $V_{EA.I}$ determines the duty cycle while $V_{EA.V}$ is saturated to HIGH.

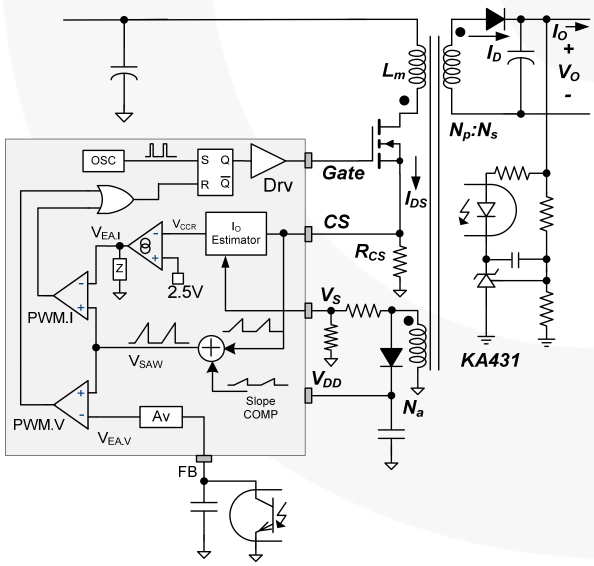


Figure 24. Internal PWM Control Circuit

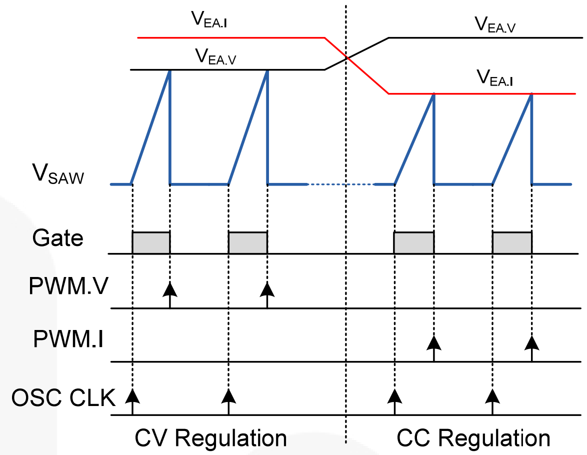


Figure 25. PWM Operation for CC and CV

Output Current Estimation

Figure 26 shows the key waveform of a flyback converter operating in Discontinuous Conduction Mode (DCM), where the secondary-side diode current reaches zero before the next switching cycle begins. Since the output current estimator is designed for DCM operation, the power stage should be designed such that DCM is guaranteed for the entire operating range. The output current is obtained by averaging the triangular output diode current area over a switching cycle:

$$I_O = < I_D >_{AVG} = I_{PK} \frac{N_P}{N_S} \bullet \frac{t_{DIS}}{2t_S} \quad (1)$$

where I_{PK} is the peak value of the primary-side current; N_P and N_S are the number of turns of transformer primary-side and secondary-side, respectively; t_{DIS} is the diode current discharge time; and t_S is the switching period.

With a given current sensing resistor, the output current can be programmed as:

$$I_O = \frac{1.25}{K \bullet R_{SENSE}} \frac{N_P}{N_S} \quad (2)$$

where K is the design parameter of IC, which is 10.5.

The peak value of primary-side current is obtained by an internal peak detection circuit, while diode current discharge time is obtained by detecting the diode current zero-crossing instant. Since the diode current cannot be sensed directly with primary-side control, Zero Crossing Detection (ZCD) is accomplished indirectly by monitoring the auxiliary winding voltage. When the diode current reaches zero, the transformer winding voltage begins to drop by the resonance between the MOSFET output capacitance and the transformer magnetizing inductance. To detect the starting instant of the resonance, the V_S is sampled at 85% of diode current discharge time of the previous switching cycle, then compared with the instantaneous V_S voltage. When instantaneous V_S drops below the sampled voltage by more than 200 mV, ZCD of diode current is obtained, as shown in Figure 27.

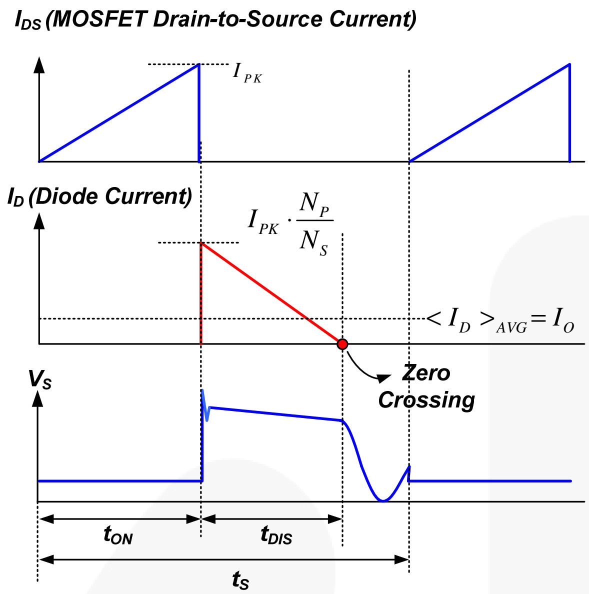


Figure 26. Key Waveforms of DCM Flyback Converter

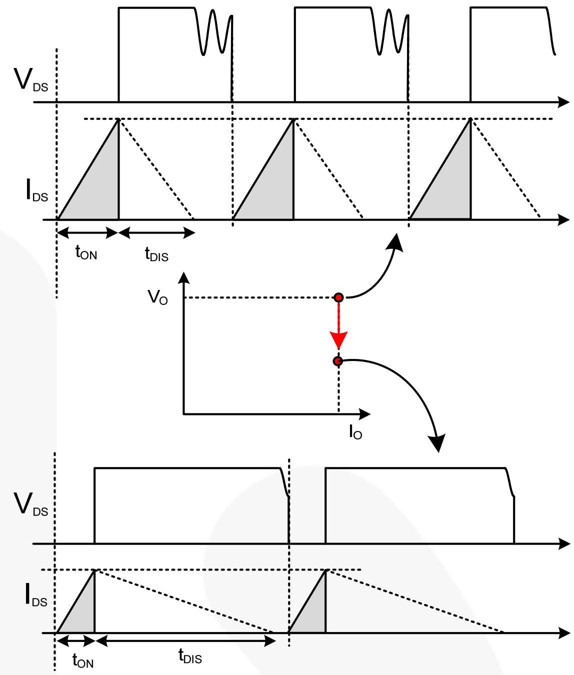


Figure 28. t_{DIS} Variation in CC Mode

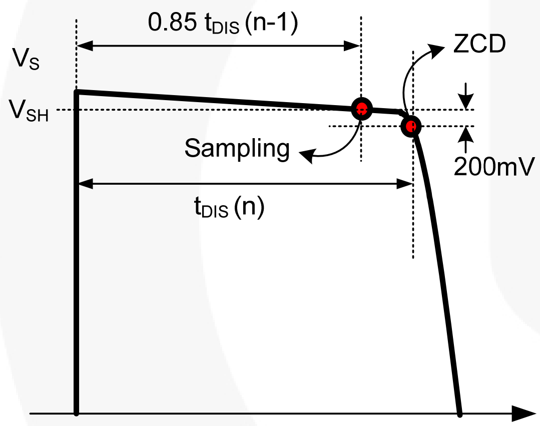


Figure 27. Detailed Waveform for ZCD

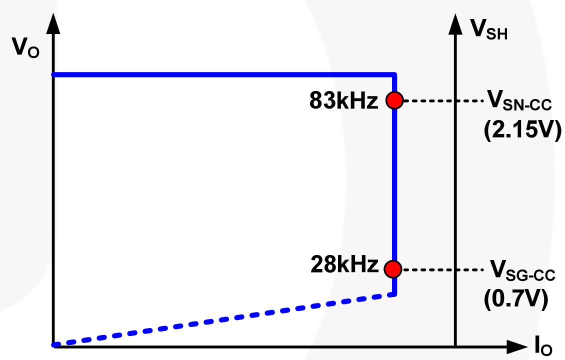


Figure 29. Frequency Reduction with V_{SH}

Frequency Reduction in CC Mode

An important design consideration is that the transformer guarantee DCM operation across the whole range since the output current is properly estimated only in DCM operation. As can be seen in Figure 28, the discharge time (t_{DIS}) of the diode current increases as the output voltage decreases in CC Mode. The converter tends to go into CCM as output voltage drops in CC Mode when operating at the fixed switching frequency. To prevent this CCM operation while maintaining good output current estimation in DCM, FAN302HLMY_F117 decreases switching frequency as output voltage drops, as shown in Figure 28 and Figure 29. FAN302HLMY_F117 indirectly monitors the output voltage by the sample-and-hold voltage (V_{SH}) of V_S, which is taken at 85% of diode current discharge time of the previous switching cycle, as shown in Figure 27. Figure 30 shows how the frequency reduces as the sample-and-hold voltage of VS decreases.

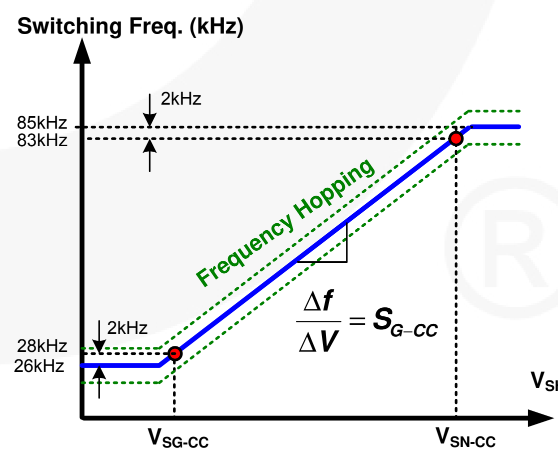


Figure 30. Frequency Reduction Curve in CC Regulation

CCM Prevention Function

Even if the power supply is designed to operate in DCM, it can go into CCM when there is not enough design margin to cover all the circuit parameter variations and operating conditions. FAN302HLMY_F117 has a CCM-prevention function that delays the next cycle turn-on of MOSFET until ZCD on the VS pin is obtained, as shown in Figure 31. To guarantee stable DCM operation, FAN302HLMY_F117 prohibits the turn-on of the next switching cycle for 10% of its switching period after ZCD is obtained. In Figure 31, the first switching cycle has ZCD before 90% of its original switching period and, therefore, the turn-on instant of the next cycle is determined without being affected by the ZCD instant. The second switching cycle does not have ZCD by the end of the original switching period; thus, the turn-on of the third switching cycle occurs after ZCD is obtained, with a delay of 10% of its original switching period. The minimum switching frequency that CCM prevention function allows is 18 kHz ($f_{OSC\text{-}CM\text{-}MIN}$). If the ZCD is not given until the end of maximum switching period of 55.6 µs (1/18 kHz), the converter can go into CCM operation, losing output regulation.

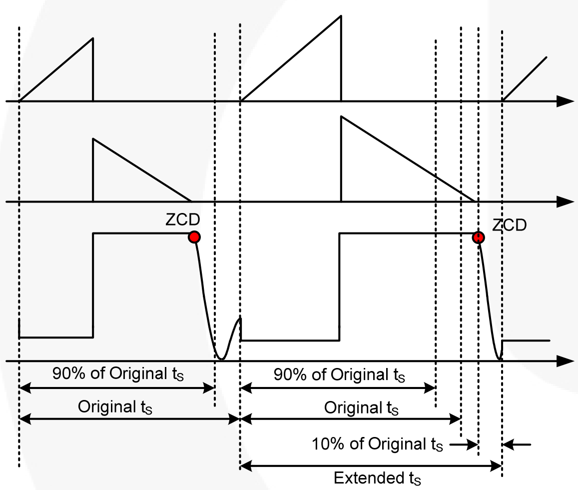


Figure 31. CCM Prevention Function

Power Limit Mode

When the sampled voltage of VS (V_{SH}) drops below $V_{S\text{-}CM\text{-}MIN}$ (0.55 V), FAN302HLMY_F117 enters constant Power Limit Mode, where the primary-side current-limit voltage (V_{CS}) changes from V_{STH} (0.8 V) to $V_{STH\text{-}VA}$ (0.3 V) to avoid V_S sampling and ZCD, as shown in Figure 32. Once V_S sampling voltage is higher than $V_{S\text{-}CM\text{-}MAX}$ (0.75 V), the V_{CS} returns to V_{STH}. This mode prevents the power supply from going into CCM and losing output regulation when the output voltage is too low. This effectively protects the power supply when there is a fault condition in the load, such as output short or overload. This mode also implements soft-start by limiting the transformer current until V_S sampling voltage reaches $V_{S\text{-}CM\text{-}MAX}$ (0.75 V).

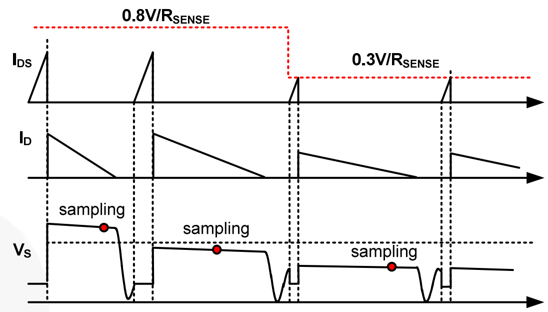


Figure 32. Power Limit Mode Operation

High-Voltage Startup

Figure 33 shows the high-voltage (HV) startup circuit. Internally, JFET is used to implement the high-voltage current source, whose characteristics are shown in Figure 34. Technically, the HV pin can be directly connected to the DC link (V_{DL}). To improve reliability and surge immunity; it is typical to use about a 100 kΩ resistor between the HV pin and the DC link. The actual HV current with given DC link voltage and startup resistor is determined by the intersection of V-I characteristics line and load line, as shown in Figure 34.

During startup, the internal startup circuit is enabled and the DC link supplies the current, I_{HV}, to charge the hold-up capacitor, C_{VDD}, through R_{START}. When the V_{DD} voltage reaches $V_{DD\text{-}ON}$, the internal HV startup circuit is disabled and the IC starts PWM switching. Once the HV startup circuit is disabled, the energy stored in C_{VDD} should supply the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, C_{VDD} should be designed to prevent V_{DD} from dropping to $V_{DD\text{-}OFF}$ before the auxiliary winding builds up enough voltage to supply V_{DD}. Capacitance tolerance is an important factor to consider for C_{DD} selection. Connecting a 22 µF capacitor between the V_{DD} and GND pins is recommended to ensure system stability across the wide operation temperature range.

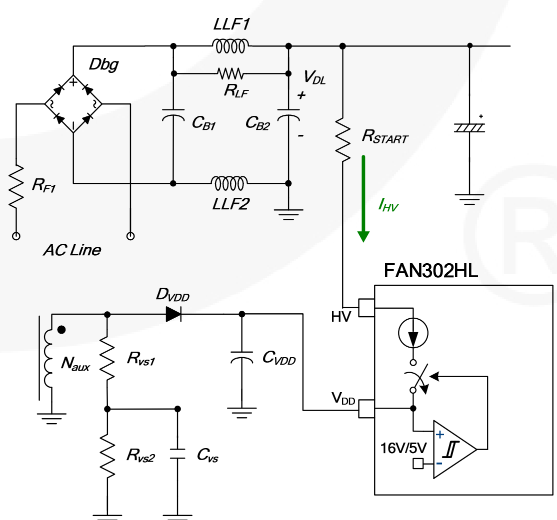


Figure 33. HV Startup Circuit

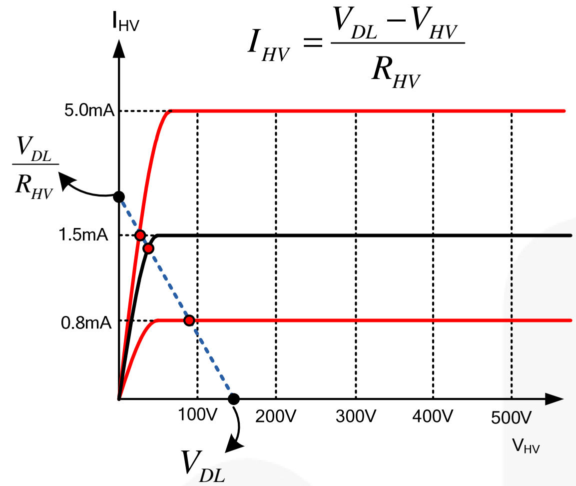


Figure 34.V-I Characteristics of HV Pin

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth of the EMI test equipment. The frequency-hopping circuit changes the switching frequency progressively between 82 kHz and 88 kHz with a period of t_p, as shown in Figure 35.

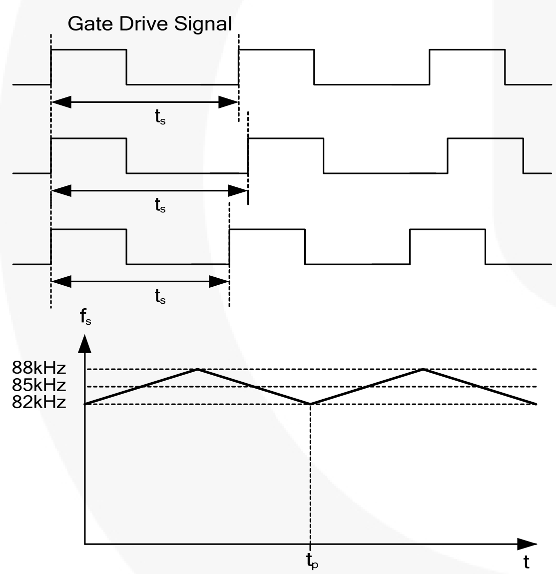


Figure 35. Frequency Hopping

Burst-Mode Operation

The power supply enters Burst Mode at no-load or extremely light-load conditions. As shown in Figure 36, when V_{FB} drops below V_{FBL}; the PWM output shuts off and the output voltage drops at a rate dependent on load current. This causes the feedback voltage to rise. Once V_{FB} exceeds V_{FBH}, the internal circuit starts to provide switching pulse. The feedback voltage then falls and the process repeats. Burst Mode operation alternately enables and disables switching of the MOSFET, reducing the switching losses in Standby Mode. Once FAN302HLMY_F117 enters Burst Mode, the operating current is reduced from 3.5 mA to 200 μA to minimize power consumption.

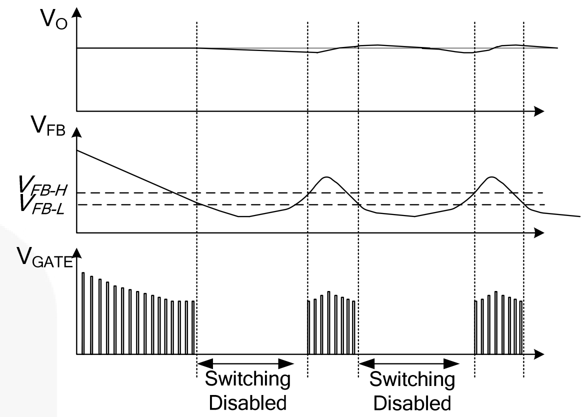


Figure 36. Burst-Mode Operation

Slope Compensation

The sensed voltage across the current-sense resistor is used for Current-Mode control and pulse-by-pulse current limiting. A synchronized ramp signal with positive slope is added to the current sense information at each switching cycle, improving noise immunity of Current-Mode control.

Protections

The self-protection functions include V_{DD} Over-Voltage Protection (OVP), internal Over-Temperature Protection (OTP), V_S Over-Voltage Protection (OVP), and brownout protection. V_{DD} OVP and brownout protection are implemented as Auto-Restart Mode, while the V_S OVP and internal OTP are implemented as Latch Mode.

When an Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5 V; the protection is reset, the internal startup circuit is enabled, and the supply current drawn from the HV pin charges the hold-up capacitor. When V_{DD} reaches the turn-on voltage of 16 V, normal operation resumes. In this manner, auto-restart alternately enables and disables MOSFET switching until the abnormal condition is eliminated, as shown in Figure 37.

When a Latch Mode protection is triggered, PWM switching is terminated and the MOSFET remains off, causing V_{DD} to drop. When V_{DD} drops to the V_{DD} turn-off voltage of 5 V, the internal startup circuit is enabled without resetting the protection and the supply current drawn from HV pin charges the hold-up capacitor. Since the protection is not reset, the IC does not resume PWM switching even when V_{DD} reaches the turn-on voltage of 16 V, disabling HV startup circuit. Then V_{DD} drops down to 5 V. In this manner, the Latch Mode protection alternately charges and discharges V_{DD} until there is no more energy in the DC link capacitor. The protection is reset when V_{DD} drops to 2.5 V, which is allowed only after the power supply is unplugged from the AC line, as shown in Figure 38.

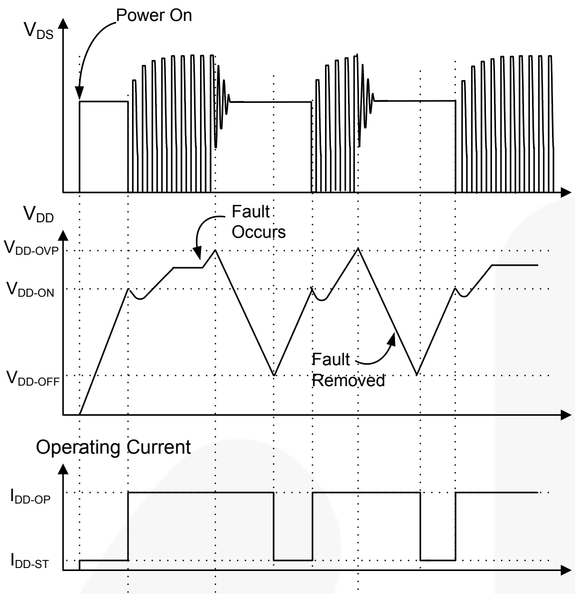


Figure 37. Auto-Restart Mode Operation

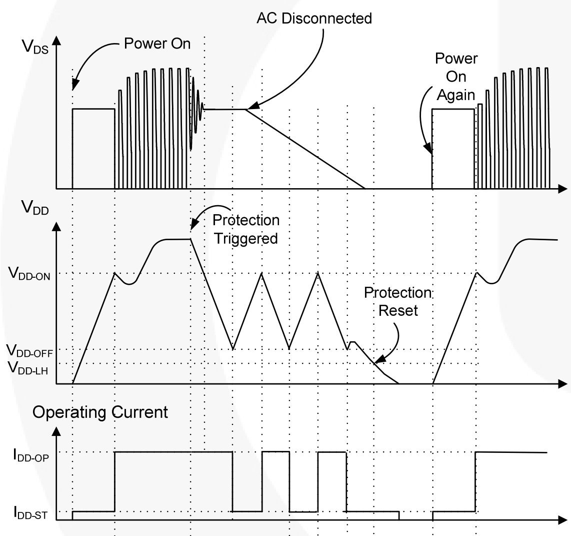


Figure 38. Latch-Mode Operation

Over-Temperature Protection (OTP)

The temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 140°C (t_{OTP}).

V_{DD} Over-Voltage Protection

V_{DD} over-voltage protection prevents IC damage from over-voltage exceeding the IC voltage rating. When the V_{DD} voltage exceeds 26.5 V due to an abnormal condition, the protection is triggered. This protection is typically caused by open circuit in the secondary-side feedback network.

Input Voltage Sensing

The FAN302HL indirectly senses input voltage using the VS pin current while the MOSFET is turned on. Since the VS pin voltage is clamped at 0.7 V when the MOSFET is turned on, the current flowing out of the VS pin is approximately proportional to the input voltage as:

$$I_{VS.ON} = \frac{(\frac{N_A}{N_P}V_{DL} + 0.7)}{R_{VS1}} + \frac{0.7}{R_{VS2}} \cong \frac{N_A}{N_P}\frac{V_{DL}}{R_{VS1}} \quad (3)$$

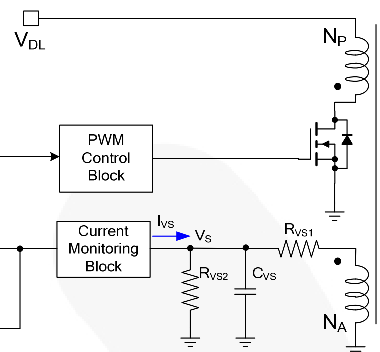


Figure 39. Vs Pin Current Sensing

FAN302HL modulates the minimum on time of the MOSFET such that it reduces as input voltage increases, as shown Figure 40. This allows smaller minimum on time for high line condition, ensuring Burst Mode operation occurs at almost same power level regardless of line voltage variation. The minimum on time is related to the bundle frequency of Burst Mode.

When selecting R_{VS1} and R_{VS2}, 150 µA is the VS current level to consider seriously. If the VS current is lower than 150 µA, t_{on_min} won't be larger.

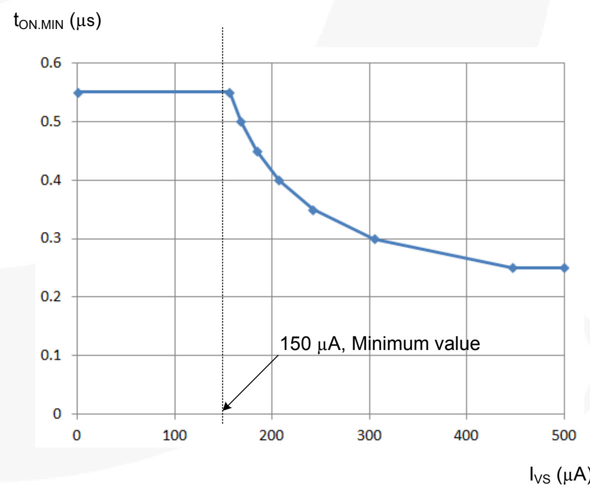


Figure 40. Minimum On Time vs. VS Pin Current

V_S Over-Voltage Protection (OVP)

V_S over-voltage protection prevents damage due to output over-voltage conditions. Figure 41 shows the VS OVP protection method. The OVP is triggered when the V_S sampling voltage is above 2.8 V (V_{VS_OVP}) for longer than eight switching cycles. Then PWM pulses are disabled and FAN302HL enters Latch Mode. The protection is reset and normal operation resumes when V_{DD} drops below $V_{DD\text{-}LH}$. V_S over-voltage conditions are usually caused by an open circuit in the secondary-side feedback network or abnormal behavior by the VS pin divider resistor.

When the secondary-side feedback circuit is opened, no current flows through the opto-coupler diode, which pulls up the feedback voltage, commanding maximum power be delivered to the load. Since more power than the load demand is delivered, the output voltage rises until the OVP is triggered.

The worst-case OVP trip point at no load is calculated as:

$$V_O^{OVP} = \sqrt{\left[V_{VS\_OVP}\frac{N_S}{N_A}\frac{R_{VS1}+R_{VS2}}{R_{VS2}}\right]^2 + \frac{2E_{SURPLUS}}{C_O}} \qquad (4)$$

where $E_{SURPLUS}$ is the surplus energy delivered to the load during the debounce time.

The $E_{SURPLUS}$ can be defined as:

$$E_{SURPLUS} = \frac{L_m}{2}\left(\frac{V_{STH}}{R_{CS}} + \frac{V_{DL}}{L_m}(t_{DLY.OFF})\right)^2 \times 8 \qquad (5)$$

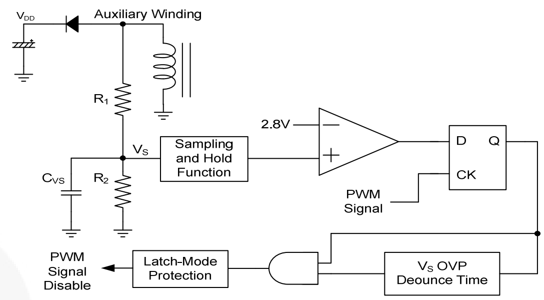


Figure 41. V_S OVP Protection

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs at the sense resistor. To avoid premature termination of the switching pulse, a 150 ns leading-edge blanking time is built in. Conventional RC filtering can therefore be omitted. During this blanking period, the current-limit comparator is disabled and it cannot switch off the gate driver.

Noise Immunity

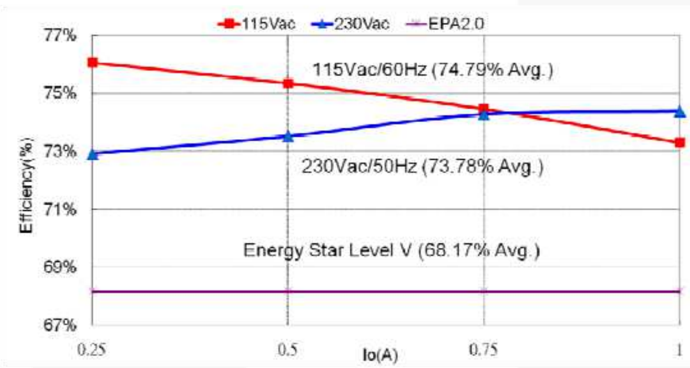
Noise from the current sense or the control signal can cause significant pulse-width jitter. While slope compensation helps alleviate these problems, further precautions should still be taken. Good placement and layout practices should be followed. Avoid long PCB traces and component leads. Locate bypass filter components near the PWM IC.

Typical Application Circuit (Flyback Charger)

Application	Fairchild Device	Input Voltage Range	Output
Cell Phone Charger	FAN302HLMY_F117	90~265 V_{AC}	5 V/1.2 A (6 W)

Features

- High Efficiency (>71% Avg.), Meets Energy Star V2.0 Standard (Avg. 68.17%)
- Ultra-Low Standby Power Consumption, <10 mW at 230 V_{AC} (Pin=6.3 mW for 115 V_{AC} and Pin=7.3 mW for 230 V_{AC})
- Output Regulation: CV= ±5%, CC= ±15%



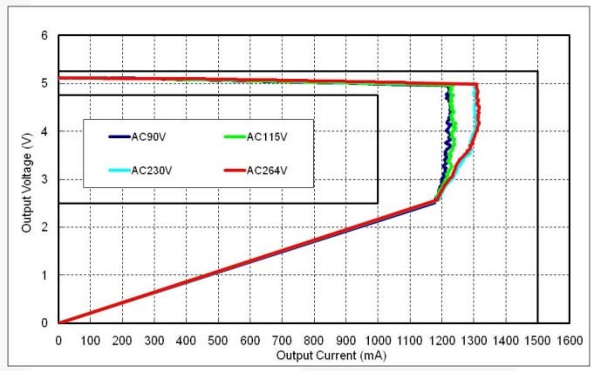


Figure 42. Measured Efficiency and Output Regulation

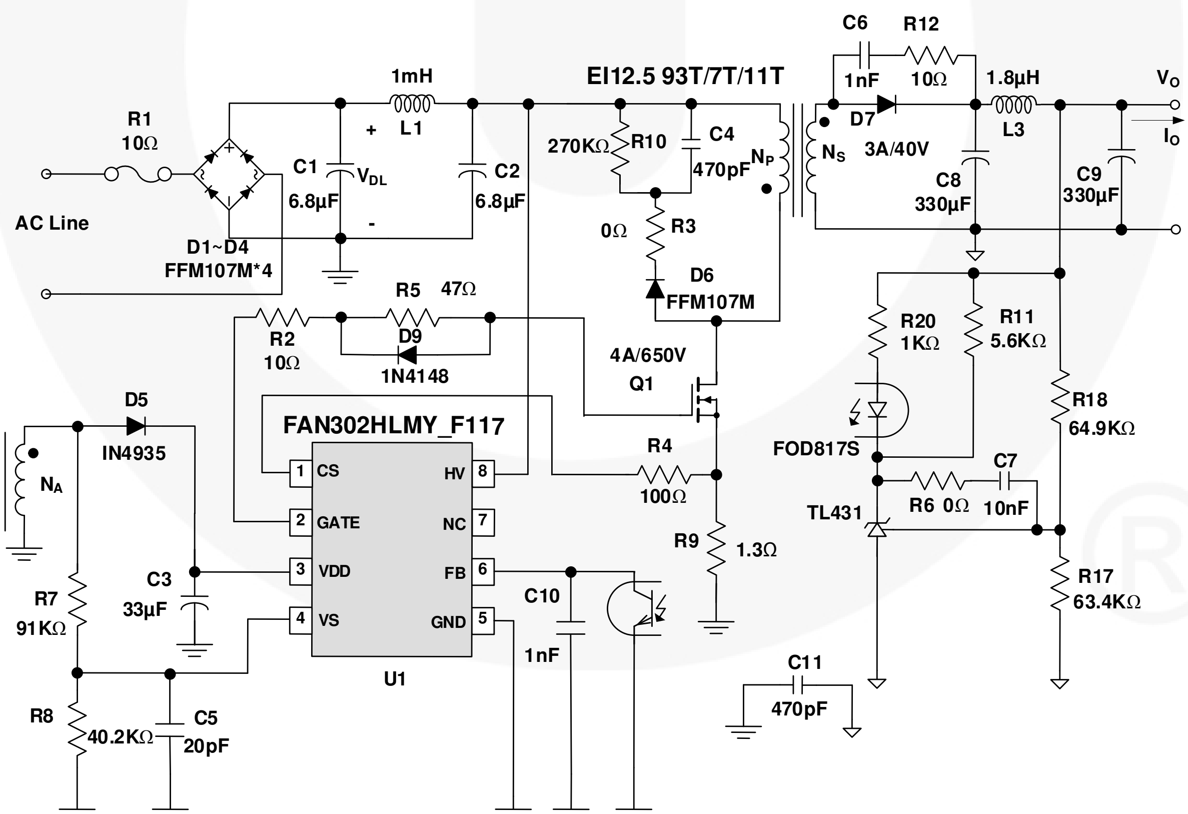


Figure 43.Schematic of Typical Application Circuit

Typical Application Circuit (Continued)

Transformer Specification

- Core: EI12.5
- Bobbin: EI12.5

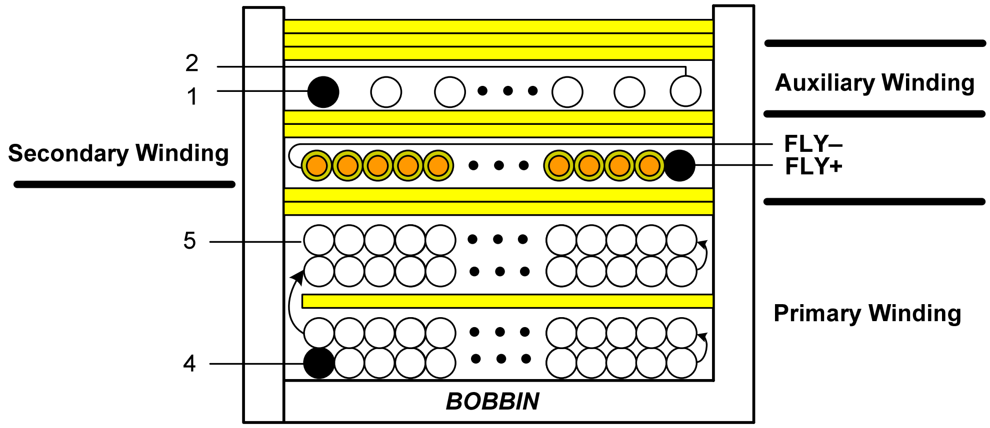


Figure 44.Transformer

Notes:

7. W1 consists of four layers with different number of turns. The number of turns of each layer is specified in Table 1. Add one insulation tape between the second and third layers.
8. W2 consists of two layers with triple-insulated wire. The leads of positive and negative fly lines are 3.5 cm and 2.5 cm, respectively.
9. W3 is space winding in one layer.

Table 1. Transformer Winding Specifications

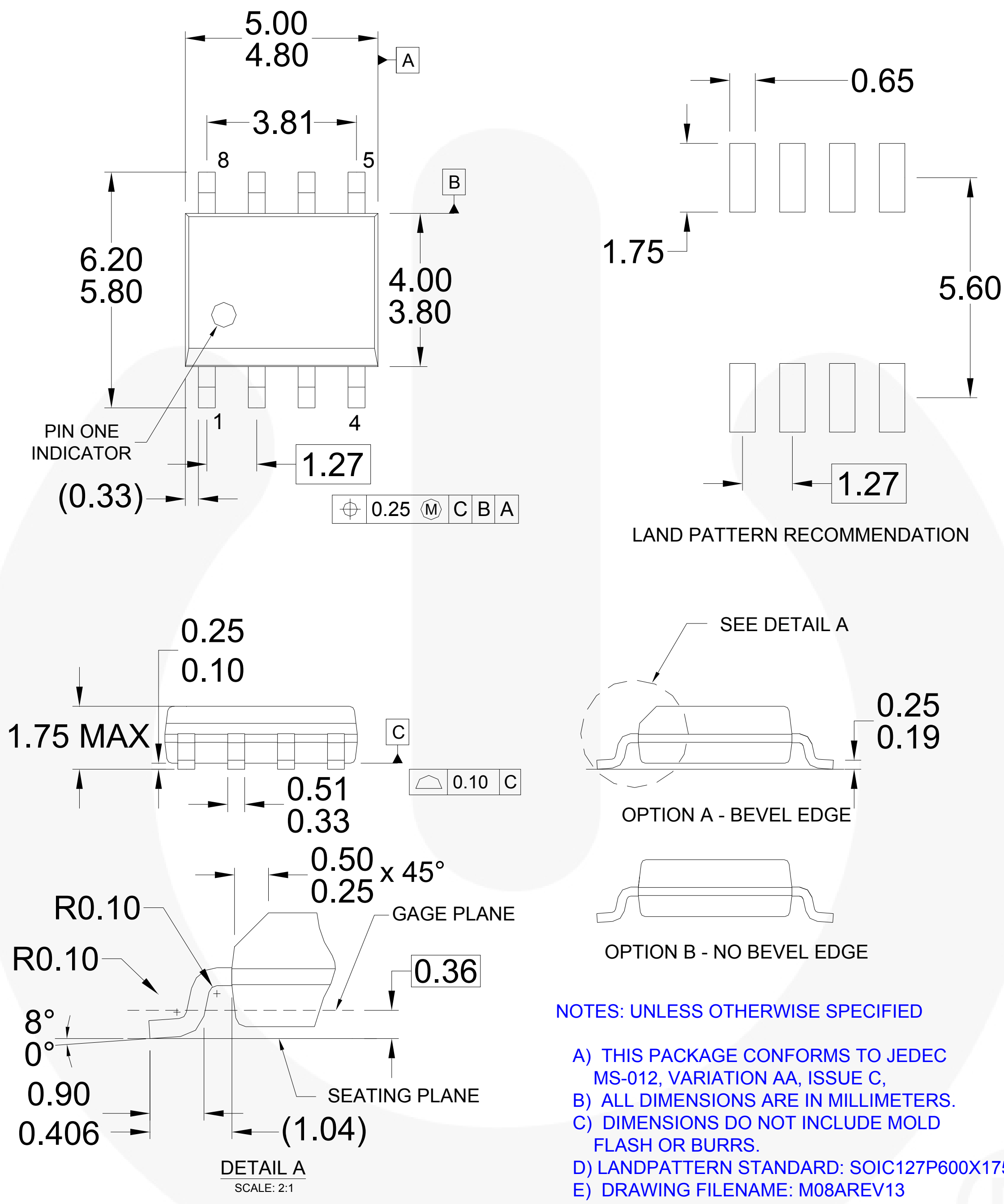
NO.	Terminal		Wire	Turns	Insulation
	Start Pin	End Pin			Turns
W1	4	5	2UEW 0.1*1	26	0
				25	1
				24	0
				18	2
W2	Fly+	Fly-	TEX-E 0.45*1	7	2
W3	1	2	2UEW 0.18*1	11	2
			Core Rounding Tape		3
			Core		0
W4	2		2UEW 0.18*1	5	2

Note:

10. W4 is the outermost and space winding.

	Pin	Specifications	Remark
Primary-Side Inductance	4－5	700 µH ±7%	100 kHz, 1 V
Primary-Side Leakage Inductance	4－5	130 µH ±7%	Short One of the Secondary-Side Windings

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 45. 8-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch, Narrow Body

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Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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