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FAN49103

2.5 A, 1.8 MHz, TinyPower™ I^2C Buck-Boost Regulator

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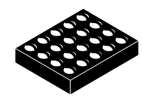
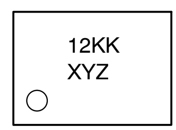


WLCSP20 2.015x1.615x0.586
CASE 567QK

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2−weeks Date Code
Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Description

The FAN49103 is a high efficiency buck−boost switching mode regulator which accepts input voltages either above or below the regulated output voltage. Using full− bridge architecture with synchronous rectification, the FAN49103 is capable of delivering up to 2.5 A while regulating the output at 3.4 V. The FAN49103 exhibits seamless transition between step−up and step−down modes reducing output disturbances. The output voltage and operation mode of the regulator can be programmed through an I^2C interface.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate the device in power−save mode to maintain high efficiency. In PFM mode, the part still exhibits excellent transient response during load steps. At moderate to heavier loads or Forced PWM mode, the regulator switches to PWM fixed−frequency control. While in PWM mode, the regulator operates at a nominal fixed frequency of 1.8 MHz, which allows for reduced external component values.

The FAN49103 is available in a 20−bump 1.615 mm x 2.15 mm with 0.4 mm pitch WLCSP.

Features

- 24 µA Typical PFM Quiescent Current
- Above 95% Efficiency
- Total Layout Area = 11.61 mm^2
- Input Voltage Range: 2.5 V to 5.5 V
- Maximum Continuous Load Current:
  - 3.0 A at V_{OUT} = 3.4 V, V_{IN} = 3.3 V
  - 2.5 A at V_{OUT} = 3.4 V, V_{IN} = 3.0 V
  - 2.0 A at V_{OUT} = 3.4 V, V_{IN} = 2.5 V
- I^2C Compatible Interface
- Programmable Output Voltage:
  - 2.8 V to 4.0 V in 25 mV Steps
- 1.8 MHz Fixed−Frequency Operation in PWM Mode
- Automatic / Seamless Step−up and Step−down Mode Transitions
- Forced PWM and Automatic PFM/PWM Mode Selection
- 0.5 µA Typical Shutdown Current
- Low Quiescent Current Pass−Through Mode
- Internal Soft−Start and Output Discharge
- Low Ripple and Excellent Transient Response
- Internally Set, Automatic Safety Protections (UVLO, OTP, SCP, OCP)
- Package: 20 Bump, 0.4 mm Pitch WLCSP

Applications

- Smart Phones
- Tablets, Netbooks, Ultra−Mobile PCs
- Portable Devices with Li−ion Battery
- 2G/3G/4G Power Amplifiers
- NFC Applications

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June, 2018 − Rev. 3
Publication Order Number:
FAN49103/D

ORDERING INFORMATION

Part Number	Default VOUT	Output Discharge	Temperature Range	Package	Packing Method	Device Marking
FAN49103AUC340X	3.4 V	Yes	−40 to 85°C	20−Ball (WLCSP)	Tape and Reel	FF
FAN49103AUC330X	3.3 V	Yes	−40 to 85°C	20−Ball (WLCSP)	Tape and Reel	KX

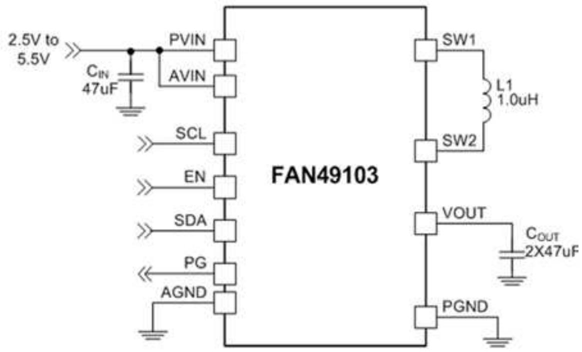

Figure 1. Typical Application

BLOCK DIAGRAM

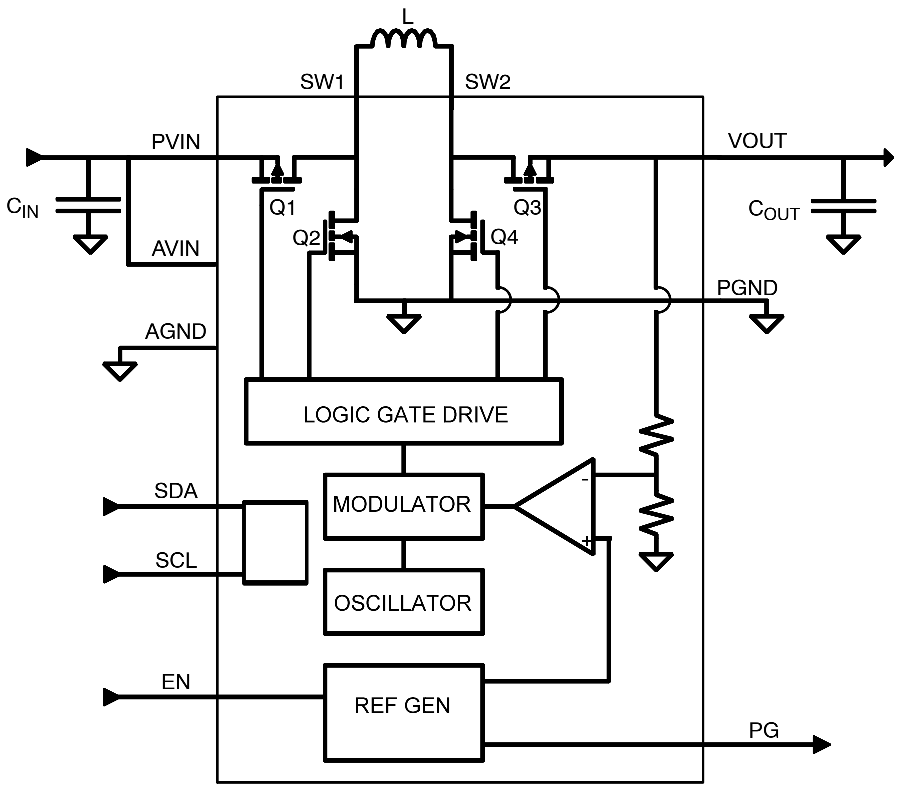

Figure 2. Block Diagram

PIN CONFIGURATION

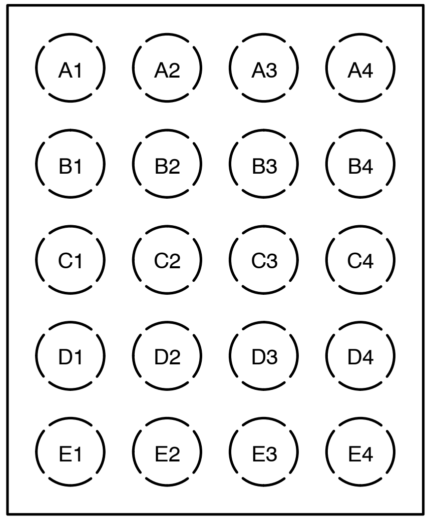

Figure 3. Top View (Bump Down)

PIN DEFINITIONS

Pin #	Name	Description
A3, A4	PVIN	**Power Input Voltage.** Connect to input power source. Connect to C_{IN} with minimal path
A1	AVIN	**Analog Input Voltage.** Analog input for device. Connect to C_{IN} and PVIN
A2	EN	**Enable.** A HIGH logic level on this pin forces the device to be enabled. A LOW logic level forces the device into shutdown. EN pin can be tied to VIN or driven via a GPIO logic voltage
B3, B4	SW1	**Switching Node 1.** Connect to inductor L1
E1	AGND	**Analog Ground.** Control block signal is referenced to this pin. Short AGND to PGND at GND pad of C_{OUT}.
B1, C1, C2, C3, C4, D1	PGND	**Power Ground.** Low−side MOSFET of buck and main MOSFET of boost are referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins
D2	SDA	**I²C Data Line.** Used for I²C communication
D3, D4	SW2	**Switching Node 2.** Connect to inductor L1
E2	PG	**Power Good.** This is an open−drain output and normally High Z. An external pull−up resistor from VOUT can be used to generate a logic HIGH. PG is pulled LOW if output falls out of regulation due to current overload or if thermal protection threshold is exceeded. If EN is LOW, PG is high impedance
B2	SCL	**I²C Clock Line.** Used for I²C communication
E3, E4	VOUT	**Output Voltage.** Buck−Boost Output. Connect to output load and C_{OUT}

1. Refer to Layout Recommendation section located near the end of the datasheet.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter		Min.	Max.	Unit
PVIN/AVIN	PVIN/AVIN Voltage		−0.3	6.5	V
VOUT	VOUT Voltage		−0.3	6.5	V
SW1, SW2	SW Nodes Voltage		−0.3	7.0	V
	Other Pins		−0.3	6.5	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22−A114	2000		V
		Charged Device Model per JESD22−C101	1000		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
PVIN	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current (Note 2)	0		2.5	A
L	Inductor (Note 5)		1.0		μH
C_{IN}	Input Capacitance (Notes 2, 3, 4, 5)	2	47		μF
C_{OUT}	Output Capacitance (Notes 2, 3, 4, 5)	17	47		μF
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Depends on input and output voltages. Thermal properties of the device should be taken into consideration; refer to Thermal Consideration in the Application Information section.
3. Typical value reflects the capacitor value needed to meet minimum requirement. Minimum passive component values indicate effective capacitance which includes temperature, voltage de−rating, tolerance, and stability.
4. Output capacitance affects load transient response and loop phase margin; see Application Information section.
5. Refer to Additional Application Information section.

THERMAL PROPERTIES

Symbol	Parameter	Min.	Typ.	Max.	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance (Note 7)		66		°C/W

6. Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four− layer 2s2p with vias JEDEC class boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.
7. See Thermal Considerations in the Application Information section.

ELECTRICAL CHARACTERISTICS Minimum and maximum values are at PVIN = AVIN = 2.5 V to 5.5 V, T_A = −40°C to +85°C. Typical values are at T_A = 25°C, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V. (Note 9)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
I_Q	Quiescent Current	PFM Mode, I_{OUT} = 0 mA (Note 10)		24		μA
		PT Mode, I_{OUT} = 0 mA		27		
I_{SD}	Shutdown Supply Current	EN = GND, PVIN = 3.6 V		0.5	5.0	μA
V_{UVLO}	Under−Voltage Lockout Threshold	Falling PVIN	1.95	2.00	2.05	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			200		mV
EN, SDA, SCL						
V_{IH}	HIGH Level Input Voltage		1.1			V
V_{IL}	LOW Level Input Voltage				0.4	V
I_{IN}	Input Bias Current Into Pin	Input Tied to GND or PVIN		0.01	1.00	μA
PG						
V_{PG}	PG LOW	I_{PG} = 5 mA			0.4	V
I_{PG_LK}	PG Leakage Current	V_{PG} = 5 V			1	μA
SWITCHING						
f_{SW}	Switching Frequency	PVIN = 3.6 V, T_A = 25°C	1.6	1.8	2.0	MHz
I_{p_LIM}	Peak PMOS Current Limit	PVIN = 3.6 V	4.6	5.2	5.9	A
ACCURACY						
V_{OUT_ACC}	DC Output Voltage Accuracy	PVIN = 3.6 V, Forced PWM, I_{OUT} = 0 mA, VOUT = 3.4 V	3.366	3.400	3.434	V
		PVIN = 3.6 V, PFM Mode, I_{OUT} = 0 mA, VOUT = 3.4 V	3.366	3.475	3.563	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Refer to Typical Characteristics waveforms/graphs for Closed−Loop data and its variation with input voltage and ambient temperature. Electrical Characteristics reflects Open−Loop steady state data. System Characteristics reflects both steady state and dynamic Close−Loop data associated with the recommended external components.
9. Minimum and Maximum limits are verified by design, test, or statistical analysis. Typical (Typ.) values are not tested, but represent the parametric norm.
10. Device is not switching.

SYSTEM CHARACTERISTICS The following table is verified by design and bench test while using circuit of Figure 1 with the following external components: L = 1.0 μH, DFE201612E−1R0M (TOKO), C_{IN} = 47 μF, C_{OUT} = 2 x 47 μF, 0603 (1608 metric) CL10A476MQ8NZNE (SEMCO). Typical values are at T_A = 25°C, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V. These parameters are not verified in production.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{OUT_ACC}	Total Accuracy (Includes DC accuracy and load transient) (Note 11)			±5		%
ΔV_{OUT}	Load Regulation	I_{OUT} = 0.4 A to 2.5 A, PVIN = 3.6 V		−0.20		%/A
ΔV_{OUT}	Line Regulation	3.0 V ≤ PVIN ≤ 4.2 V, I_{OUT} = 1.5 A		−0.06		%/V
V_{OUT_RIPPLE}	Ripple Voltage	PVIN = 4.2 V, VOUT = 3.4 V, I_{OUT} = 1 A, PWM Mode		4		mV
		PVIN = 3.6 V, VOUT = 3.4 V, I_{OUT} = 100 mA, PFM Mode		22		
		PVIN = 3.0 V, VOUT = 3.4 V, I_{OUT} = 1 A, PWM Mode		14		
η	Efficiency	PVIN = 3.0 V, VOUT = 3.4 V, I_{OUT} = 50 mA, PFM		90		%
		PVIN = 3.0 V, VOUT = 3.4 V, I_{OUT} = 500 mA, PWM		96		
		PVIN = 3.8 V, VOUT = 3.4 V, I_{OUT} = 50 mA, PFM		90		
		PVIN = 3.8 V, VOUT = 3.4 V, I_{OUT} = 600 mA, PWM		94		
		PVIN = 3.4 V, VOUT = 3.4 V, I_{OUT} = 300 mA, PWM		94		
T_{SS}	Soft−Start	EN HIGH to 95% of Target VOUT, I_{OUT} = 68 mA		260		μs
ΔV_{OUT_LOAD}	Load Transient	PVIN = 3.4 V, I_{OUT} = 0.5 A ⇔ 1 A, TR = TF = 1 μs		±45		mV
		PVIN = 3.4 V, I_{OUT} = 0.5 A ⇔2.0 A, TR = TF = 1 μs, Pulse Width = 577 μs		±125		
ΔV_{OUT_LINE}	Line Transient	PVIN = 3.0 V ⇔ 3.6 V, TR = TF = 10 μs, I_{OUT} = 1 A		±60		mV

11. Load transient is from 0.5 A ⇔1 A.

TYPICAL CHARACTERISTICS

Unless otherwise noted, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V, L = 1.0 μH, DFE201612E−1R0M (TOKO), C_{IN} = 47 μF, C_{OUT} = 2 × 47 μF, 0603 (1608 metric) CL10A476MQ8NZNE (SEMCO), AUTO Mode, T_A = 25°C.

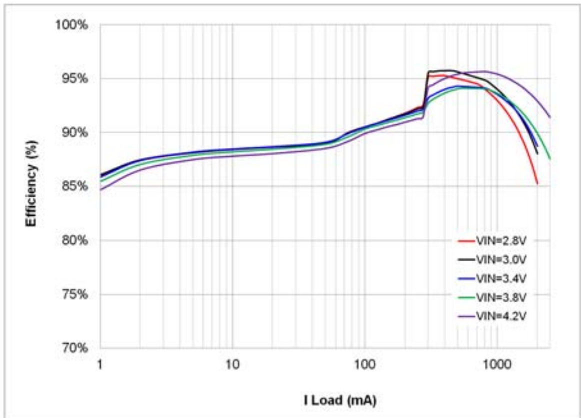

Figure 4. Efficiency vs. Load

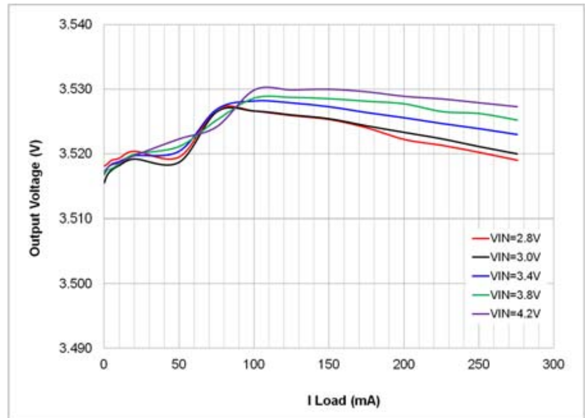

Figure 5. Output Regulation vs. Load

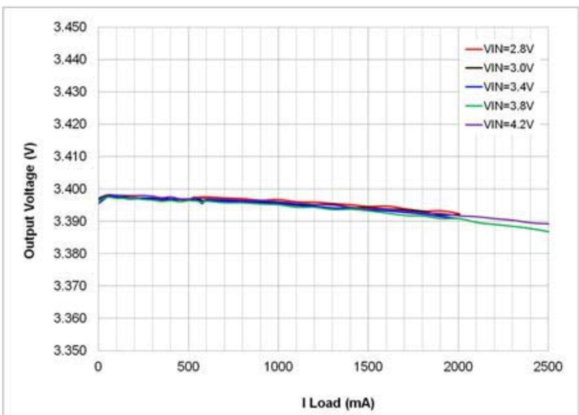

Figure 6. Output Regulation vs. Load, FPWM Mode

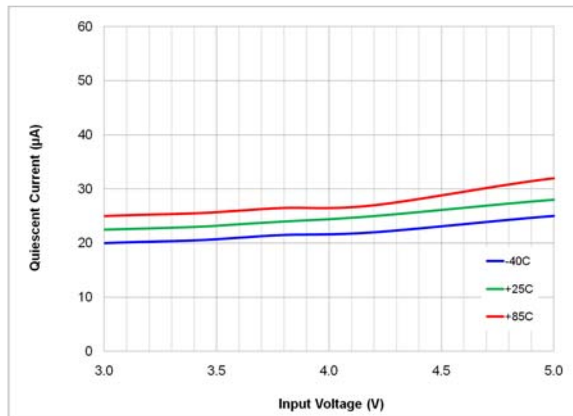

Figure 7. Quiescent Current (No Switching) vs. Input Voltage

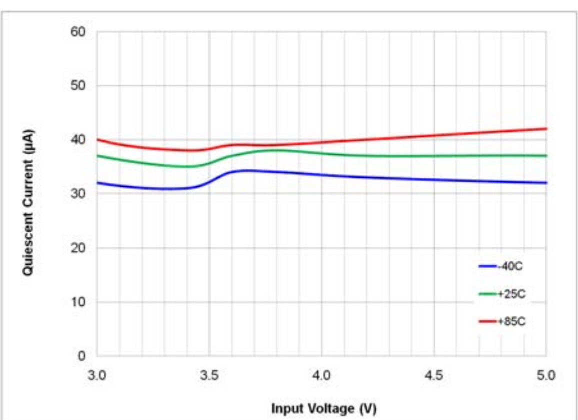

Figure 8. Quiescent Current (Switching) vs. Input Voltage

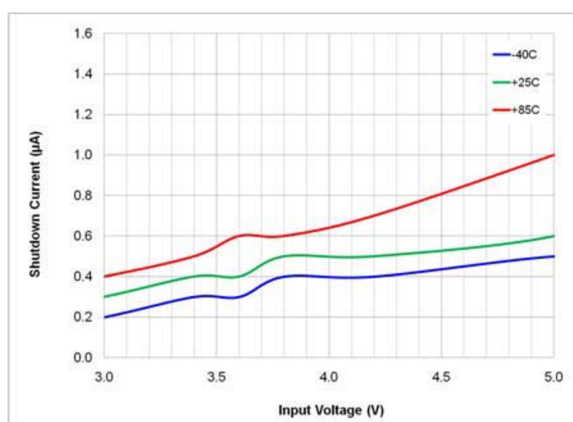

Figure 9. Shutdown Current vs. Input Voltage

TYPICAL CHARACTERISTICS

Unless otherwise noted, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V, L = 1.0 μH, DFE201612E−1R0M (TOKO), C_{IN} = 47 μF, C_{OUT} = 2 × 47 μF, 0603 (1608 metric) CL10A476MQ8NZNE (SEMCO), AUTO Mode, T_A = 25°C.

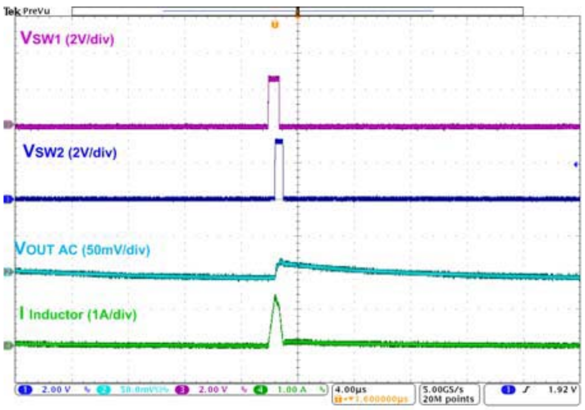

Figure 10. Output Ripple, VIN = 2.8 V, I_{OUT} = 20 mA, Boost Operation

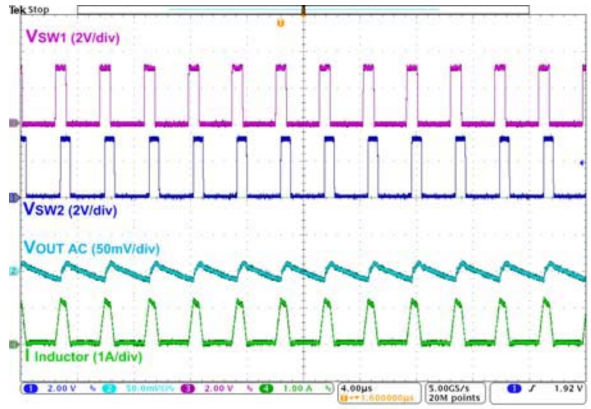

Figure 11. Output Ripple, VIN = 3.3 V, I_{OUT} = 200 mA, Buck−Boost Operation

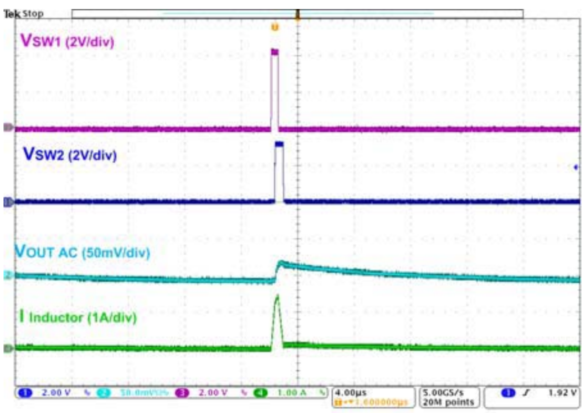

Figure 12. Output Ripple, VIN = 4.2 V, I_{OUT} = 20 mA, Buck Operation

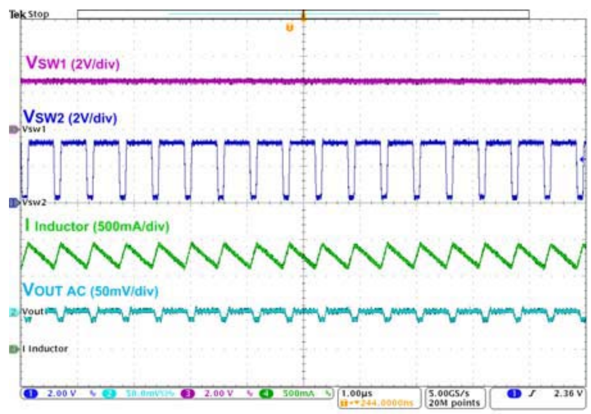

Figure 13. Output Ripple, VIN = 2.5 V, I_{OUT} = 1000 mA, Boost Operation

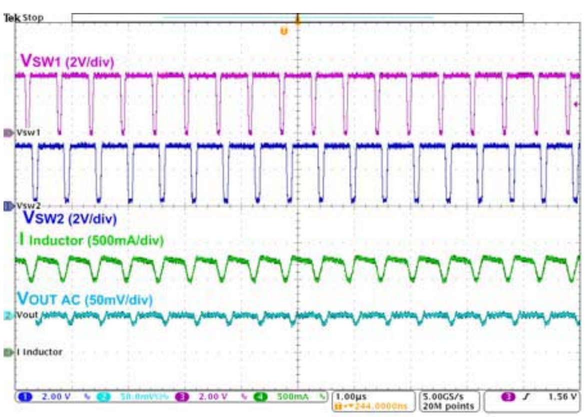

Figure 14. Output Ripple, VIN = 3.3 V, I_{OUT} = 1000 mA, Buck−Boost Operation

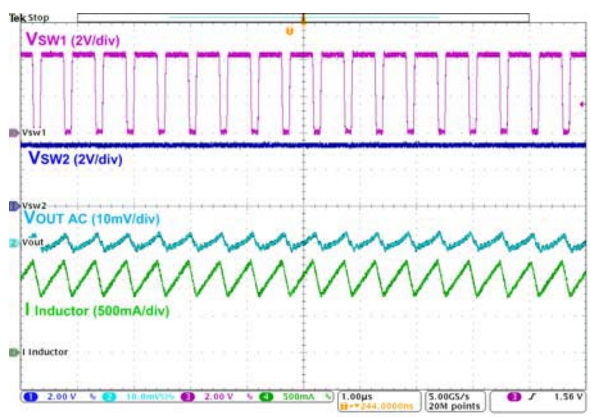

Figure 15. Output Ripple, VIN = 4.5 V, I_{OUT} = 1000 mA, Buck Operation

TYPICAL CHARACTERISTICS

Unless otherwise noted, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V, L = 1.0 μH, DFE201612E−1R0M (TOKO), C_{IN} = 47 μF, C_{OUT} = 2 × 47 μF, 0603 (1608 metric) CL10A476MQ8NZNE (SEMCO), AUTO Mode, T_A = 25°C.

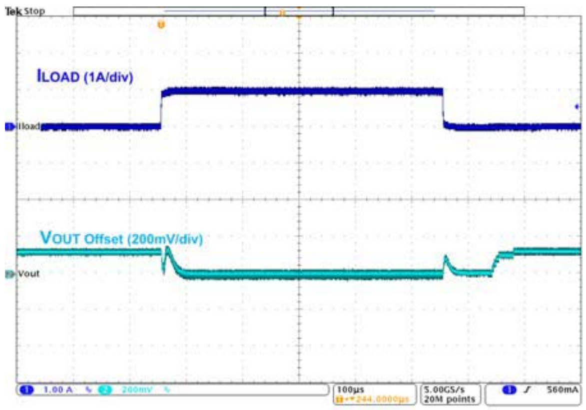

Figure 16. Load Transient, 0 mA ⇔ 1000 mA, 1 ms Edge, VIN = 3.60 V

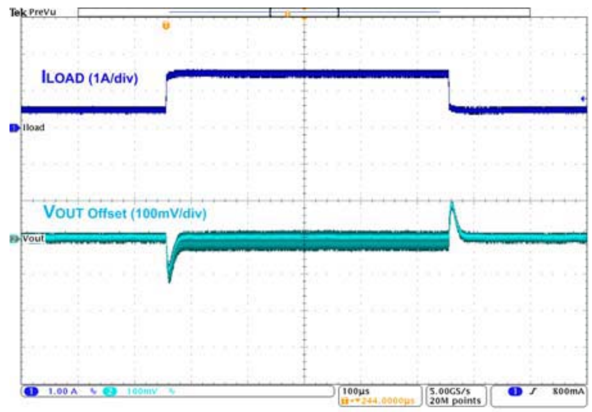

Figure 17. Load Transient, 500 mA ⇔ 1500 mA, 1 ms Edge, VIN = 3.60 V

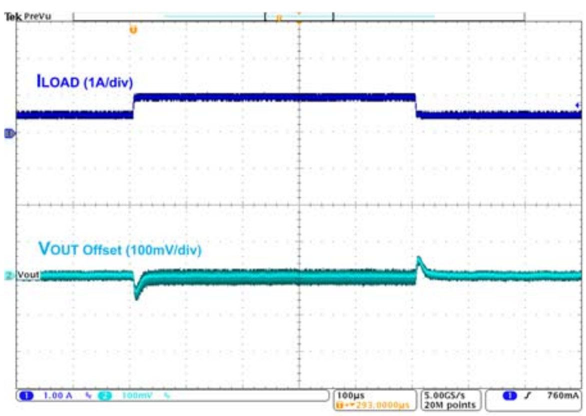

Figure 18. Load Transient, 500 mA ⇔ 1000 mA, 1 ms Edge, VIN = 3.40 V

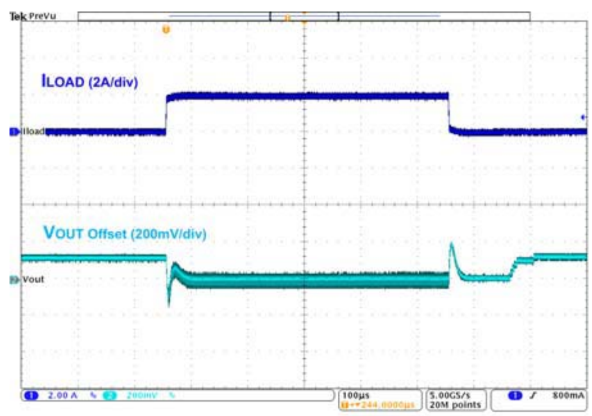

Figure 19. Load Transient, 0 mA ⇔ 2000 mA, 1 ms Edge, VIN = 3.60 V

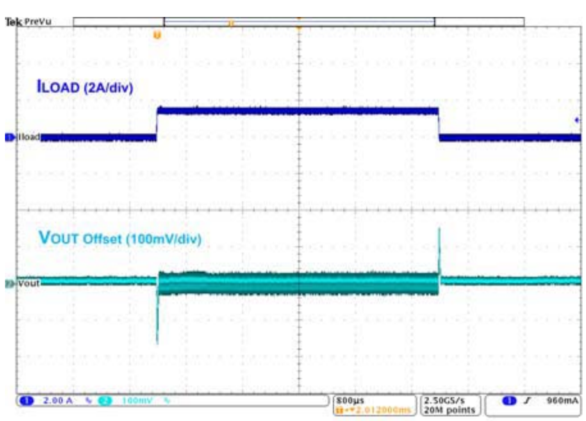

Figure 20. Load Transient, 0 mA ⇔ 1500 mA, 10 ms Edge, VIN = 2.80 V, PWM Mode

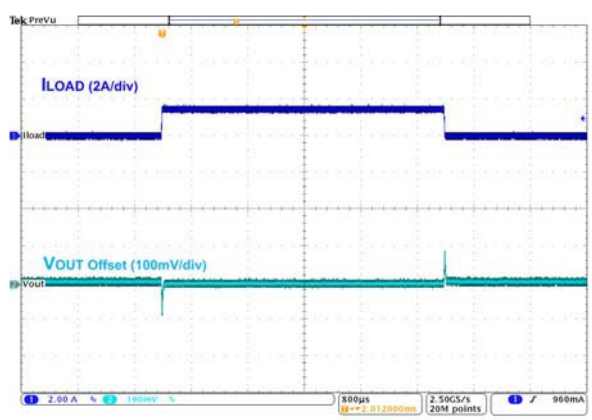

Figure 21. Load Transient, 0 mA ⇔ 1500 mA, 10 ms Edge, VIN = 4.20 V, PWM Mode

TYPICAL CHARACTERISTICS

Unless otherwise noted, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V, L = 1.0 μH, DFE201612E−1R0M (TOKO), C_{IN} = 47 μF, C_{OUT} = 2 × 47 μF, 0603 (1608 metric) CL10A476MQ8NZNE (SEMCO), AUTO Mode, T_A = 25°C.

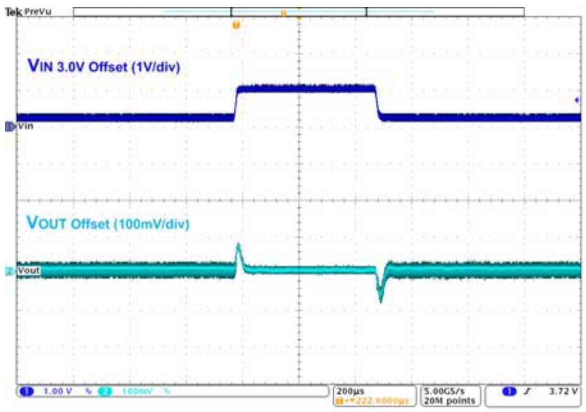

Figure 22. Line Transient, 3.2 ⇔ 4.0 VIN, 10 ms Edge, 1000 mA Load

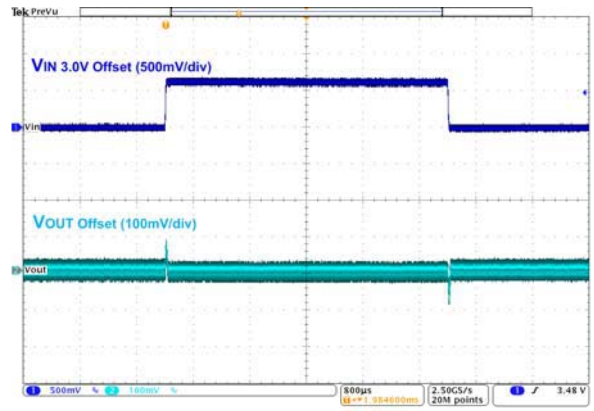

Figure 23. Line Transient, 3.0 ⇔ 3.6 VIN, 10 ms Edge, 1500 mA Load, PWM

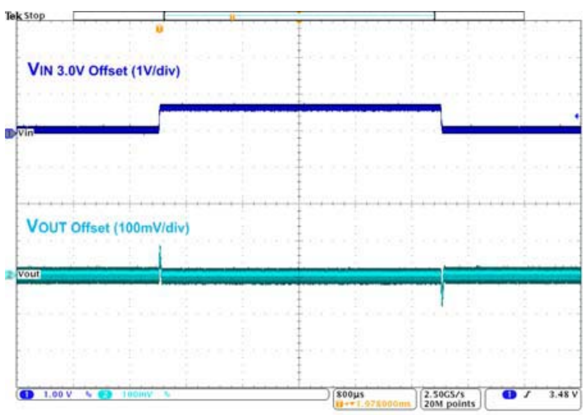

Figure 24. Line Transient, 3.0 ⇔ 3.6 VIN, 10 ms Edge, 1000 mA Load, PWM

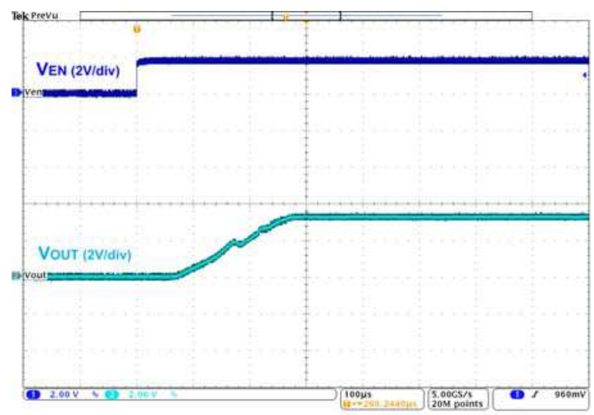

Figure 25. Startup, VIN = 3.6 V, I_{OUT} = 0 mA

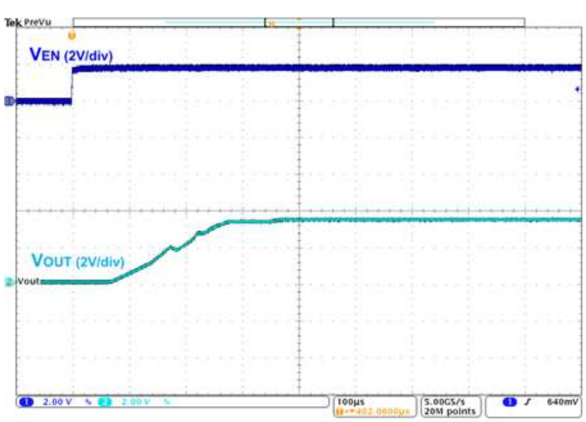

Figure 26. Startup, VIN = 3.6 V, I_{OUT} = 68 mA

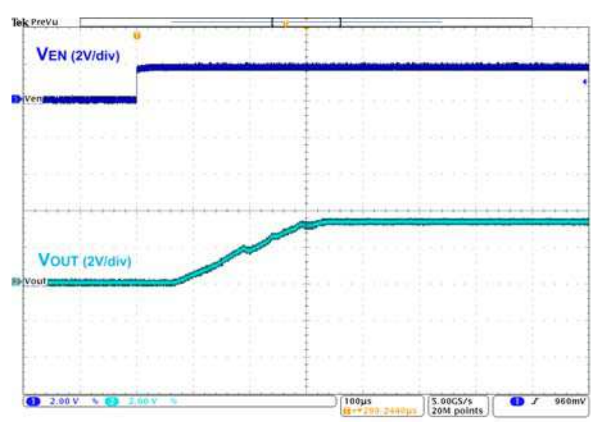

Figure 27. Startup, VIN = 3.6 V, I_{OUT} = 1000 mA

TYPICAL CHARACTERISTICS

Unless otherwise noted, PVIN = AVIN = V_{EN} = 3.6 V, VOUT = 3.4 V, L = 1.0 μH, DFE201612E−1R0M (TOKO), C_{IN} = 47 μF, C_{OUT} = 2 × 47 μF, 0603 (1608 metric) CL10A476MQ8NZNE (SEMCO), AUTO Mode, T_A = 25°C.

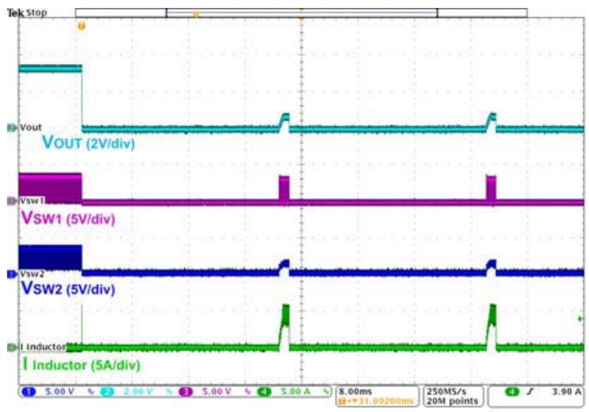

Figure 28. Short−Circuit Protection

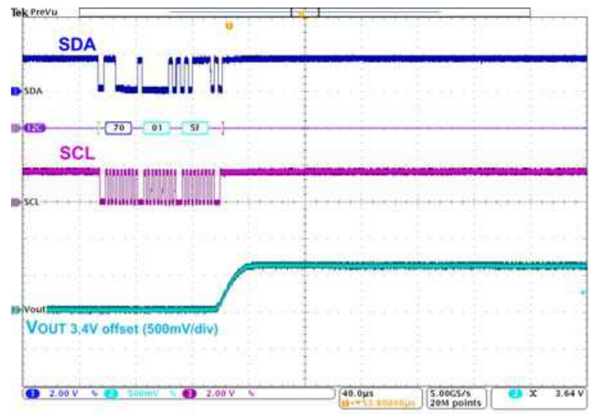

Figure 29. V_{OUT} Transition, 3.4 V ⇔ 4.0 V, 500 mA Load

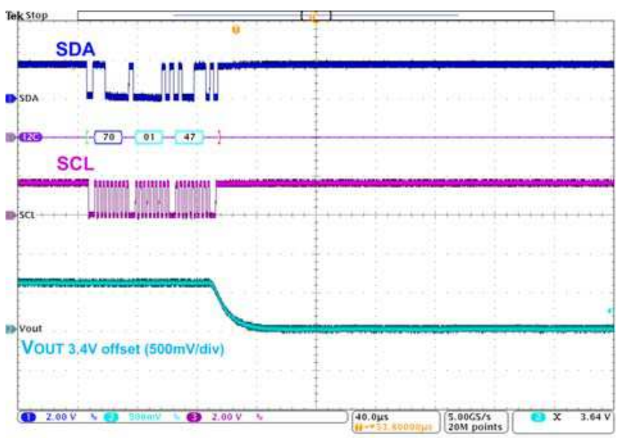

Figure 30. V_{OUT} Transition, 4.0 V ⇔ 3.4 V, 500 mA Load

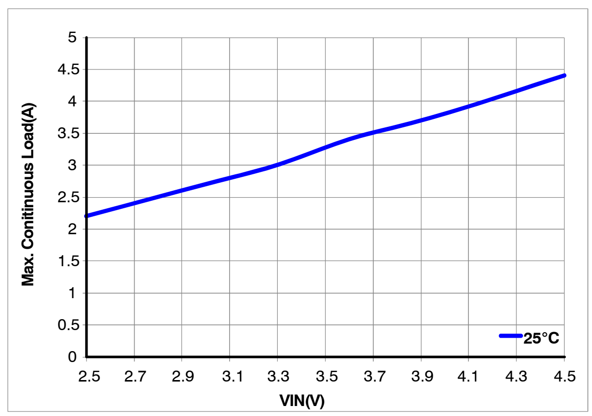

Figure 31. Typical Maximum Continuous Load vs. Input Voltage, V_{OUT}= 3.4 V, 25°C

APPLICATION INFORMATION

Functional Description

FAN49103 is a fully integrated synchronous, full bridge DC−DC converter that can operate in buck operation (during high PVIN), boost operation (for low PVIN) and a combination of buck−boost operation when PVIN is close to the target VOUT value. The PWM/PFM controller switches automatically and seamlessly between buck, buck−boost and boost modes.

The FAN49103 uses a four−switch operation during each switching period when in the buck−boost mode. Mode operation is as follows: referring to the power drive stage shown in Figure 32 if PVIN is greater than target VOUT, then the converter is in buck mode: Q3 is ON and Q4 is OFF continuously leaving Q1, Q2 to operate as a current−mode controlled PWM converter. If PVIN is lower than target VOUT then the converter is in boost mode with Q1 ON and Q2 OFF continuously, while leaving Q3, Q4 to operate as a current−mode boost converter. When PVIN is near VOUT, the converter goes into a 3−phase operation in which combines a buck phase, a boost phase and a reset phase; all switches are switching to maintain an average inductor volt−second balance.

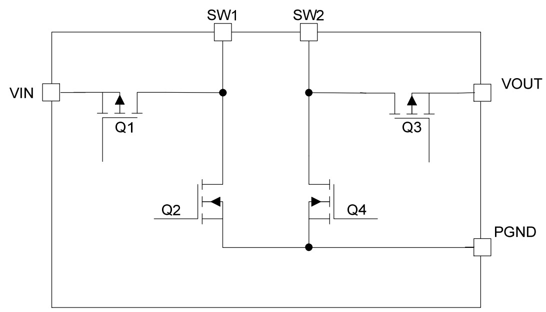

Figure 32. Simplified Block Diagram

PFM/PWM Mode

The FAN49103 uses a current−mode modulator to achieve smooth transitions between PWM and PFM operation. In Pulsed Frequency Modulation (PFM), frequency is reduced to maintain high efficiency. During PFM operation, the converter positions the output voltage typically 75 mV higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. As the load increased from light loads, the converter enters PWM operation typically at 300 mA of current load. The converter switching frequency is typically 1.8 MHz during PWM operation for moderate to heavy load currents.

PT (Pass−Through) Mode

In Pass−Through mode, all of the switches are not switching and VOUT tracks PVIN (VOUT = PVIN − I_{OUT} × ($Q1_{RDSON}$ + $Q3_{RDSON}$ +L_{DCR}). In PT mode only Over−Temperature (OTP) and Under Voltage Lockout (UVLO) protection circuits are activated. There is no Over− Current Protection (OCP) in PT mode.

Shutdown and Startup

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. During shutdown, VOUT is isolated from PVIN. Raising EN pin activates the device and begins the soft− start cycle. During soft−start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. If VOUT fails to reach target VOUT value after 1 ms, a FAULT condition is declared.

Over−Temperature (OTP)

The regulator shuts down when the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

Output Discharge

When the regulator is disabled and driving the EN pin LOW, a 230 Ω internal resistor is activated between VOUT and GND. The Output Discharge is not activated during a FAULT state condition.

Over−Current Protection (OCP)

If the peak current limit is activated for a typical 700 μs, a FAULT state is generated, so that the IC protects itself as well as external components and load.

FAULT State

The regulator enters the FAULT state under any of the following conditions:

- VOUT fails to achieve the voltage required after soft−start
- Peak current limit triggers
- OTP or UVLO are triggered

Once a FAULT is triggered, the regulator stops switching and presents a high−impedance path between PVIN and VOUT. After waiting 30 ms, a restart is attempted.

Power Good

PG, an open−drain output, is LOW during FAULT state and HIGH for Power Good.

The PG pin is provided for signaling the system when the regulator has successfully completed soft−start and no FAULTs have occurred. PG pin also functions as a warning flag for high die temperature and overload conditions.

- PG is released HIGH when the soft−start sequence is successfully completed
- PG is pulled LOW when a FAULT is declared. Any FAULT condition causes PG to be de−asserted

Thermal Considerations

For best performance, the die temperature and the power dissipated should be kept at moderate values. The maximum power dissipated can be evaluated based on the following relationship:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\Theta_{JA}} \right\}$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die; T_A is the ambient operating temperature; and θ_{JA} is dependent on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground.

The addition of backside copper with through−holes, stiffeners, and other enhancements can help reduce θ_{JA}. The heat contributed by the dissipation of devices nearby must be included in design considerations. Following the layout recommendation may lower the θ_{JA}.

I²C Interface

The FAN49103's serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I²C−Bus specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is E0.

Table 1. I²C SLAVE ADDRESS

Hex	Bits							
	7	6	5	4	3	2	1	0
E0	1	1	1	0	0	0	0	R/$\overline{W}$

Bus Timing

As shown in Figure 33, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the

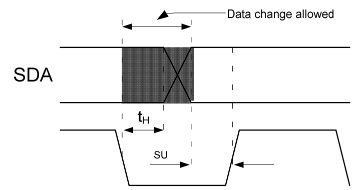

Figure 33. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 34.

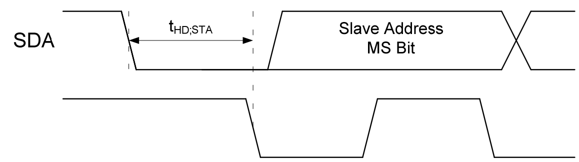

Figure 34. START Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 35.

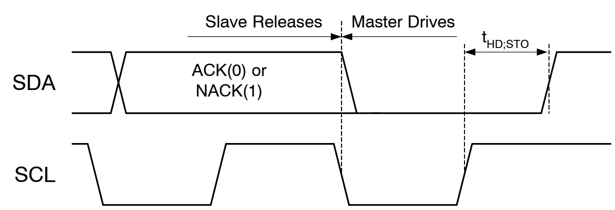

Figure 35. STOP Bit

During a read from the FAN49103, the master issues a REPEATED START after sending the register address, and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 36.

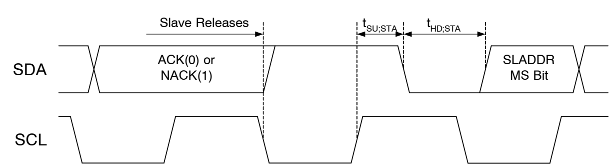

Figure 36. REPEATED START Bit

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical; except the bus speed for HS mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 34) that causes all slaves on the bus to switch to HS Mode. The master then sends I2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 35) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 36).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as

Master Drives Bus

and

Slave Drives Bus.

All addresses and data are MSB first.

Table 2. I²C BIT DEFINITIONS FOR FIGURE 37 & FIGURE 38

Symbol	Definition
R	REPEATED START, see Figure 36
P	STOP, see Figure 35
S	START, see Figure 34
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet
A	NACK. The slave sends a 1 to NACK the preceding packet
R	REPEATED START, see Figure 36
P	STOP, see Figure 35

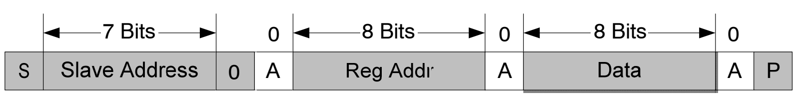

Figure 37. Write Transaction

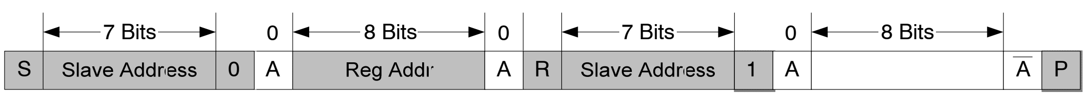

Figure 38. Read Transaction

Register Description

Table 3. REGISTER TABLE

Hex Address	Name	Function
00	SOFT−RESET	Resets all registers to default values
01	VOUT_REF	Set the target regulation point of VOUT
02	CONTROL	PT and MODE control
40	Manufacturer_ID	Read−only register identifies vendor and device type
41	Device_ID	Read−only register identifies die ID

BIT DEFINITIONS

The following table defines the operation of each register bit. **Bold** indicates power−on default values.

Bit	Name	Value	Description
SOFT−RESET W			**REGISTER ADDRESS: 00**
7:1	Reserved	**0000000**	
0	Soft_reset	**0**	Write 1 to reset all registers.
VOUT_REF R/W			**REGISTER ADDRESS: 01**
7	Reserved	**0**	
6:0	Ref_dac_code	**1000111**	Sets the target regulation point for VOUT.

HEX	VOUT	HEX	VOUT
00 – 2E	Reserved	47	3.400
2F	2.800	48	3.425
30	2.825	49	3.450
31	2.850	4A	3.475
32	2.875	4B	3.500
33	2.900	4C	3.525
34	2.925	4D	3.550
35	2.950	4E	3.575
36	2.975	4F	3.600
37	3.000	50	3.625
38	3.025	51	3.650
39	3.050	52	3.675
3A	3.075	53	3.700
3B	3.100	54	3.725
3C	3.125	55	3.750
3D	3.150	56	3.775
3E	3.175	57	3.800
3F	3.200	58	3.825
40	3.225	59	3.850
41	3.250	5A	3.875
42	3.275	5B	3.900
43	3.300	5C	3.925
44	3.325	5D	3.950
45	3.350	5E	3.975
46	3.375	5F	4
		60 – 7F	Reserved

Bit	Name	Value	Description
CONTROL R/W			**REGISTER ADDRESS: 02**
7:4	Reserved	**0000**	
3	i2c_pt_in	**0**	Enables Pass−Through mode. Code / Mode 0 – Regulated output (Boost, Buck or Buck−Boost) 1 – Pass−Through enabled
2	i2c_mode_in	**0**	Enables Forced PWM mode, as long as Pass−Through is not enabled. Code / Mode 0 – Auto PWM − PFM mode based on load 1 – Forced PWM mode enabled
1:0	Reserved	**00**	
MANUFACTURER_ID R			**REGISTER ADDRESS: 40**
7:0	Manufacture_ID	**10000011**	
DEVICE_ID R			**REGISTER ADDRESS: 41**
7:0	Device_ID	**00000110**	

ADDITIONAL APPLICATION INFORMATION

Table 4. RECOMMENDED CAPACITORS

Capacitor	Part Number	Vendor	Value	Case Size	Rating
C_{IN}	CL10A476MQ8NZNE	SEMCO	47 μF	0603 (1608 Metric)	6.3 V
C_{OUT}	CL10A476MQ8NZNE	SEMCO	2 × 47 μF	0603 (1608 Metric)	6.3 V

Output Capacitance (C_{OUT}) and Input Capacitance (C_{IN}) Stability

The effective capacitance (C_{EFF}) of small, high−value, ceramic capacitors will decrease as bias voltage increases. FAN49103 is guaranteed for stable operation with the minimum value of 17 μF ($C_{EFF(MIN)}$) output capacitance when using a 1 μH value inductor and a minimum value of 13 μF ($C_{EFF(MIN)}$) output capacitance when using a 0.47 μH value inductor. Furthermore, FAN49103 is guaranteed for stable operation with the minimum value of 2 μF ($C_{EFF(MIN)}$) input capacitance. De−rating factors should be taken into consideration to ensure selected components meet minimum requirement.

Table 5. MINIMUM C_{EFF} (Note 12) REQUIRED FOR STABILITY

VOUT (V)	I_{LOAD} (A)	Inductor Value	$C_{EFF(MIN)}$
3.3 V, 3.4 V	0 – 2.5 A	1.0 μH	17 μF
3.3 V, 3.4 V	0 – 2.5 A	0.47 μH	13 μF

12. C_{EFF} is defined as the capacitance value during operating conditions and not the capacitor value. A capacitor varies with manufacturer, material, case size, voltage rating and temperature.

Inductor Selection

Recommended nominal inductance value is 1.0 μH. An inductor value of 0.47 μH can be used but higher peak currents could lead to lower efficiency; however, transient response performance may be improved. FAN49103 employs peak current limiting and the peak inductor current can reach typically 5.2 A for a short duration during overload conditions. Therefore, current saturation value should be taken into consideration when choosing an inductor.

Table 6. RECOMMENDED INDUCTORS

Part Number	Vendor	Value	Dimension	Isat	DCR
DFE201610E1R0M	TOKO	1.0 μH	2.0 mm × 1.6 mm × 1.0 mm	3.9 A	48 mΩ
DFE201612E1R0M			2.0 mm × 1.6 mm × 1.2 mm	4.4 A	40 mΩ
DFE201610ER47M		0.47 μH (Note 13) (Optional)	2.0 mm × 1.6 mm × 1.0 mm	5.3 A	26 mΩ
DFE201612ER47M			2.0 mm × 1.6 mm × 1.2 mm	6.1 A	20 mΩ

13. When using 0.47 μH inductor value, one 47 μF (CL10A476MQ8NZNE) capacitor can be used at the output of the regulator.

LAYOUT RECOMMENDATIONS

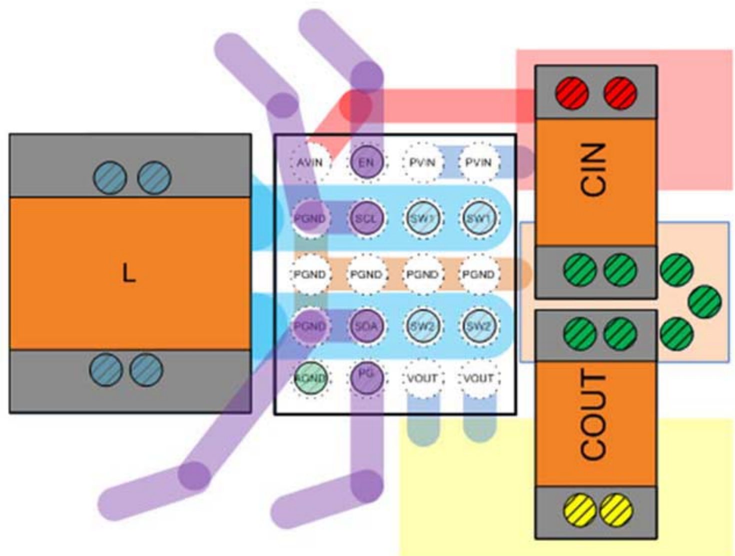

Figure 39. Component Placement and Routing for FAN49103

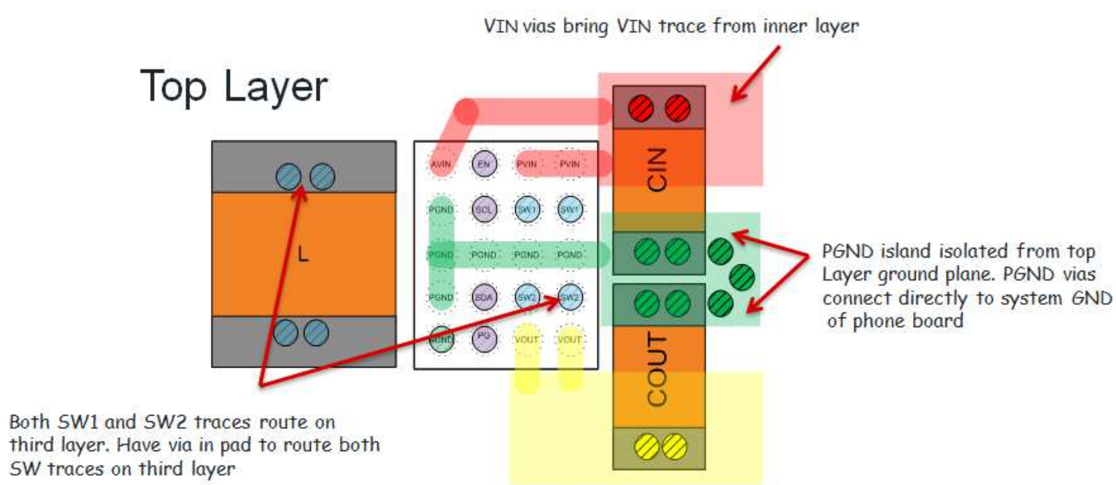

Figure 40. Top Layer Routing for FAN49103

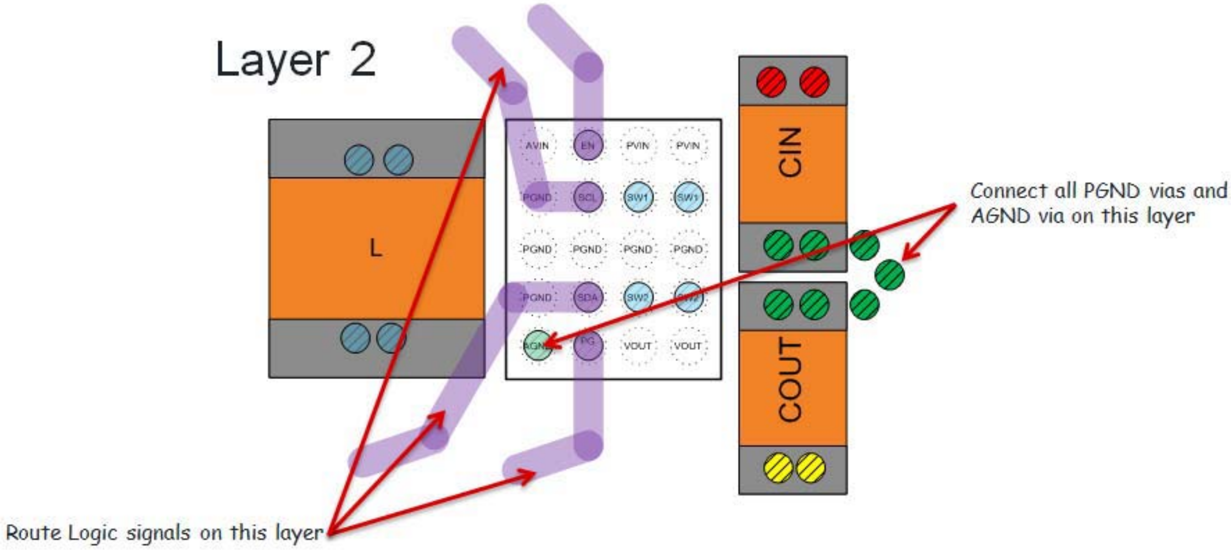

Figure 41. Layer 2 Routing for FAN49103

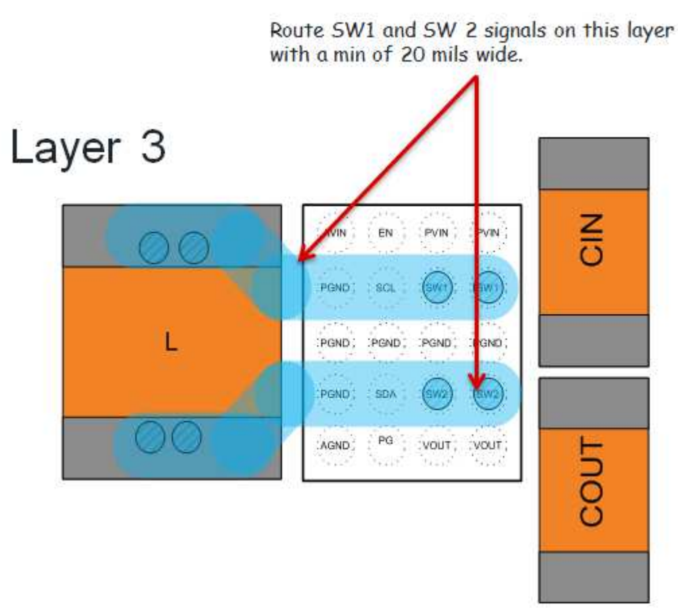

Figure 42. Layer 3 Routing for FAN49103

PHYSICAL DIMENSIONS

This table information applies to the Package drawing on the following page.

Product	D	E	X	Y
FAN49103AUC340X	2.015 ±0.030	1.615 ±0.030	0.2075	0.2075
FAN49103AUC330X	2.015 ±0.030	1.615 ±0.030	0.2075	0.2075

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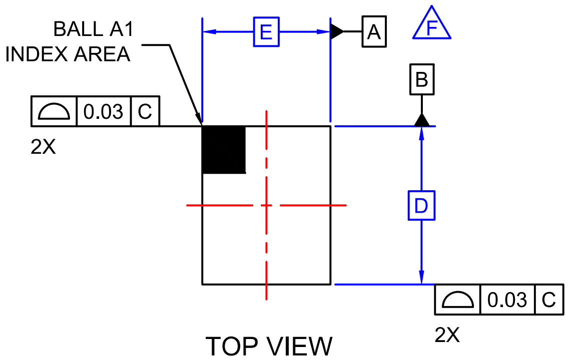
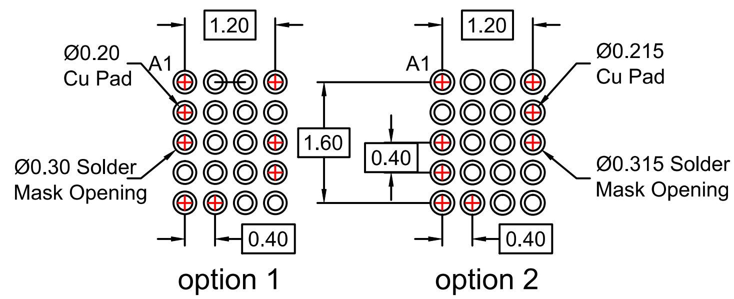
WLCSP20 2.015x1.615x0.586
CASE 567QK
ISSUE O

DATE 31 OCT 2016

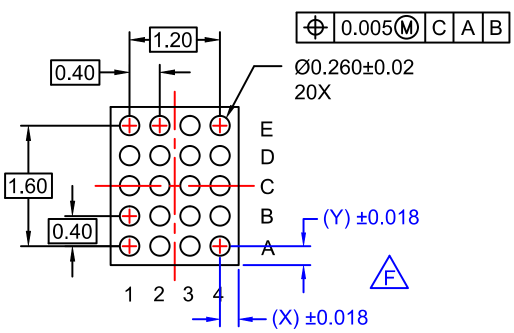


TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD TYPE)

SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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