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# FAN5033

## 8-Bit Programmable, 2- to 3-Phase, Synchronous Buck Controller

### Features

- Selectable 2- or 3-phase operation at up to 1MHz per phase
- $\pm 7.7\text{mV}$  worst-case differential sensing error over temperature
- Active current balancing between the output phases
- Power Good and Crowbar blanking supports on-the-fly VID code changes
- 0.5V to 1.6V output
- Fully compliant with the Intel® VR10 and VR11 specifications
- Selectable VR10 extended (7-bit) and VR11 (8-bit) VID tables
- Programmable soft-start ramp
- Programmable short-circuit protection and latch-off delay

### Applications

- Desktop PC/Server processor power supplies for existing and next-generation Intel processors
- VRM modules

### Description

The FAN5033 device is a multi-phase buck switching regulator controller optimized to convert a 12V input supply to the processor core voltage required by high performance Intel® processors. It has an internal 8-bit DAC that converts a digital voltage identification (VID) code, sent from the processor, to set the output voltage between 0.5V and 1.6V in 6.25mV steps. It outputs PWM signals to external MOSFET drivers that drive the switching power MOSFETs. The switching frequency of the design is programmable by a single resistor value. The number of phases can be programmed to support two- or three-phase applications.

The FAN5033 also includes programmable no-load offset and droop functions to adjust the output voltage as a function of the load current, as required by the Intel specifications. The FAN5033 provides an accurate and reliable short-circuit protection function with an adjustable over-current set point.

The FAN5033 is specified over the commercial temperature range of 0°C to +85°C and is available in a 32-lead MLP package.

### Ordering Information

Part Number	Temperature Range	Pb-Free	Package Type	Packing Method	Quantity
FAN5033MPX	0°C to 85°C	Yes	MLP-32	Tape and Reel	3,000 per Reel

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Block Diagram

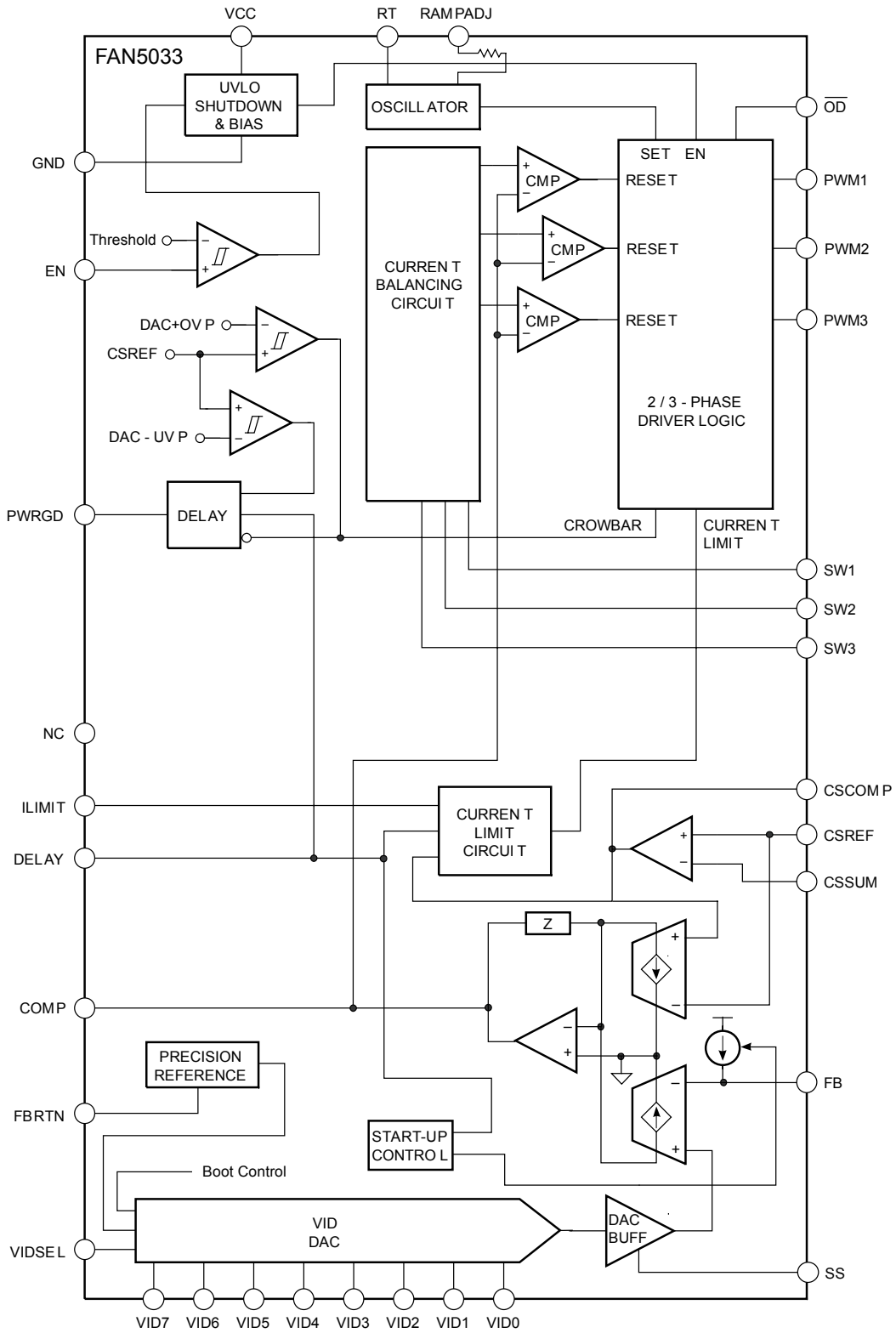


Figure 1: Block Diagram

## Pin Assignment

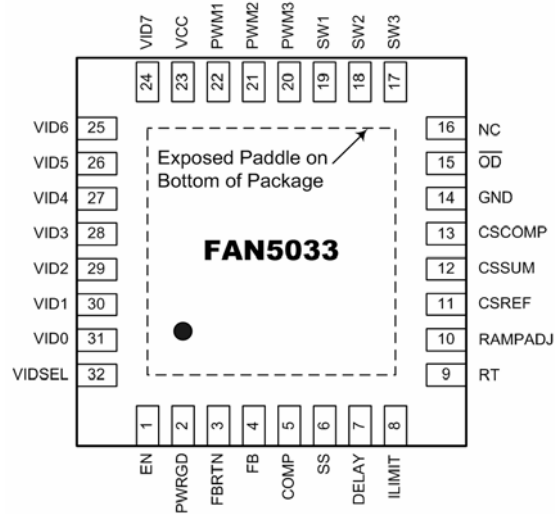



Figure 2: Pin Assignment

## Pin Definitions

Pin #	Name	Description
1	EN	<b>Power Supply Enable Input.</b> Analog comparator input with hysteresis. If input voltage is higher than the internal threshold, the controller is enabled. If lower, the controller is disabled.
2	PWRGD	<b>Power Good Output.</b> Open drain output that pulls to GND when the output voltage is outside the proper operating range.
3	FBRTN	<b>Feedback Return.</b> VID DAC and Error Amplifier reference for remote sensing of output voltage.
4	FB	<b>Feedback Input.</b> Error amplifier input for remote sensing of output voltage. A positive internal current source is connected to this pin to allow the output voltage to be offset lower than the DAC voltage.
5	COMP	<b>Error Amplifier Output.</b> For loop compensation.
6	SS	<b>Soft-Start Input.</b> An external capacitor connected between this pin and GND sets the soft-start ramp-up time.
7	DELAY	<b>Delay Timer Input.</b> An external capacitor connected between this pin and GND sets the over-current latch-off delay time, BOOT voltage hold time, EN delay time, and PWRGD delay time.
8	ILIMIT	<b>Current Limit Set.</b> An external resistor from this pin to GND sets the current limit threshold of the converter.
9	RT	<b>Frequency Set Input.</b> An external resistor connected between this pin and GND sets the oscillator frequency of the device.
10	RAMPADJ	<b>PWM Ramp Set Input.</b> An external resistor connected between this pin and the converter input voltage sets the internal PWM ramp.
11	CSREF	<b>Current Sense Amplifier Positive Input.</b> The voltage on this pin is used as the reference for the current sense amplifier. The Power Good and Crowbar functions are also internally connected to this pin.
12	CSSUM	<b>Current Sense Amplifier Negative Input.</b>
13	CSCOMP	<b>Current Sense Amplifier Compensation Output.</b>

Pin #	Name	Description
14	GND	<b>Ground.</b> All internal biasing and logic output signals of the device are referenced to this ground.
15	 OD	<b>Output Disable.</b> This pin is actively pulled low when the EN input is low or when $V_{CC}$ is below its UVLO threshold to disable the external MOSFET drivers. (Also referred to as OD# in the text of this document.)
16	NC	<b>No Connection.</b> This pin is not connected internally.
17 to 19	SW3 to SW1	<b>Switching Node Current Balance Inputs.</b> Sense the switching side of the inductor and used to measure the current level in each phase. The SW pins of unused phases should be left open.
20 to 22	PWM3 to PWM1	<b>PWM Outputs.</b> Each output is connected to the input of an external MOSFET driver, such as the FAN5109. Connecting the PWM3 output to VCC disables that phase, allowing the FAN5033 to operate as a two-phase controller.
23	VCC	<b>Supply Voltage for the Device.</b>
24 to 31	VID7 to VID0	<b>Voltage Identification Code Inputs.</b> These digital inputs are connected to the internal DAC and used to program the output voltage. These pins have $1\mu\text{A}$ internal pull-down; so if they are left open, the input state is decoded as logic low.
32	VIDSEL	<b>VID Table Select Input.</b> A logic low selects the extended VR10 DAC table and a logic high selects the VR11 DAC table. This pin has a $1\mu\text{A}$ internal pull-down; so if left open, the input state is decoded as logic low.
-	Exposed Paddle	<b>Internally connected to die ground.</b> May be connected to ground or left floating. Connect to ground for lowest package thermal resistance.

## Absolute Maximum Rating

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Unless otherwise specified, all other voltages are referenced to GND.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	-0.3		+15	V
	FBRTN	-0.3		+0.3	V
	RAMPADJ, PWM3	-0.3		V <sub>CC</sub> + 0.3	V
	SW1 – SW3	-10		+25	V
	All Other Inputs and Outputs	-0.3		+5.5	V
T <sub>J</sub>	Operating Junction Temperature	0		+125	°C
T <sub>STG</sub>	Storage Temperature	-65		+150	°C
T <sub>L</sub>	Lead Soldering Temperature (10 seconds)			300	°C
T <sub>LI</sub>	Lead Infrared Temperature (15 seconds)			260	°C
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient <sup>(1)</sup>			45	°C/W

### Note:

1. Junction-to-ambient thermal resistance, θ<sub>JA</sub>, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage, VCC to GND	9.6	12	14.4	V
T <sub>A</sub>	Ambient Temperature	0		+85	°C

## Electrical Characteristics

$V_{CC} = 12V$ ,  $FBRTN = GND$ , and  $T_A = +25^\circ C$ . The • denotes specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Error Amplifier</b>						
$V_{COMP}$	Output Voltage Range		• 0.5		4.0	V
$V_{FB}$	Accuracy Relative to nominal DAC output, referenced to FBRTN. Figure 3	VRM11 VID Range: 1.00625V to 1.60000V	• -7.7		+7.7	mV
$V_{FB(BOOT)}$	Accuracy Relative to nominal DAC output, referenced to FBRTN. Figure 3	During Start-up	• 1.092	1.100	1.108	V
	Load Line Droop Accuracy	CSREF-CSCOMP= 80mV Figure 5	• -78	-80	-82	mV
	Differential Non-linearity		• -1		+1	LSB
$\Delta V_{FB}$	Line Regulation	$V_{CC} = 10V$ to $14V$		0.05		%
$I_{FB}$	Input Bias Current		• 13.5	15.0	16.5	$\mu A$
$I_{FBRTN}$	FBRTN Current		•	70	95	$\mu A$
$I_{O(ERR)}$	Output Current	FB forced to $V_{OUT} - 3\%$		500		$\mu A$
$GBW_{(ERR)}$	Gain Bandwidth Product	COMP = $FB^{(2)}$		20		MHz
	Slew Rate	COMP = $FB^{(2)}$		25		V/ $\mu s$
$V_{CSCOMP}$	CSCOMP Voltage Range	Relative to CSREF	• -250		+250	mV
$t_{BOOT}$	BOOT Voltage Hold Time	$C_{DELAY} = 10nF$		2		ms
<b>VID Inputs and VIDSEL</b>						
$V_{IH(VID)}$	Input Low Voltage	VIDx, VIDSEL	•		0.4	V
$V_{IL(VID)}$	Input High Voltage	VIDx, VIDSEL	• 0.8		3.3	V
$V_{IH(VID)}$	Select VR10 Table	VIDSEL Logic Low			0.4	V
$I_{IN(VID)}$	Select VR11 Table	VIDSEL Logic High		0.8	3.3	V
	Input Current, VID Low			-1		$\mu A$
	VID Transition Delay Time	VID code change to FB change <sup>(2)</sup>	• 200			ns
	No CPU Detection Turn-off Delay Time	VID code change to OFF state to PWM going low <sup>(2)</sup>	• 200			ns
<b>Oscillator</b>						
$f_{OSC}$	Frequency		• 0.25		4.50	MHz
$f_{PHASE}$	Frequency Variation	$T_A = 25C$ , $R_T = 200K$ , 3- phase		-20%	400	20% kHz
$V_{RT}$	Output Voltage	$R_T = 100k\Omega$ to GND	• 1.9	2.0	2.1	V
$V_{RAMPADJ}$	RAMPADJ Output Voltage	$V_{RAMPADJ} = V_{DAC} + 2k\Omega * (V_{CC} - V_{DAC}) / (R_{RAMPADJ} + 2K\Omega)$	• -50		+50	mV
$I_{RAMPADJ}$	RAMPADJ Input Current Range			1	50	$\mu A$

### Electrical Characteristics (Continued)

$V_{CC} = 12V$ ,  $FBRTN = GND$ , and  $T_A = +25^\circ C$ . The • denotes specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
<b>Current Sense Amplifier</b>							
$V_{OS(CSA)}$	Offset Voltage	CSSUM – CSREF Figure 4	•	-1.0		+1.0	mV
$I_{BIAS(CSSUM)}$	Input Bias Current (for CSSUM)		•	-50		+50	nA
$I_{BIAS(CSREF)}$	Input Current (for CSREF)	Current drawn by CSREF Pin	•	-3		+3	$\mu A$
$GBW_{(CSA)}$	Gain Bandwidth Product	CSSUM = $C_{SCOMP}^{(2)}$			10		MHz
	Slew Rate	$C_{SCOMP} = 10pF^{(2)}$			10		V/ $\mu s$
$V_{CSACM}$	Input Common-Mode Range	CSSUM and CSREF	•	0		3.2	V
	Output Voltage Range		•	0.05		3.2	V
$I_{CSCOMP}$	Output Current				1		mA
$t_{OC(DELAY)}$	Current Limit Latch-off Delay Time	$C_{DELAY} = 10nF$			5		ms
<b>Current Balance Circuit</b>							
$V_{SW(x)CM}$	Common Mode Range <sup>(2)</sup>		•	-600		+200	mV
$R_{SW(x)}$	Input Resistance	$SW(x) = 0V$	•	35	50	65	$k\Omega$
$I_{SW(x)}$	Input Current	$SW(x) = 0V$	•	1.6	3.3	5.0	$\mu A$
$\Delta I_{SW(x)}$	Input Current Matching	$SW(x) = 0V$	•	-5		+5	%
<b>Current Limit Comparator</b>							
$V_{LIMIT}$	Output Voltage	$R_{LIMIT} = 143k\Omega$	•	1.6	1.7	1.8	V
$I_{LIMIT}$	Output Current	$R_{LIMIT} = 143k\Omega$			12		$\mu A$
	Maximum Output Current		•	60			$\mu A$
$V_{CL}$	Current Limit Threshold Voltage	$V_{CSREF} - V_{CSCOMP}$ , $R_{LIMIT} = 143k\Omega$	•	100	120	140	mV
	Current Limit Setting Ratio	$V_{CL} / I_{LIMIT}$			10		mV/ $\mu A$
<b>Delay Timer</b>							
$I_{DELAY}$	Normal Mode Output Current		•	12	15	18	$\mu A$
$I_{DELAY(CL)}$	Output Current in Current Limit		•	3.0	3.75	4.5	$\mu A$
$V_{DELAY(TH)}$	Threshold Voltage		•	1.6	1.7	1.8	V
<b>Soft-Start</b>							
$I_{(SS)}$	Output Current	During Start-up	•	12	15	18	$\mu A$
<b>Enable Input</b>							
$V_{TH(EN)}$	Threshold Voltage		•	800	850	900	mV
$V_{HYS(EN)}$	Threshold Hysteresis		•	80	100	120	mV
$I_{IN(EN)}$	Enable Input Current				1		$\mu A$
$t_{DELAY(EN)}$	Turn-on Delay	Start-up sequence, $EN > 950mV$ , $C_{DELAY} = 10nF$			2		ms



**Electrical Characteristics** (Continued)

$V_{CC} = 12V$ , FBRTN = GND, and  $T_A = +25^\circ C$ . The • denotes specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
<b>OD Output</b>							
$V_{OL(ODB)}$	Output Voltage Low	$I_{PWM(SINK)} = 400\mu A$	•		160	400	mV
$V_{OH(ODB)}$	Output Voltage High	$I_{PWM(SOURCE)} = 400\mu A$	•	4	5		V
<b>Power Good Comparator</b>							
$V_{PWRGD(UV)}$	Under-Voltage Threshold	Relative to Nominal DAC Output	•	-300	-250	-200	mV
$V_{PWRGD(OV)}$	Over-Voltage Threshold	Relative to Nominal DAC Output	•	100	150	200	mV
$V_{OL(PWRGD)}$	Output Low Voltage	$I_{PWRGD(SINK)} = -4mA$	•		200	300	mV
$t_{PWRGD}$	Power Good Delay Time	$C_{DELAY} = 10nF$ Power Good Blanking Time	Start-up sequence	•		2	ms
			VID code Changing	•		250	$\mu s$
			VID Code Static	•	100	200	ns
$V_{CROWBAR}$	Crowbar Trip Point	Relative to Nominal DAC Output	•	100	150	200	mV
	Crowbar Reset Point	Relative to FBRTN	•	250	300	350	mV
$t_{CROWBAR}$	Crowbar Delay Time	Over-voltage to PWM going low Crowbar Blanking Time	VID code Change	•	100	250	$\mu s$
			VID Code Static	•		400	ns
<b>PWM Outputs</b>							
$V_{OL(VRTM)}$	Output Voltage Low	$I_{PWM(SINK)} = 400\mu A$	•		160	400	mV
$V_{OH(VRTM)}$	Output Voltage High	$I_{PWM(SOURCE)} = 400\mu A$	•	4	5		V
	Phase Disable Voltage	Applicable to PWM3 pins only. Connect this pin to VCC to disable the phase. <sup>(3)</sup>	•	$V_{CC} - 1$			V
<b>Input Supply</b>							
$V_{CC}$	DC Supply Current	EN = Logic HIGH	•		8	12	mA
$V_{UVLO}$	UVLO Threshold	$V_{CC}$ rising	•	6.5	6.9	7.3	V
$V_{ULVOLHYS}$	UVLO Hysteresis		•	0.7	0.9	1.1	V

**Notes:**

- All limits at operating temperature extremes are guaranteed by design, characterization, and statistical quality control.
- AC specifications guaranteed by design and characterization; not production tested.
- To operate FAN5033 with fewer than three phases, PWM3 should be connected to VCC to disable this phase. See the "Theory of Operation" section for details.

Test Diagrams

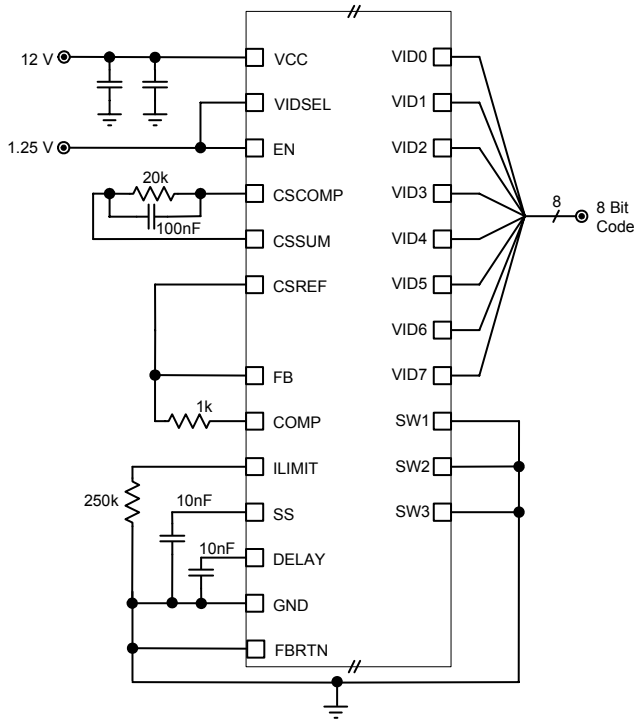


Figure 3: Closed-Loop Output Voltage Accuracy

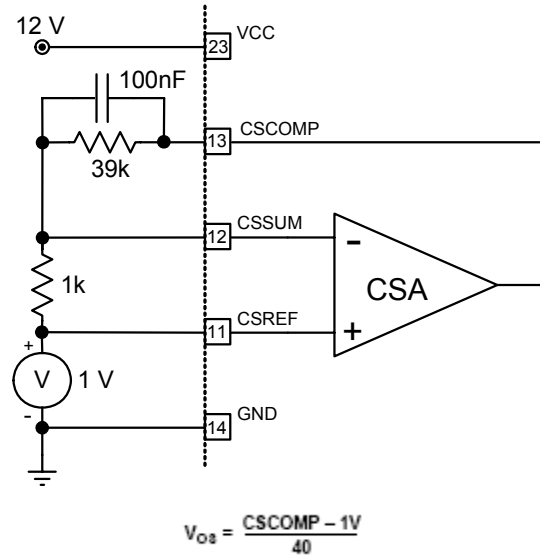


Figure 4: Current Sense Amplifier  $V_{OS}$

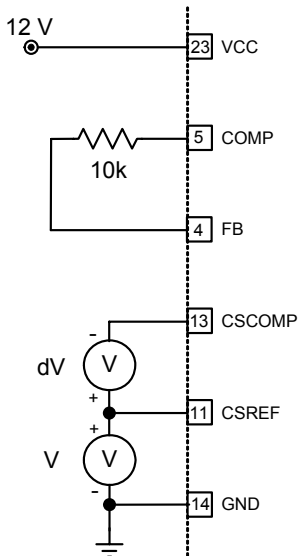


Figure 5: Droop Voltage Accuracy

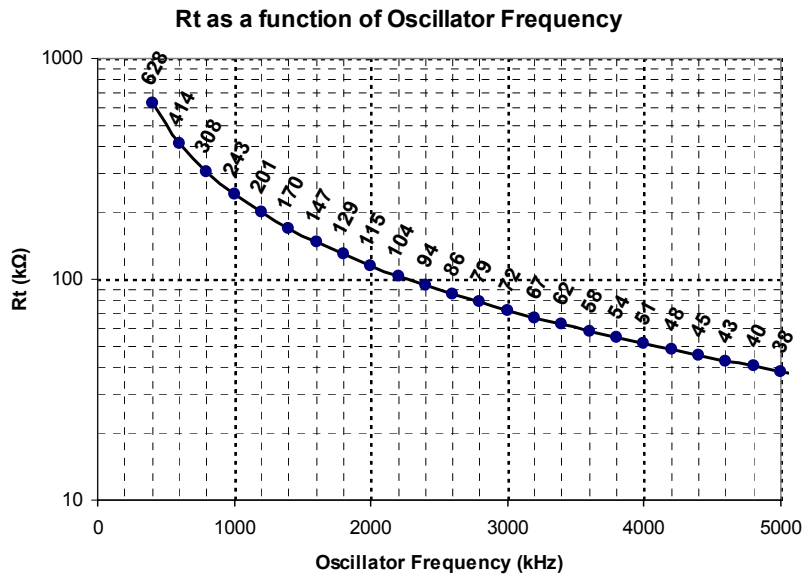


Figure 6:  $R_T$  Required to Set Oscillator Frequency

**Table 1: Output Voltage Programming Codes (extended VR10) ; 0 = logic LOW; 1 = logic HIGH.**

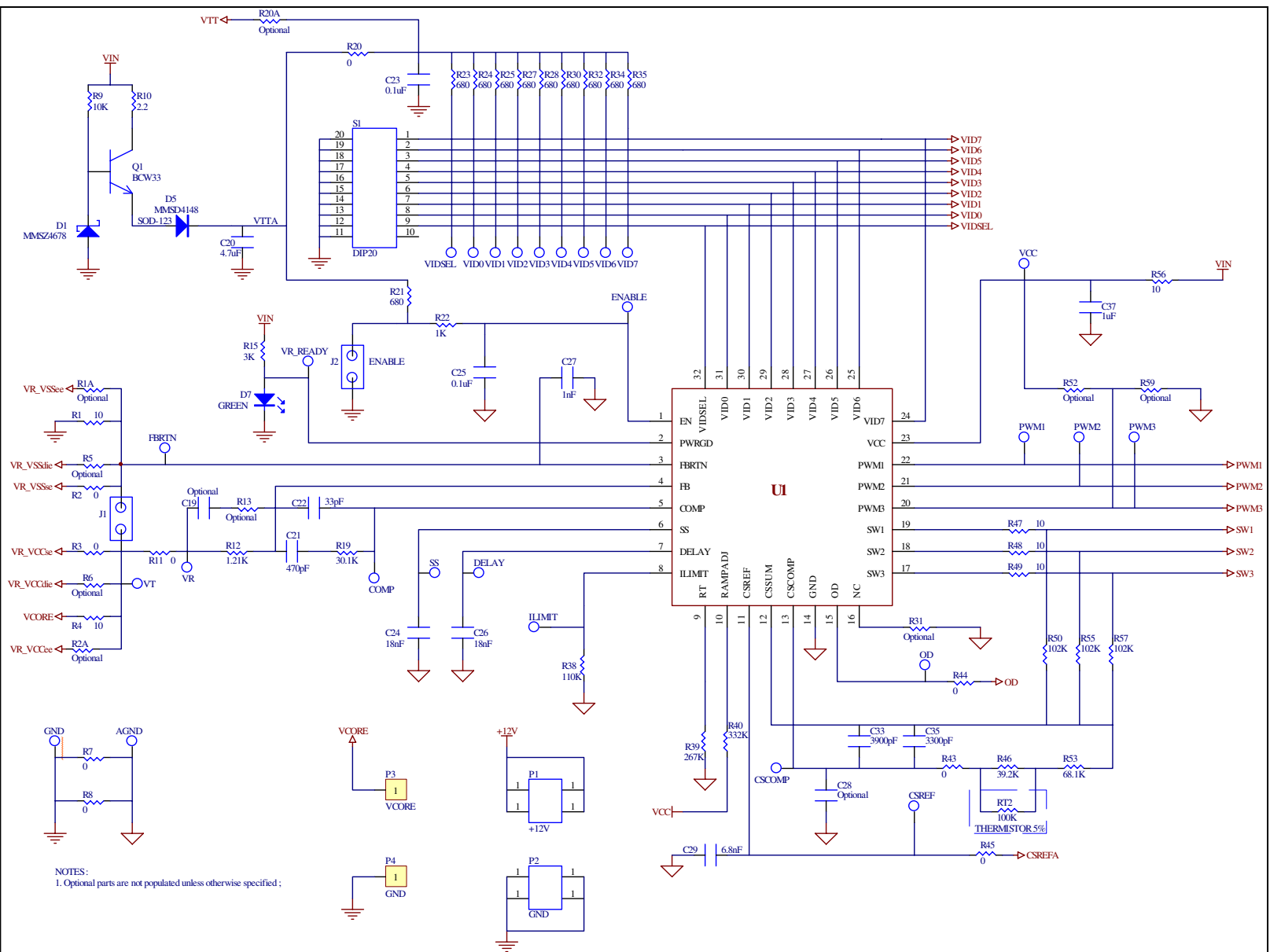
VID4	VID3	VID2	VID1	VID0	VID5	VID6	V <sub>OUT</sub> (V)
1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	0	1	OFF
1	1	1	1	0	1	0	1.09375
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	0	1	1.11250
1	1	1	0	1	1	0	1.11875
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	0	1	1.13750
1	1	1	0	0	1	0	1.14375
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	0	1	1.16250
1	1	0	1	1	1	0	1.16875
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	0	1	1.18750
1	1	0	1	0	1	0	1.19375
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	0	1	1.21250
1	1	0	0	1	1	0	1.21875
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	0	1	1.23750
1	1	0	0	0	1	0	1.24375
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	0	1	1.26250
1	0	1	1	1	1	0	1.26875
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	0	1	1.28750
1	0	1	1	0	1	0	1.29375
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	0	1	1.31250
1	0	1	0	1	1	0	1.31875
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	0	1	1.33750
1	0	1	0	0	1	0	1.34375
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	0	1	1.36250
1	0	0	1	1	1	0	1.36875
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	0	1	1.38750
1	0	0	1	0	1	0	1.39375
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	0	1	1.41250
1	0	0	0	1	1	0	1.41875
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	0	1	1.43750
1	0	0	0	0	1	0	1.44375
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	0	1	1.46250

**Table 1: Continued**

VID4	VID3	VID2	VID1	VID0	VID5	VID6	V <sub>OUT</sub> (V)
0	1	1	1	1	1	0	1.46875
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	0	1	1.48750
0	1	1	1	0	1	0	1.49375
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	0	1	1.51250
0	1	1	0	1	1	0	1.51875
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	0	1	1.53750
0	1	1	0	0	1	0	1.54375
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	0	1	1.56250
0	1	0	1	1	1	0	1.56875
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	0	1	1.58750
0	1	0	1	0	1	0	1.59375
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	0	0	0.83125
0	1	0	1	0	0	1	0.83750
0	1	0	0	1	1	0	0.84375
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	0	1	0.86250
0	1	0	0	0	1	0	0.86875
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	0	1	0.88750
0	0	1	1	1	1	0	0.89375
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	0	1	0.91250
0	0	1	1	0	1	0	0.91875
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	0	1	0.93750
0	0	1	0	1	1	0	0.94375
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	0	1	0.96250
0	0	1	0	0	1	0	0.96875
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	0	1	0.98750
0	0	0	1	1	1	0	0.99375
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	0	1	1.01250
0	0	0	1	0	1	0	1.01875
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	0	1	1.03750
0	0	0	0	1	1	0	1.04375
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	0	1	1.06250
0	0	0	0	0	1	0	1.06875
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	0	1	1.08750

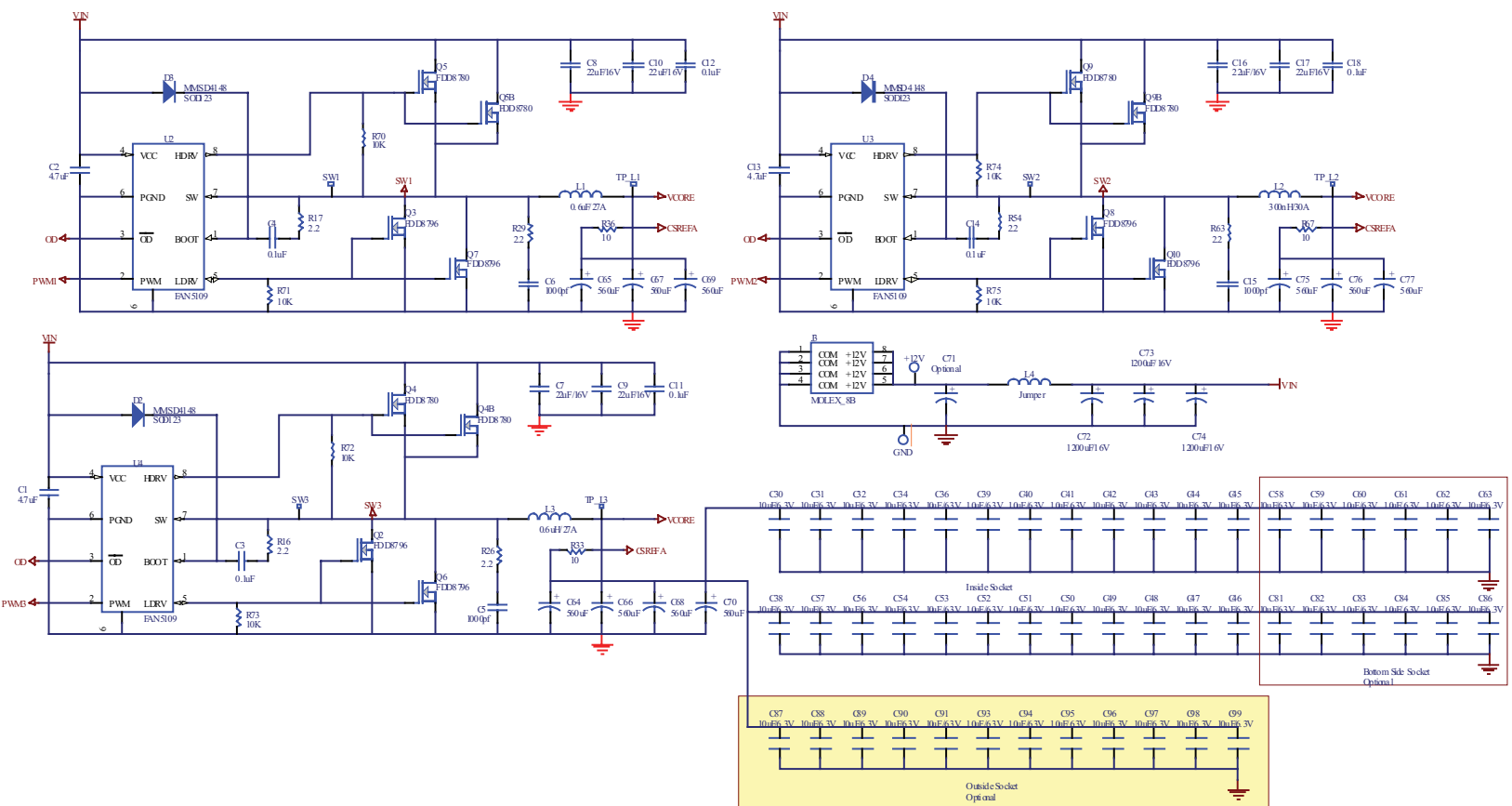
**Table 2: Output Voltage Programming Codes (8-bit) 0 = logic LOW; 1 = logic HIGH. (MSB: VID7, LSB: VID0; 11110001<sub>b</sub> = F1<sub>h</sub>)**

HEX	Voltage	Tolerance	HEX	Voltage	Tolerance	HEX	Voltage	Tolerance	HEX	Voltage	Tolerance
00	OFF		40	1.21250	+15mV LL (0 - 110A)	80	0.81250	Monotonic	C0	0.4125	Don't Care
01	OFF		41	1.20625	+15mV LL (0 - 110A)	81	0.80625	Monotonic	C1	0.40625	Don't Care
02	1.60000	+15mV LL (0 -	42	1.20000	+15mV LL (0 - 110A)	82	0.8	Monotonic	C2	0.40000	Don't Care
03	1.59375	+15mV LL (0 -	43	1.19375	+15mV LL (0 - 110A)	83	0.79375	Monotonic	C3	0.39375	Don't Care
04	1.58750	+15mV LL (0 -	44	1.18750	+15mV LL (0 - 110A)	84	0.7875	Monotonic	C4	0.38750	Don't Care
05	1.58125	+15mV LL (0 -	45	1.18125	+15mV LL (0 - 110A)	85	0.78125	Monotonic	C5	0.38125	Don't Care
06	1.57500	+15mV LL (0 -	46	1.17500	+15mV LL (0 - 110A)	86	0.775	Monotonic	C6	0.37500	Don't Care
07	1.56875	+15mV LL (0 -	47	1.16875	+15mV LL (0 - 110A)	87	0.76875	Monotonic	C7	0.36875	Don't Care
08	1.56250	+15mV LL (0 -	48	1.16250	+15mV LL (0 - 110A)	88	0.7625	Monotonic	C8	0.36250	Don't Care
09	1.55625	+15mV LL (0 -	49	1.15625	+15mV LL (0 - 110A)	89	0.75625	Monotonic	C9	0.35625	Don't Care
0A	1.55000	+15mV LL (0 -	4A	1.15000	+15mV LL (0 - 110A)	8A	0.75	Monotonic	CA	0.35000	Don't Care
0B	1.54375	+15mV LL (0 -	4B	1.14375	+15mV LL (0 - 110A)	8B	0.74375	Monotonic	CB	0.34375	Don't Care
0C	1.53750	+15mV LL (0 -	4C	1.13750	+15mV LL (0 - 110A)	8C	0.7375	Monotonic	CC	0.33750	Don't Care
0D	1.53125	+15mV LL (0 -	4D	1.13125	+15mV LL (0 - 110A)	8D	0.73125	Monotonic	CD	0.33125	Don't Care
0E	1.52500	+15mV LL (0 -	4E	1.12500	+15mV LL (0 - 110A)	8E	0.725	Monotonic	CE	0.32500	Don't Care
0F	1.51875	+15mV LL (0 -	4F	1.11875	+15mV LL (0 - 110A)	8F	0.71875	Monotonic	CF	0.31875	Don't Care
10	1.51250	+15mV LL (0 -	50	1.11250	+15mV LL (0 - 110A)	90	0.7125	Monotonic	D0	0.31250	Don't Care
11	1.50625	+15mV LL (0 -	51	1.10625	+15mV LL (0 - 110A)	91	0.70625	Monotonic	D1	0.30625	Don't Care
12	1.50000	+15mV LL (0 -	52	1.10000	+15mV LL (0 - 110A)	92	0.7	Monotonic	D2	0.30000	Don't Care
13	1.49375	+15mV LL (0 -	53	1.09375	+15mV LL (0 - 110A)	93	0.69375	Monotonic	D3	0.29375	Don't Care
14	1.48750	+15mV LL (0 -	54	1.08750	+15mV LL (0 - 110A)	94	0.6875	Monotonic	D4	0.28750	Don't Care
15	1.48125	+15mV LL (0 -	55	1.08125	+15mV LL (0 - 110A)	95	0.68125	Monotonic	D5	0.28125	Don't Care
16	1.47500	+15mV LL (0 -	56	1.07500	+15mV LL (0 - 110A)	96	0.675	Monotonic	D6	0.27500	Don't Care
17	1.46875	+15mV LL (0 -	57	1.06875	+15mV LL (0 - 110A)	97	0.66875	Monotonic	D7	0.26875	Don't Care
18	1.46250	+15mV LL (0 -	58	1.06250	+15mV LL (0 - 110A)	98	0.6625	Monotonic	D8	0.26250	Don't Care
19	1.45625	+15mV LL (0 -	59	1.05625	+15mV LL (0 - 110A)	99	0.65625	Monotonic	D9	0.25625	Don't Care
1A	1.45000	+15mV LL (0 -	5A	1.05000	+15mV LL (0 - 110A)	9A	0.65	Monotonic	DA	0.25000	Don't Care
1B	1.44375	+15mV LL (0 -	5B	1.04375	+15mV LL (0 - 110A)	9B	0.64375	Monotonic	DB	0.24375	Don't Care
1C	1.43750	+15mV LL (0 -	5C	1.03750	+15mV LL (0 - 110A)	9C	0.6375	Monotonic	DC	0.23750	Don't Care
1D	1.43125	+15mV LL (0 -	5D	1.03125	+15mV LL (0 - 110A)	9D	0.63125	Monotonic	DD	0.23125	Don't Care
1E	1.42500	+15mV LL (0 -	5E	1.02500	+15mV LL (0 - 110A)	9E	0.625	Monotonic	DE	0.22500	Don't Care
1F	1.41875	+15mV LL (0 -	5F	1.01875	+15mV LL (0 - 110A)	9F	0.61875	Monotonic	DF	0.21875	Don't Care
20	1.41250	+15mV LL (0 -	60	1.01250	+15mV LL (0 - 110A)	A0	0.6125	Monotonic	E0	0.21250	Don't Care
21	1.40625	+15mV LL (0 -	61	1.00625	+15mV LL (0 - 110A)	A1	0.60625	Monotonic	E1	0.20625	Don't Care
22	1.40000	+15mV LL (0 -	62	1.00000	Monotonic DAC (6.25 mV)	A2	0.6	Monotonic	E2	0.20000	Don't Care
23	1.39375	+15mV LL (0 -	63	0.99375	Monotonic DAC (6.25 mV)	A3	0.59375	Monotonic	E3	0.19375	Don't Care
24	1.38750	+15mV LL (0 -	64	0.98750	Monotonic DAC (6.25 mV)	A4	0.5875	Monotonic	E4	0.18750	Don't Care
25	1.38125	+15mV LL (0 -	65	0.98125	Monotonic DAC (6.25 mV)	A5	0.58125	Monotonic	E5	0.18125	Don't Care
26	1.37500	+15mV LL (0 -	66	0.97500	Monotonic DAC (6.25 mV)	A6	0.575	Monotonic	E6	0.17500	Don't Care
27	1.36875	+15mV LL (0 -	67	0.96875	Monotonic DAC (6.25 mV)	A7	0.56875	Monotonic	E7	0.16875	Don't Care
28	1.36250	+15mV LL (0 -	68	0.96250	Monotonic DAC (6.25 mV)	A8	0.5625	Monotonic	E8	0.16250	Don't Care
29	1.35625	+15mV LL (0 -	69	0.95625	Monotonic DAC (6.25 mV)	A9	0.55625	Monotonic	E9	0.15625	Don't Care
2A	1.35000	+15mV LL (0 -	6A	0.95000	Monotonic DAC (6.25 mV)	AA	0.55	Monotonic	EA	0.15000	Don't Care
2B	1.34375	+15mV LL (0 -	6B	0.94375	Monotonic DAC (6.25 mV)	AB	0.54375	Monotonic	EB	0.14375	Don't Care
2C	1.33750	+15mV LL (0 -	6C	0.93750	Monotonic DAC (6.25 mV)	AC	0.5375	Monotonic	EC	0.13750	Don't Care
2D	1.33125	+15mV LL (0 -	6D	0.93125	Monotonic DAC (6.25 mV)	AD	0.53125	Monotonic	ED	0.13125	Don't Care
2E	1.32500	+15mV LL (0 -	6E	0.92500	Monotonic DAC (6.25 mV)	AE	0.525	Monotonic	EE	0.12500	Don't Care
2F	1.31875	+15mV LL (0 -	6F	0.91875	Monotonic DAC (6.25 mV)	AF	0.51875	Monotonic	EF	0.11875	Don't Care
30	1.31250	+15mV LL (0 -	70	0.91250	Monotonic DAC (6.25 mV)	B0	0.5125	Monotonic	F0	0.11250	Don't Care
31	1.30625	+15mV LL (0 -	71	0.90625	Monotonic DAC (6.25 mV)	B1	0.50625	Monotonic	F1	0.10625	Don't Care
32	1.30000	+15mV LL (0 -	72	0.90000	Monotonic DAC (6.25 mV)	B2	0.5	Monotonic	F2	0.10000	Don't Care
33	1.29375	+15mV LL (0 -	73	0.89375	Monotonic DAC (6.25 mV)	B3	0.49375	Don't Care	F3	0.09375	Don't Care
34	1.28750	+15mV LL (0 -	74	0.88750	Monotonic DAC (6.25 mV)	B4	0.4875	Don't Care	F4	0.08750	Don't Care
35	1.28125	+15mV LL (0 -	75	0.88125	Monotonic DAC (6.25 mV)	B5	0.48125	Don't Care	F5	0.08125	Don't Care
36	1.27500	+15mV LL (0 -	76	0.87500	Monotonic DAC (6.25 mV)	B6	0.475	Don't Care	F6	0.07500	Don't Care
37	1.26875	+15mV LL (0 -	77	0.86875	Monotonic DAC (6.25 mV)	B7	0.46875	Don't Care	F7	0.06875	Don't Care
38	1.26250	+15mV LL (0 -	78	0.86250	Monotonic DAC (6.25 mV)	B8	0.4625	Don't Care	F8	0.06250	Don't Care
39	1.25625	+15mV LL (0 -	79	0.85625	Monotonic DAC (6.25 mV)	B9	0.45625	Don't Care	F9	0.05625	Don't Care
3A	1.25000	+15mV LL (0 -	7A	0.85000	Monotonic DAC (6.25 mV)	BA	0.45	Don't Care	FA	0.05000	Don't Care
3B	1.24375	+15mV LL (0 -	7B	0.84375	Monotonic DAC (6.25 mV)	BB	0.44375	Don't Care	FB	0.04375	Don't Care
3C	1.23750	+15mV LL (0 -	7C	0.83750	Monotonic DAC (6.25 mV)	BC	0.4375	Don't Care	FC	0.03750	Don't Care
3D	1.23125	+15mV LL (0 -	7D	0.83125	Monotonic DAC (6.25 mV)	BD	0.43125	Don't Care	FD	0.03125	Don't Care
3E	1.22500	+15mV LL (0 -	7E	0.82500	Monotonic DAC (6.25 mV)	BE	0.425	Don't Care	FE	OFF	
3F	1.21875	+15mV LL (0 -	7F	0.81875	Monotonic DAC (6.25 mV)	BF	0.41875	Don't Care	FF	OFF	



NOTES:  
1. Optional parts are not populated unless otherwise specified;

Figure 7A: Typical FAN5033 Three-Phase Design, Controller  
(Contact your Fairchild representative for the latest VR11 reference designs)



**Figure 7B: Typical FAN5033 Three-Phase Design, Drivers**  
 (Contact your Fairchild representative for the latest VR11 reference designs)

## Theory of Operation

**Note:** The values shown in this section are for reference only. See the parametric tables for actual values.

The FAN5033 is a fixed-frequency PWM controller with multi-phase logic outputs for use in two- and three-phase synchronous buck CPU power supplies. It has an internal VID DAC designed to interface directly with Intel's 8-bit VRD/VRM 11 and 7-bit VRD/VRM 10.x-compatible CPUs. Multi-phase operation is required for the high currents and low voltages of today's Intel's microprocessors that can require up to 150A of current.

The integrated features of the FAN5033 ensure a stable, high-performance topology for:

- Balanced currents and thermals between phases
- High-speed response at the lowest possible switching frequency and output decoupling capacitors
- Tight load line regulation and accuracy
- High-current output by allowing up to three-phase designs
- Reduced output ripple due to multi-phase operation
- Good PC board layout noise immunity
- Easily settable and adjustable design parameters with simple component selection
- Two- to three-phase operation allows optimizing designs for cost/performance and support a wide range of applications

### START-UP SEQUENCE

The FAN5033 start-up sequence is shown in Figure 8. Once the EN and UVLO conditions are met, the DELAY pin goes through one cycle (TD1); after which, the internal oscillator starts. The first two clock cycles are used for phase detection. The soft-start ramp is enabled (TD2), raising the output voltage up to the boot voltage of 1.1V. The boot hold time (TD3) allows the processor VID pins settle to the programmed VID code. After TD3 timing is finished, the output soft-starts, either up or down, to the final VID voltage during TD4. TD5 is the time between the output reaching the VID voltage and the PWRGD being presented to the system.

### PHASE-DETECTION SEQUENCE

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the FAN5033 operates as a three-phase PWM controller. For two-phase operation, connect the PWM3 pin to VCC.

The PWM logic, which is driven by the master oscillator, directs the phase sequencer and channel detectors. Channel detection occurs during the first two clock cycles after the chip is enabled. During the detection

period, PWM3 is connected to a 100 $\mu$ A sinking current source and two internal voltage comparators check the pin voltage of PWM3 versus a threshold of 3V typical. If the pin is tied to VIN, the pin voltage is above 3V and that phase is disabled and put in a tri-state mode. Otherwise, the internal 100 $\mu$ A current source pulls PWM pin below the 3V threshold. After channel detection, the 100 $\mu$ A current source is removed.

Shorting PWM3 to VCC configures the system for two-phase operation.

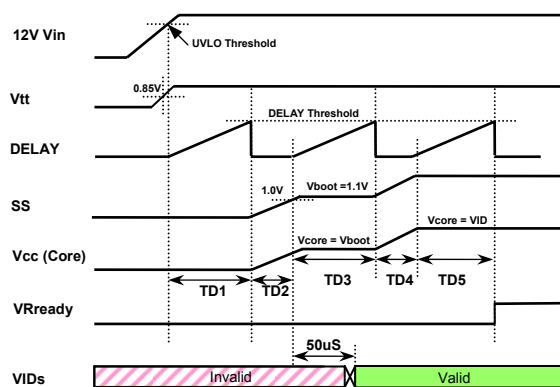


Figure 8: Start-Up Sequence Timing

After detection time is complete, the PWM outputs that were not sensed as “pulled high” function as normal PWM outputs. PWM outputs that were sensed as “pulled high” are put into a high-impedance state.

The PWM signals are logic-level outputs intended for driving external gate drivers, such as the FAN5109. Since each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at the same time to allow overlapping phases.

### MASTER CLOCK FREQUENCY

The clock frequency of the FAN5033 is set with an external resistor connected from the RT pin to ground. The frequency to resistor relationship is shown in Figure 6. To determine the frequency per phase, divide the clock by the number of enabled phases.

### OUTPUT CURRENT SENSING (See Figure 2)

The FAN5033 provides a dedicated current sense amplifier (CSA) to monitor the output current for proper voltage positioning and for current limit detection. It differentially senses the voltage drop across the DCR of the inductors to give the total average current being delivered to the load. This method is inherently more accurate than peak current detection or sampling the voltage across the low-side MOSFETs. The CSA implementation can be configured several ways, depending on the objectives of the system. It can use output inductor DCR sensing without a thermistor, for



lowest cost, or output inductor DCR sensing with a thermistor, for improved accuracy with tracking of inductor temperature.

To measure the differential voltage across the output inductors, the positive input of the CSA (CSREF pin) is connected, using equal value resistors, to the output capacitor side of the inductors. The negative input of the CSA (CSSUM pin) is connected, again using equal value resistors, to the MOSFET side of the inductors. The CSA's output (CSCOMP) is a voltage equal to the voltage dropped across the inductors, times the gain of the CSA, and is inversely proportional to the output current.

The gain of the CSA is set by connecting an external feedback resistor between the CSA's CSCOMP and CSSUM pins. A capacitor, connected across the resistor, is used to create a low pass filter to remove high-frequency switching effects and to create a RC pole to cancel the zero created by the L/DCR of the inductor. The end result is that the voltage between the CSCOMP and CSREF pins is inversely proportional to the output current (CSCOMP goes negative relative to CSREF as current increases) and the CSA gain sets the ratio of the CSA output voltage change as a function of output current change. This voltage difference is used by the current limit comparator and is also used by the droop amplifier to create the output load line.

The CSA is designed to have a low offset input voltage. The sensing gain is determined by external resistors so that it can be extremely accurate.

#### LOAD LINE IMPEDANCE CONTROL

The FAN5033 has an internal "Droop Amp" that effectively subtracts the voltage applied between the CSCOMP and CSREF pins from the FB pin voltage of the error amplifier, allowing the output voltage to be varied independent of the DAC setting. A positive voltage on CSCOMP (relative to CSREF) increases the output voltage and a negative voltage decreases it. Since the voltage between the CSA's CSCOMP and CSREF pins is inversely proportional to the output, current causes the output voltage to decrease an amount directly proportional to the increase in output, current, creating a droop or "Load Line." The ratio of output voltage decrease to output current increase is the effective  $R_o$  of the power supply and is set by the DC gain of the CSA.

#### CURRENT CONTROL MODE AND THERMAL BALANCE

The FAN5033 has individual SW inputs for each phase. They are used to measure the voltage drop across the bottom FETs to determine the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system. This gives good current balance accuracy that takes into account, not only the current, but also the thermal balance between the bottom FETs in each phase.

External resistors  $R_{SW1}$  through  $R_{SW3}$  can be placed in series with individual SW inputs to create an intentional current imbalance if desired, such as in cases where one phase has better cooling and can support higher

currents. It is best to have the ability to add these resistors in the initial design to ensure that placeholders are provided in the layout. To increase the current in a phase, increase  $R_{SW}$  for that phase. Even adding a resistor of a few hundred ohms can make a noticeable increase in current, so use small steps.

The amplitude of the internal ramp is set by a resistor connected between the input voltage and the RAMPADJ pin. This method also implements the Voltage Feed Forward function.

#### OUTPUT VOLTAGE DIFFERENTIAL SENSING

The FAN5033 uses differential sensing in conjunction with a high accuracy DAC and a low offset error amplifier to maintain a worst-case specification of  $\pm 7.7\text{mV}$  differential sensing accuracy over its specified operating range.

A high gain-bandwidth error amplifier is used for the voltage control loop. The voltage on the FB pin is compared to the DAC voltage to control the output voltage. The FB voltage is also effectively offset by the CSA output voltage for accurately positioning the output voltage as a function of current. The output of the error amplifier is the COMP pin, which is compared to the internal PWM ramps to create the PWM pulse widths.

The negative input (FB) is tied to the output sense location with a resistor ( $R_B$ ) and is used for sensing and controlling the output voltage at this point. Additionally a current source is connected internally to the FB pin, which causes a fixed DC current to flow through  $R_B$ . This current creates a fixed voltage drop (offset voltage) across  $R_B$ . The offset voltage adds to the sensed output voltage, which causes the error amp to regulate the actual output voltage lower than the programmed VID voltage by this amount. The main loop compensation is incorporated into the feedback by an external network connected between FB and COMP.

#### DELAY TIMER

The delay times for the start-up timing sequence are set with a capacitor from the DELAY pin to ground, as described in the Start-Up Sequence section. In UVLO or when EN is logic low, the DELAY pin is held at ground. Once the UVLO and EN are asserted, a  $15\mu\text{A}$  current flows out of the DELAY pin to charge  $C_{DLY}$ . A comparator, with a threshold of 1.7V, monitors the DELAY pin voltage. The delay time is therefore set by the  $15\mu\text{A}$  charging the delay capacitor from 0V to 1.7V. This DELAY pin is used for multiple delay timings (TD1, TD3, and TD5) during start-up. DELAY is also used for timing the current limit latch off as explained in the CURRENT LIMIT section.

#### SOFT-START

The soft-start times for the output voltage are set with a capacitor from the SS pin to ground. After TD1 and the phase-detection cycle have been completed, the SS time (TD2 in Figure 8) starts. The SS pin is disconnected from GND and the capacitor is charged up to the 1.1V boot voltage by the SS amplifier, which has a limited output current of  $15\mu\text{A}$ . The voltage at the FB pin follows the ramping voltage on the SS pin, limiting

the inrush current during start-up. The soft-start time depends on the value of the boot voltage and  $C_{SS}$ .

Once the SS voltage is within 100mV of the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft-start time (TD4). The SS voltage changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using the SS amplifier with the limited output current of 15 $\mu$ A. The voltage of the FB pin follows the ramping voltage of the SS pin, limiting the inrush current during the transition from the boot voltage to the final DAC voltage. The second soft-start time depends on the boot voltage, the programmed VID DAC voltage, and  $C_{SS}$ .

If either EN is taken low or  $V_{CC}$  drops below UVLO, DELAY and SS are reset to ground to be ready for another soft-start cycle. Figure 9 shows typical start-up waveforms for the FAN5033.

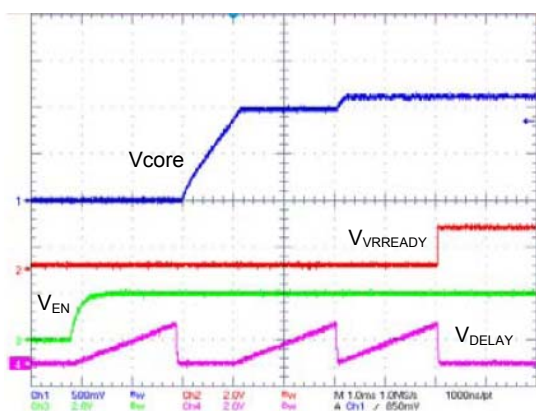


Figure 9: Start-up Waveforms

### CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The FAN5033 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The current limit level is set with the resistor from the ILIMIT pin to ground. During operation, the voltage on ILIMIT is 1.7V. The current through the external resistor is internally scaled to give a current limit threshold of 10mV/ $\mu$ A. If the voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After TD5 has completed, an over-current (OC) event starts a latch-off delay timer. The delay timer uses the DELAY pin timing capacitor. During current limit, the DELAY pin current is reduced to 3.75  $\mu$ A. When the voltage on the delay pin reaches 1.7V, the controller shuts down and latches off. The current limit latch-off delay time is therefore set by the current of 3.75 $\mu$ A charging the delay capacitor 1.7V. This delay is four times longer than the delay time during the start-up sequence. If there is a current limit during start-up, the FAN5033 goes through TD1 to TD5 in current limit and

starts the latch-off timer. Because the controller continues to operate during the latch-off delay time, if the OC is removed before the 1.7V threshold is reached, the controller returns to normal operation and the DELAY capacitor is reset to GND.

The latch-off function can be reset by cycling the supply voltage to the FAN5033 or by toggling the EN pin low for a short time. To disable the short-circuit latch-off function, an external resistor can be placed in parallel with  $C_{DLY}$  to prevent the DELAY capacitor from charging up to the 1.7V threshold. The addition of this resistor causes a slight increase in the delay times.

During start-up, when the output voltage is below 200mV, a secondary current limit is active. This secondary current limit clamps the internal COMP voltage at the PWM comparators to 1.5V. Typical over-current latch-off waveforms are shown in Figure 10.

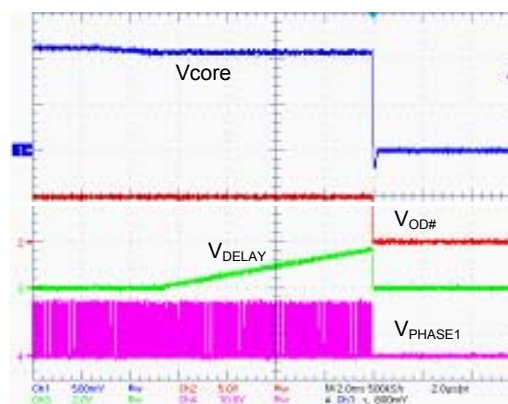


Figure 10: Over-Current Latch-off Waveforms

### DYNAMIC VID

The FAN5033 has the ability to dynamically change the VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID on-the-fly (OTF). A VID OTF can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID input changes state, the FAN5033 detects the change and ignores the DAC inputs for a minimum of 200ns. This time prevents a false code due to logic skew while the eight VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 $\mu$ s to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

### POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified based on the VID voltage setting. PWRGD goes low if the output voltage is

outside of the specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a VID OTF event for a period of  $\sim 200\mu\text{s}$  to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn-on delay time (TD5) based on the DELAY timer. Prior to the SS voltage reaching the programmed VID DAC voltage of  $-100\text{mV}$ , the PWRGD pin is held low. Once the SS pin is within  $100\text{mV}$  of the programmed DAC voltage, the capacitor on the DELAY pin begins to charge up. A comparator monitors the DELAY voltage and enables PWRGD when the voltage reaches  $1.7\text{V}$ . The PWRGD delay time is therefore set by a current of  $15\mu\text{A}$  charging a capacitor from  $0\text{V}$  to  $1.7\text{V}$ .

### OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately  $300\text{mV}$ .

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this action current-limits the input supply, protecting the microprocessor.

### OUTPUT ENABLE AND UVLO

For the FAN5033 to begin switching, the input supply ( $V_{\text{CC}}$ ) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its  $0.85\text{V}$  threshold. This initiates a system start-up sequence. If either UVLO or EN is less than their respective thresholds, the FAN5033 is disabled, which holds the

PWM outputs low, discharges the DELAY and SS capacitors, and forces PWRGD and OD# signals low.

In the application circuit, the OD# pin should be connected to the OD# inputs of the FAN5009 or FAN5109 drivers. Pulling OD# low disables the drivers such that both DRVH and DRVL are driven low. This turns off the bottom MOSFETs to prevent them from discharging the output capacitors through the output inductors. If the bottom MOSFETs were left on, the output capacitors could ring with the output inductors and produce a negative output voltage to the processor.

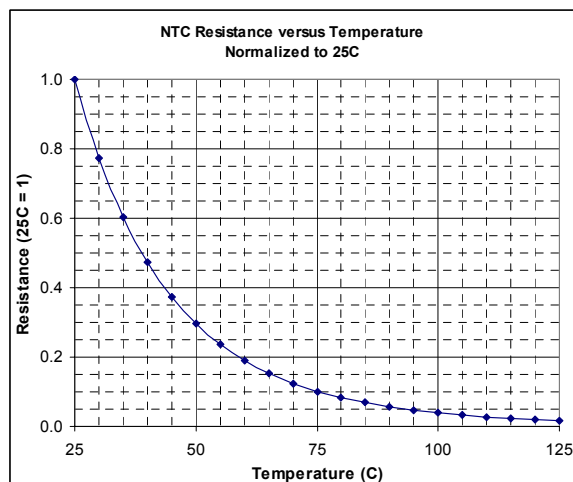


Figure 11: Typical NTC Resistance vs. Temperature

## Application Section

### Instructions

The purpose of this Mathcad program is to cover design and optimization of the control design that is very important for the FAN5029/31/32/33 based multiphase VR design in order to meet critical dynamic performance requirements. This Mathcad program is available from Fairchild upon request, and feel free to contact us should you have any questions.

Highlight regions, such as  $V_{in} := 12$  are required input fields.

### Input Parameters

$V_{in} := 12$		Input voltage (V)
$V_o := 1.4$		Output voltage (V)
$I_{omax} := 110$		Max. output current (A)
$\eta := 80\%$		Estimated converter efficiency at max. load
$D := \frac{V_o}{V_{in} \cdot \eta}$	$D = 0.146$	Duty cycle
$f_s := 300 \cdot 10^3$		Per phase switching frequency (Hz)
$T_s := \frac{1}{f_s}$	$T_s = 3.333 \times 10^{-6}$	Per phase switching period
$N_p := 3$		Number of phases
$R_o := \frac{V_o}{I_{omax}}$	$R_o = 0.013$	
$I_{rms} := I_{omax} \cdot \sqrt{\frac{D}{N_p} - D^2}$	$I_{rms} = 18.190$	

Choose input capacitors based on this input RMS current.

Select inductor peak-to-peak ripple current from 25% to 55%.

$i_{ripple} := 30\%$		Per phase Inductor peak-to-peak ripple current percentage
$I_{ripple} := \frac{I_{omax}}{N_p} \cdot i_{ripple}$	$I_{ripple} = 11.000$	Per phase inductor peak-to-peak ripple current (A)
$L := \frac{1 - D}{f_s} \cdot \frac{V_o \cdot N_p}{I_{omax} \cdot i_{ripple}}$	$L = 3.624 \times 10^{-7}$	
$L := 0.6 \cdot 10^{-6}$		Per phase inductance (at 0A load)
$k_L := 1.0$		Inductor roll-off factor at max. load

$$r := \ln\left(\frac{\max}{\min}\right) \quad s_k := \min \cdot e^{\frac{r}{n}} \quad j := \sqrt{-1}$$

### Open Loop Transfer Function Definition

$sz1 := \frac{1}{Rc \cdot C}$	$fz1 := \frac{sz1}{2 \cdot \pi}$	$fz1 = 4.060 \times 10^4$	Output bulk capacitor ESR zero (Hz)
$sz2 := \frac{1}{Rc2 \cdot C2}$	$fz2 := \frac{sz2}{2 \cdot \pi}$	$fz2 = 5.305 \times 10^6$	Output ceramic capacitor ESR zero (Hz)
$wo := \frac{1}{\sqrt{L \cdot C}}$	$fo := \frac{wo}{2 \cdot \pi}$	$fo = 4.756 \times 10^3$	Open loop power stage double poles (Hz)
$Q(Ro) := \frac{1}{wo} \cdot \frac{1}{\left(\frac{L}{Ro}\right) + C \cdot Rc}$		$Q(Ro) = 1.704$	Open loop power stage damping factor

### Open-Loop Control-to-Output Transfer Function F2(s)

$$A(Ro) := Rc \cdot Rc2 \cdot C \cdot C2 + \frac{L}{Ro} \cdot (Rc \cdot C + Rc2 \cdot C2) + L \cdot (C + C2)$$

$$B(Ro) := \frac{L}{Ro} \cdot Rc \cdot Rc2 \cdot C \cdot C2 + L \cdot C \cdot C2 \cdot (Rc + Rc2)$$

$$F2(s, Ro) := Vin \cdot \frac{(1 + s \cdot Rc \cdot C) \cdot (1 + s \cdot Rc2 \cdot C2)}{1 + s \cdot \left(Rc \cdot C + Rc2 \cdot C2 + \frac{L}{Ro}\right) + s^2 \cdot A(Ro) + s^3 \cdot B(Ro)}$$

$$magF2(i, Ro) := 20 \cdot \left(\log\left(\left|F2\left(s_1 \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseF2(i, Ro) := \text{angle}\left(\text{Re}\left(F2\left(s_1 \cdot j \cdot 2 \cdot \pi, Ro\right)\right), \text{Im}\left(F2\left(s_1 \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi} - 360$$

$$\text{coef} := \begin{pmatrix} 1 \\ Rc \cdot C + Rc2 \cdot C2 + \frac{L}{Ro} \\ A(Ro) \\ B(Ro) \end{pmatrix} \quad \text{polyroots}(\text{coef}) = \begin{pmatrix} -3.202 \times 10^6 \\ -7.630 \times 10^3 - 2.702i \times 10^4 \\ -7.630 \times 10^3 + 2.702i \times 10^4 \end{pmatrix}$$

### Open Loop Output Impedance Zp(s)

$$Zp(s, Ro) := \frac{RL \cdot (1 + s \cdot Rc \cdot C) \cdot (1 + s \cdot Rc2 \cdot C2) \cdot \left(1 + s \cdot \frac{L}{RL}\right)}{1 + s \cdot \left(Rc \cdot C + Rc2 \cdot C2 + \frac{L}{Ro}\right) + s^2 \cdot A(Ro) + s^3 \cdot B(Ro)}$$

$$s_{217} = 1.216 \times 10^4$$

$$magF2(217, Ro) = 5.598$$

$$phaseF2(217, Ro) = -151.560$$

$$magZp(i, Ro) := 20 \cdot \left(\log\left(\left|Zp\left(s_1 \cdot j \cdot 2 \cdot \pi, Ro\right)\right|\right)\right)$$

$$phaseZp(i, Ro) := \text{angle}\left(\text{Re}\left(Zp\left(s_1 \cdot j \cdot 2 \cdot \pi, Ro\right)\right), \text{Im}\left(Zp\left(s_1 \cdot j \cdot 2 \cdot \pi, Ro\right)\right)\right) \cdot \frac{180}{\pi}$$

### Sampling Gain He(s)

$$W_n := \frac{\pi}{T_s} \qquad Q_z := \frac{-2}{\pi}$$

$$H_e(s) := 1 + \frac{s}{W_n \cdot Q_z} + \frac{s^2}{W_n^2}$$

$$F_i(s) := R_i \cdot H_e(s) \qquad \text{Current sense gain}$$

$$\text{mag}F_i(i) := 20 \cdot \left( \log \left( \left| F_i(s_1 \cdot j \cdot 2 \cdot \pi) \right| \right) \right) \qquad \text{phase}F_i(i) := \text{angle} \left( \text{Re} \left( F_i(s_1 \cdot j \cdot 2 \cdot \pi) \right), \text{Im} \left( F_i(s_1 \cdot j \cdot 2 \cdot \pi) \right) \right) \cdot \frac{180}{\pi}$$

### Open Loop Transfer Function: F5(s) = iL/iO

$$F_5(s, R_o) := \frac{1}{\frac{1}{R_c + \frac{1}{s \cdot C}} + \frac{1}{R_{c2} + \frac{1}{s \cdot C2}} + \frac{1}{R_o} + \frac{1}{s \cdot L + R_L}} \cdot \frac{1}{s \cdot L + R_L}$$

$$\text{mag}F_5(i, R_o) := 20 \cdot \left( \log \left( \left| F_5(s_1 \cdot j \cdot 2 \cdot \pi, R_o) \right| \right) \right)$$

$$\text{phase}F_5(i, R_o) := \text{angle} \left( \text{Re} \left( F_5(s_1 \cdot j \cdot 2 \cdot \pi, R_o) \right), \text{Im} \left( F_5(s_1 \cdot j \cdot 2 \cdot \pi, R_o) \right) \right) \cdot \frac{180}{\pi} - 360$$

### Open Loop Control to Inductor Current Transfer Function: F4(s) = iL/d

$$F_4(s, R_o) := V_{in} \cdot \frac{1}{s \cdot L + R_L + \frac{1}{\frac{s \cdot C}{1 + s \cdot R_c \cdot C} + \frac{s \cdot C2}{1 + s \cdot R_{c2} \cdot C2} + \frac{1}{R_o}}}$$

$$\text{mag}F_4(i, R_o) := 20 \cdot \left( \log \left( \left| F_4(s_1 \cdot j \cdot 2 \cdot \pi, R_o) \right| \right) \right)$$

$$\text{phase}F_4(i, R_o) := \text{angle} \left( \text{Re} \left( F_4(s_1 \cdot j \cdot 2 \cdot \pi, R_o) \right), \text{Im} \left( F_4(s_1 \cdot j \cdot 2 \cdot \pi, R_o) \right) \right) \cdot \frac{180}{\pi} - 0$$

### Voltage Compensator Gain Fv(s)

For most of applications using electrolytic type dominant output capacitors, a 2-pole-1-zero compensator, consisting of R2, R3, C2, and C3 as shown in below, is sufficient to meet the VR dynamic requirements. However a placeholder for a 3-pole-2-zero compensator is always recommended in the PCB layout, in order to have a little flexibility to fine tune the VR performance.

For ceramic types of output capacitor dominant applications, a 3-pole-2-zero compensator is usually mandatory.

In this design example, electrolytic type dominant output capacitors are used.

The compensator design adopts an interactive approach. In such a condition, one can optimize the control design by interactive tuning the compensator parameters through a few iterations.

As a good starting point, select the compensator zero to be around 1.5 ~ 3.5X open loop power stage double poles, and select the high frequency pole to be around 0.8 ~ 2.5X per phase switching frequency. The compensator high frequency pole is placed in order to filter out high frequency switching noise. It's not recommended to place it too close to the control bandwidth. Use the DC gain of  $\omega_l$  to adjust the control bandwidth. It's quite important to note that the

compensator zero and DC gain are critical parameters, and need to be fine tuned in interactive manner through a few iterations of this program.

$$fzc1 := 12 \cdot 10^3$$

Place the compensator zero to cancel the power stage pole (1.5 ~ 3.5X open loop power stage double poles) (Hz)

$$\omega zc1 := 2 \cdot \pi \cdot fzc1$$

$$fzc2 := 15 \cdot 10^{13}$$

To cancel the power stage pole (Hz)

$$\omega zc2 := 2 \cdot \pi \cdot fzc2$$

$$fpc1 := 80 \cdot 10^3$$

To be placed around 0.8 ~ 2.5X the per phase switching frequency (Hz)

$$\omega pc1 := 2 \cdot \pi \cdot fpc1$$

$$fpc2 := 57 \cdot 10^{13}$$

To cancel the lower power stage esr zero (Hz)

$$\omega pc2 := 2 \cdot \pi \cdot fpc2$$

$$\omega I := 1.5 \cdot 10^6$$

Cross over freq. adjustment

$$Fv(s) := \frac{\omega I \left(1 + \frac{s}{\omega zc1}\right) \left(1 + \frac{s}{\omega zc2}\right)}{s \left(1 + \frac{s}{\omega pc1}\right) \left(1 + \frac{s}{\omega pc2}\right)}$$

Input the 1% feedback resistor (Rfb) first. Instructions of how to calculate Rfb can be found in the Appendix at the end of this file.

$$R2 := 1.21 \cdot 10^3$$

Input R2 (Rfb - 1% resistor) here (ohm)  
See Appendix section for how to calculate Rfb.

Given

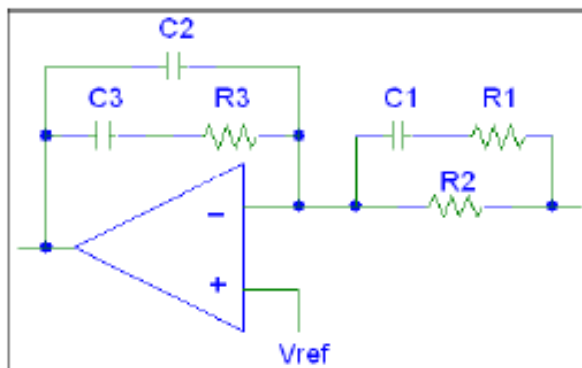
$$\frac{1}{R3 \cdot C3} = \omega zc1$$

$$\frac{1}{(R1 + R2) \cdot C1} = \omega zc2$$

$$\frac{1}{R3 \cdot C2 \cdot C3} (C2 + C3) = \omega pc1$$

$$\frac{1}{R1 \cdot C1} = \omega pc2$$

$$\frac{1}{R2 \cdot (C2 + C3)} = \omega I$$



$$\text{Find}(C1, C2, C3, R1, R3) \rightarrow \begin{pmatrix} .64612707069349998572e-18 \\ .82644628099173553719e-10 \\ .46831955922865013774e-9 \\ 432.14285714285714286 \\ 28320.217814881375924 \end{pmatrix}$$

Calculated C1 (F)  
 Calculated C2 (F)  
 Calculated C3 (F)  
 Calculated R1 (ohm)  
 Calculated R3 (ohm)

Select the closed 1% resistors, and NPO or X7R types of capacitors as the compensator elements. If the above calculated value is either less than 1pF or negative, these components are not necessary. It's a good practice to have at least 10pF capacitance for C2.

Select:

$C2 := 82 \cdot 10^{-12}$  Input capacitance closing to the above calculated compensator value (F)

$C3 := 0.47 \cdot 10^{-9}$  Input capacitance closing to the above calculated compensator value (F)

$R3 := 28.2 \cdot 10^3$  Input resistance closing to the above calculated compensator value (ohm)

$C1 := 0.820 \cdot 10^{-18}$  Input capacitance closing to the above calculated compensator value (F)

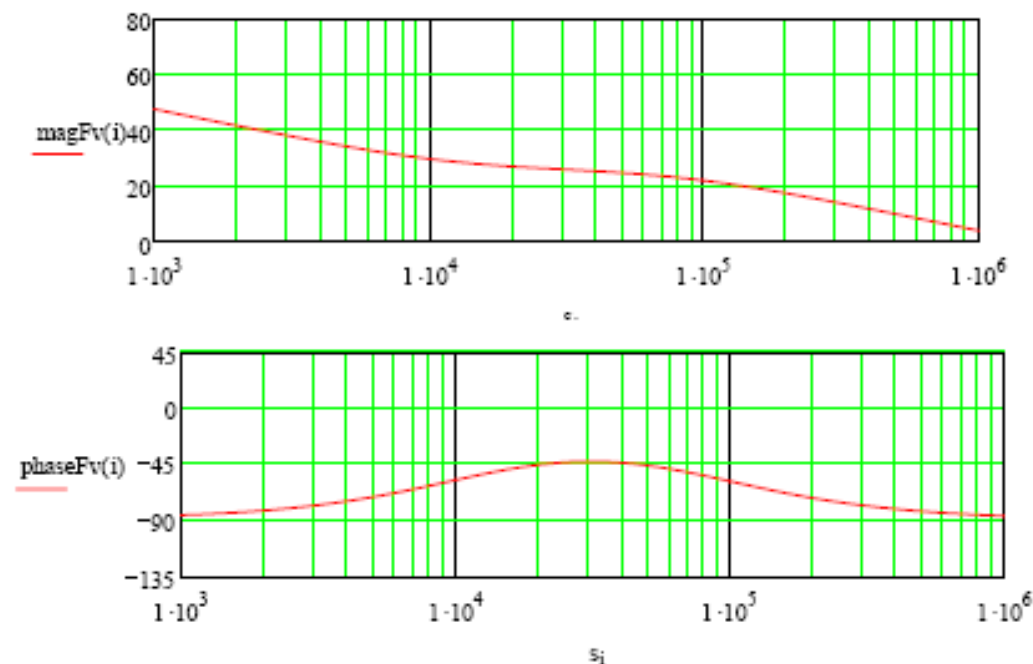
$R1 := 2.499 \cdot 10^6$  Input resistance closing to the above calculated compensator value (ohm)

$$Fv(s) := \frac{(1 + s \cdot R3 \cdot C3) \cdot [1 + s \cdot (R1 + R2) \cdot C1]}{\left[ \frac{1}{25000} + s \cdot R2 \cdot (C2 + C3) \right] \cdot \left( 1 + s \cdot R3 \cdot \frac{C2 \cdot C3}{C2 + C3} \right) \cdot (1 + s \cdot R1 \cdot C1)}$$

$$s_{217} = 1.216 \times 10^4$$

$$\text{magFv}(i) := 20 \cdot \log\left(\left|Fv(s_1 \cdot j \cdot 2 \cdot \pi)\right|\right) \quad \text{magFv}(217) = 28.811$$

$$\text{phaseFv}(i) := \frac{180}{\pi} \cdot \text{angle}\left(\text{Re}\left(Fv(s_1 \cdot j \cdot 2 \cdot \pi)\right), \text{Im}\left(Fv(s_1 \cdot j \cdot 2 \cdot \pi)\right)\right) - 360 \quad \text{phaseFv}(217) = -53.147$$



### Current Loop Gain $Ti$ & Voltage Loop Gain $Tv$

$$Ti(s, Ro) := Fm(I_{omax}) \cdot Fi(s) \cdot F4(s, Ro)$$

$$Tv(s, Ro) := Fm(I_{omax}) \cdot Fv(s) \cdot F2(s, Ro)$$

$$\text{magTi}(i, Ro) := 20 \cdot \left(\log\left(\left|Ti(s_1 \cdot j \cdot 2 \cdot \pi, Ro)\right|\right)\right)$$

$$\text{phaseTi}(i, Ro) := \text{angle}\left(\text{Re}\left(Ti(s_1 \cdot j \cdot 2 \cdot \pi, Ro)\right), \text{Im}\left(Ti(s_1 \cdot j \cdot 2 \cdot \pi, Ro)\right)\right) \cdot \frac{180}{\pi}$$



$$\text{magTv}(i, \text{Ro}) := 20 \cdot \left( \log \left( \left| \text{Tv}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right| \right) \right)$$

$$\text{phaseTv}(i, \text{Ro}) := \text{angle} \left( \text{Re} \left( \text{Tv}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right), \text{Im} \left( \text{Tv}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right) \right) \cdot \frac{180}{\pi} - 360$$

### Overall Loop Gain T1

$$\text{T1}(s, \text{Ro}) := \text{Tv}(s, \text{Ro}) + \text{Ti}(s, \text{Ro})$$

$$\text{magT1}(i, \text{Ro}) := 20 \cdot \left( \log \left( \left| \text{T1}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right| \right) \right)$$

$$\text{phaseT1}(i, \text{Ro}) := \text{angle} \left( \text{Re} \left( \text{T1}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right), \text{Im} \left( \text{T1}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right) \right) \cdot \frac{180}{\pi} - 180$$

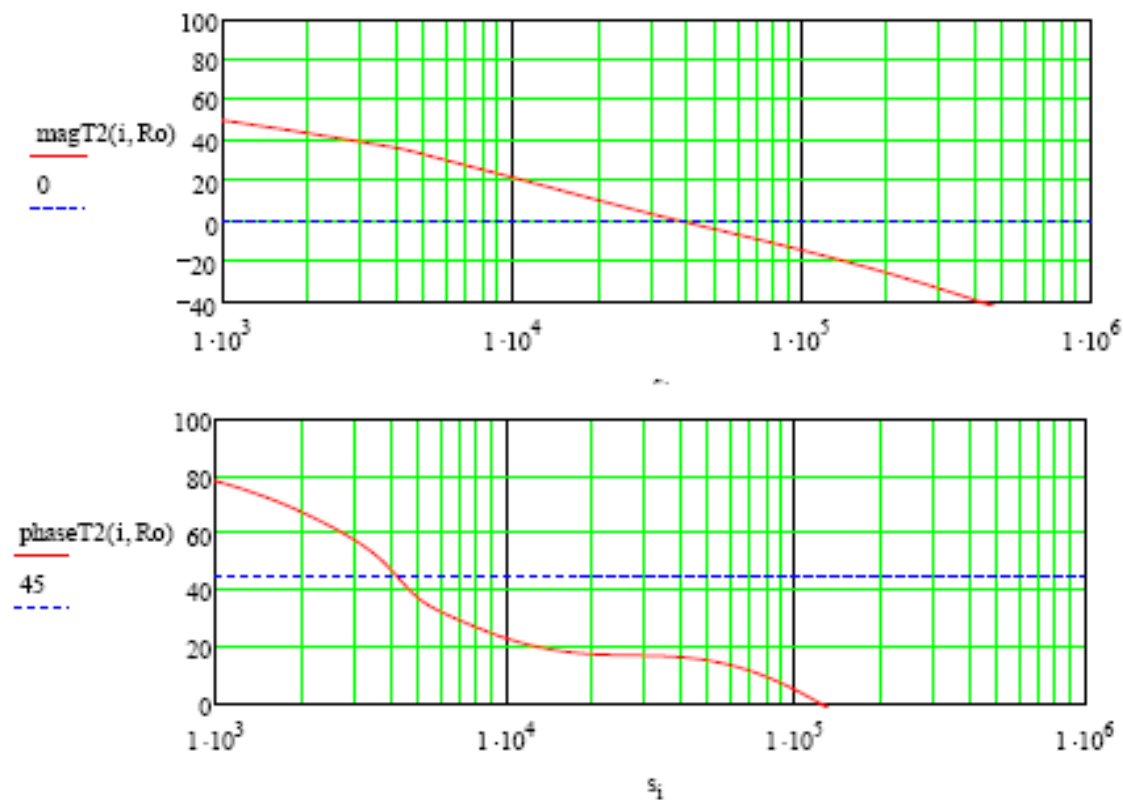
### Outer Loop Gain T2

$$\text{T2}(s, \text{Ro}) := \frac{\text{Tv}(s, \text{Ro})}{1 + \text{Ti}(s, \text{Ro})}$$

$$\text{magT2}(i, \text{Ro}) := 20 \cdot \left( \log \left( \left| \text{T2}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right| \right) \right)$$

$$\text{phaseT2}(i, \text{Ro}) := \text{angle} \left( \text{Re} \left( \text{T2}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right), \text{Im} \left( \text{T2}(s_i \cdot j \cdot 2 \cdot \pi, \text{Ro}) \right) \right) \cdot \frac{180}{\pi} - 180$$

$$\text{phaseT2}(i, \text{Ro}) := \begin{cases} \text{phaseT2}(i, \text{Ro}) & \text{if } \text{phaseT2}(i, \text{Ro}) < 180 \\ \text{phaseT2}(i, \text{Ro}) - 360 & \text{otherwise} \end{cases}$$



$$\text{magT2}(0, \text{Ro}) = 50.346$$

Guess:  $m := 300$

Given

$m := \text{round}(\text{Find}(m))$

$s_m = 4.027 \times 10^4$

T2 Crossover Frequency:

$\text{PmarginT2} := 0 + \text{phaseT2}(m, R_o)$

T2 Phase Margin:

$$20 \cdot \left( \log \left( \left| T2 \left( \min \left( e^{\frac{m}{n}} \cdot j \cdot 2 \cdot \pi, R_o \right) \right) \right| \right) \right) = 0$$

$m = 321.000$

$\text{fcrossT2} := s_m$

$\text{fcrossT2} = 4.027 \times 10^4$

$\text{PmarginT2} = 16.612$

### Droop Loop Gain Tdrp

$R_{idrp} := RL$

Droop current sense resistance = Inductor DCR / Number of Phase

Input the following droop amplifier component values for Rcs, Rph, and Ccs. Please see the Appendix section at the end of the file for instructions of how to calculate these component values.

$R_{cs} := 28.16 \cdot 10^3 + 68.1 \cdot 10^3$

Input droop amplifier component value here (ohm)

$R_{ph} := 102 \cdot 10^3$

Input droop amplifier component value here (ohm)

$R_{ph} := \frac{R_{ph}}{N_p}$

$C_{cs} := 4.7 \cdot 10^{-9} + 4.7 \cdot 10^{-9}$

Droop amplifier component value (F)

$$F_{drp}(s) := \frac{1 + s \cdot \frac{L}{RL}}{1 + s \cdot R_{cs} \cdot C_{cs}} \cdot \frac{R_{cs}}{R_{ph}}$$

To simplify the analysis, let's assume that the droop amplifier time constant  $R_{cs} \cdot C_{cs}$  exactly matches the inductor time constant  $L/RL$ . Then the above equation can be reduced to a simple gain.

$$F_{drp}(s) := \frac{R_{cs}}{R_{ph}}$$

$$T_{drp}(s, R_o) := F_4(s, R_o) \cdot R_{idrp} \cdot F_{drp}(s) \cdot (1 + F_v(s)) \cdot F_m(M_c)$$

$$\text{magTdrp}(i, R_o) := 20 \cdot \left( \log \left( \left| T_{drp}(s_i \cdot j \cdot 2 \cdot \pi, R_o) \right| \right) \right)$$

$$\text{phaseTdrp}(i, R_o) := \text{angle} \left( \text{Re} \left( T_{drp}(s_i \cdot j \cdot 2 \cdot \pi, R_o) \right), \text{Im} \left( T_{drp}(s_i \cdot j \cdot 2 \cdot \pi, R_o) \right) \right) \cdot \frac{180}{\pi} - 360$$