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March 2016

FAN54005
USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Charge Voltage Accuracy: ±0.5% at 25°C
±1% from 0 to 125°C
- ±5% Input Current Regulation Accuracy
- ±5% Charge Current Regulation Accuracy
- 20 V Absolute Maximum Input Voltage
- 6 V Maximum Input Operating Voltage
- 1.45 A Maximum Charge Rate
- Programmable through High-Speed I^2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Charger Voltage
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1 µH External Inductor
- Safety Timer with Reset Control
- 1.8 V Regulated Output from VBUS for Auxiliary Circuits
- Dynamic Input Voltage Control Automatically Reduces Charging Current with Weak Input Sources
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5 V, 500 mA Boost Mode for USB OTG for 3.0 V to 4.5 V Battery Input
- Available in a 1.96 x 1.87 mm, 20-bump, 0.4 mm Pitch WLCSP Package

Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

Description

The FAN54005 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I^2C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN54005 provides battery charging in three phases: conditioning, constant current and constant voltage.

To ensure USB compliance and minimize charging time, the input current limit can be changed through the I^2C interface by the host processor. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I^2C host. Charge status is reported to the host through the I^2C port.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, preventing leakage from the battery to the input. Charge current is reduced when the die temperature reaches 120°C, protecting the device and PCB from damage.

The FAN54005 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery and uses the same external components used for charging the battery.

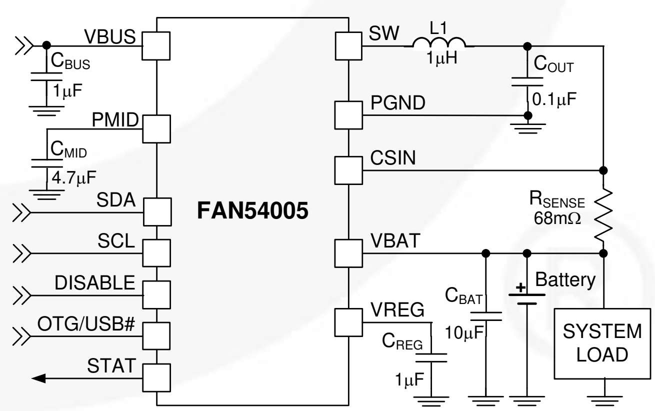


Figure 1. Typical Application

Ordering Information

Part Number	Temperature Range	Package	PN Bits: IC_INFO[4:2]	Packing Method
FAN54005UCX	-40 to 85°C	20-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch, 1.96 x 1.87 mm	101	Tape and Reel

Block Diagram

PMID	Q1A	Q1B
> V_{BAT}	ON	OFF
< V_{BAT}	OFF	ON

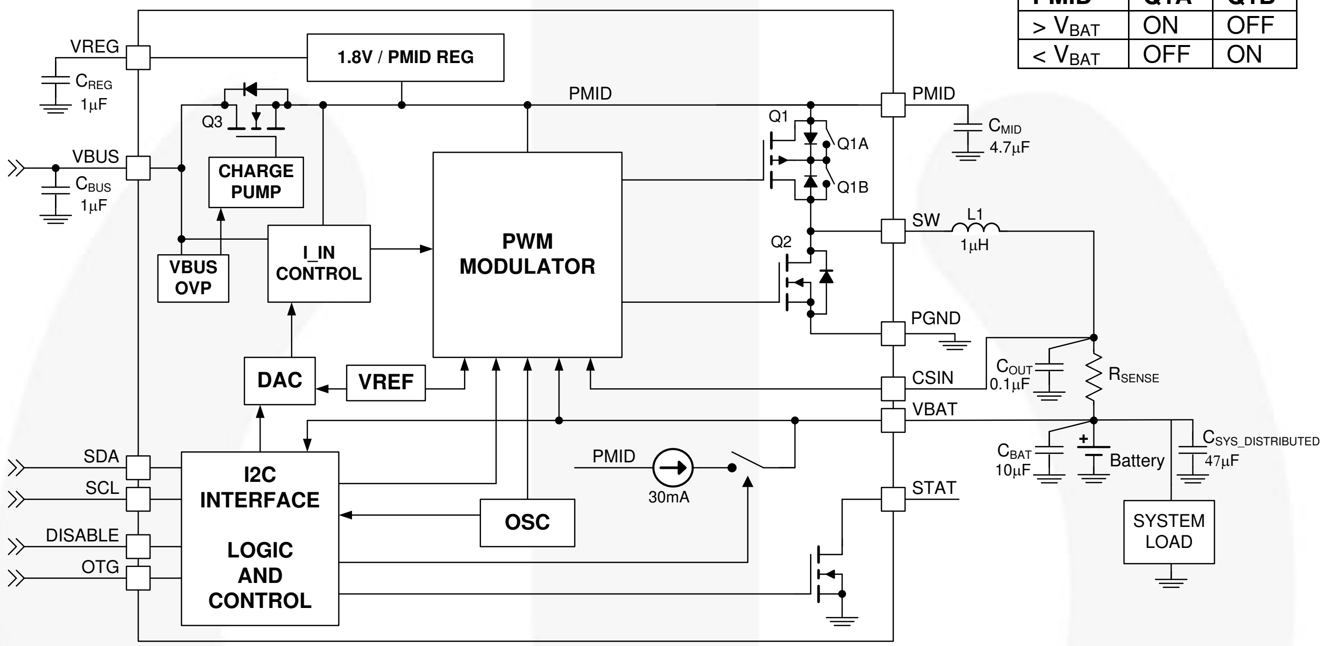


Figure 2. IC and System Block Diagram

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Unit
L1	1 μH ±20%, 4.0 A, 33 mΩ, 2016	Semco CIGT201610EH1R0M	L	1.0	μH
C_{BAT}	10 μF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M TDK: C1608X5R0J106M	C	10	μF
C_{MID}	4.7 μF, 10%, 10 V, X5R, 0603	Murata: GRM188R61A475K TDK: C1608X5R1A475K	C(1)	4.7	μF
C_{BUS}	1.0 μF, 10%, 25 V, X5R, 0603	Murata: GRM188R61E105K TDK: C1608X5R1E105M	C	1.0	μF
C_{REG}	1.0 μF, 10%, 10 V, X5R, 0402	Murata: GRM155R61A105K TDK: C1005X5R1A105K	C	1.0	μF
C_{OUT}	0.1 μF, 10%, 16 V, X7R, 0402	Murata: GRM155R71C104K TDK: C1005X7R1C104K	C	0.1	μF
$C_{SYS\_DISTRIBUTED}$ (2)	n/a	n/a	C	47	μF

Notes:

1. A 10 V rating is sufficient for C_{MID} because PMID is protected from over-voltage surges on VBUS by Q3 (Figure 2).
2. A minimum 47 μF of distributed capacitance on SYS is required for proper operation of the FAN54005.

Pin Configuration

Figure 3. WLCSP-20 Pin Assignments

Pin Definitions

Pin #	Name	Description
A1, A2	VBUS	**Charger Input Voltage** and USB-OTG output voltage. Bypass with a 1 µF capacitor to PGND.
A3	NC	**No Connect**. No external connection is made between this pin and the IC's internal circuitry.
A4	SCL	**I^2C Interface Serial Clock**. This pin should not be left floating.
B1-B3	PMID	**Power Input Voltage**. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 µF, 6.3 V capacitor to PGND.
B4	SDA	**I^2C Interface Serial Data**. This pin should not be left floating.
C1-C3	SW	**Switching Node**. Connect to output inductor.
C4	STAT	**Status**. Open-drain output indicating charge status. The IC pulls this pin LOW when charging.
D1-D3	PGND	**Power Ground**. Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{MID} should be as short as possible.
D4	OTG	**On-The-Go**. On VBUS Power-On Reset (POR), this pin sets the input current limit for t_{15MIN} charging. Also, the OTG pin enables the boost regulator in conjunction with OTG_EN and OTG_PL bits *(See Table 15)*
E1	CSIN	**Current-Sense Input**. Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin close to R_{SENSE} with a 0.1 µF capacitor to PGND.
E2	DISABLE	**Charge Disable**. If this pin is HIGH, charging is disabled. When LOW, charging is controlled by the I^2C registers. When this pin is HIGH, the 15-minute timer is reset. This pin does not affect the 32-second timer.
E3	VREG	**Regulator Output**. Connect to a 1 µF capacitor to PGND. This pin provides regulated 1.8 V and can supply up to 2mA of DC load current.
E4	VBAT	**Battery Voltage**. Connect to the positive (+) terminal of the battery pack and close to R_{SENSE}.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	VBUS Voltage	Continuous	-0.7	20.0	V
		Pulsed, 100 ms Maximum Non-Repetitive	-1.0		
V_{STAT}	STAT Voltage		-0.3	16.0	V
V_I	PMID Voltage			7.0	V
	SW, CSIN, VBAT, DISABLE Voltage		-0.3	7.0	
V_O	Voltage on Other Pins		-0.3	6.5[3]	V
$\frac{dV_{BUS}}{dt}$	Maximum V_{BUS} Slope above 5.5 V when Boost or Charger are Active			4	V/µs
$-\frac{dV_{BUS}}{dt}$	Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \le 4.7\ \mu F$ *(See VBUS Short While Charging)*	$T_A \le 60°C$		4	V/µs
		$T_A \ge 60°C$		2	
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2000		V
		Charged Device Model per JESD22-C101	1000		
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
3. Lesser of 6.5 V or V_I + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	Supply Voltage	4	6	V
$V_{BAT(MAX)}$	Maximum Battery Voltage when Boost enabled		4.5	V
T_A	Ambient Temperature	-30	+85	°C
T_J	Junction Temperature *(See Thermal Regulation and Protection section)*	-30	+120	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A. *For measured data, see Thermal Regulation and Protection.*

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	60	°C/W
θ_{JB}	Junction-to-PCB Thermal Resistance	20	°C/W

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for T_J=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_{VBUS}	VBUS Current	$V_{BUS} > V_{IN(MIN)1}$, PWM Switching		10		mA
		$V_{BUS} > V_{IN(MIN)1}$; PWM Enabled, Not Switching (Battery OVP Condition); I_IN Setting=100 mA		2.5		mA
		0°C < T_J < 85°C, HZ_MODE=1, 32S Mode		63	90	µA
I_{LKG}	VBAT to VBUS Leakage Current	0°C < T_J < 85°C, HZ_MODE=1, V_{BAT}=4.2 V, V_{BUS}=0 V		0.2	5.0	µA
I_{BAT}	Battery Discharge Current in High-Impedance Mode	0°C < T_J < 85°C, HZ_MODE=1, V_{BAT}=4.2 V			10	µA
		DISABLE=1, 0°C < T_J < 85°C, V_{BAT}=4.2 V			10	
Charger Voltage Regulation						
V_{OREG}	Charge Voltage Range		3.5		4.4	V
	Charge Voltage Accuracy	T_A=25°C	-0.5%		+0.5%	
		T_J=0 to 125°C	-1%		+1%	
Charging Current Regulation						
$I_{OCHARGE}$	Output Charge Current Range	$V_{SHORT} < V_{BAT} < V_{OREG}$, R_{SENSE}=68 mΩ	550		1450	mA
	Charge Current Accuracy Across R_{SENSE}	20 mV ≤ [$V_{CSIN} - V_{BAT}$] ≤ 40 mV	92	97	102	%
		[$V_{CSIN} - V_{BAT}$] > 40 mV	94	97	100	%
Weak Battery Detection						
V_{LOWV}	Weak Battery Threshold Range		3.4		3.7	V
	Weak Battery Threshold Accuracy		-5		+5	%
	Weak Battery Deglitch Time	Rising Voltage		30		ms
Logic Levels: DISABLE, SDA, SCL, OTG						
V_{IH}	High-Level Input Voltage		1.05			V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{BUS}		0.01	1.00	µA
Charge Termination Detection						
I_{TERM}	Termination Current Range	$V_{BAT} > V_{OREG} - V_{RCH}$, R_{SENSE}=68 mΩ	50		400	mA
	Termination Current Accuracy	[$V_{CSIN} - V_{BAT}$] from 3 mV to 20 mV	-25		+25	%
		[$V_{CSIN} - V_{BAT}$] from 20 mV to 40 mV	-5		+5	
	Termination Current Deglitch Time			30		ms
1.8 V Linear Regulator						
V_{REG}	1.8 V Regulator Output	I_{REG} from 0 to 2 mA	1.7	1.8	1.9	V
Input Power Source Detection						
$V_{IN(MIN)1}$	VBUS Input Voltage Rising	To Initiate and Pass VBUS Validation		4.29	4.42	V
$V_{IN(MIN)2}$	Minimum VBUS During Charge	During Charging		3.71	3.94	V
t_{VBUS_VALID}	VBUS Validation Time			30		ms

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for T_J=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dynamic Input Voltage Control (V_{BUS})						
V_{SP}	DIVC Accuracy		-3		+3	%
Input Current Limit						
I_{INLIM}	Input Current Limit Threshold	I_{INLIM} Set to 100 mA	88	93	98	mA
		I_{INLIM} Set to 500 mA	450	475	500	mA
V_{REF} Bias Generator						
V_{REF}	Bias Regulator Voltage	$V_{BUS} > V_{IN(MIN)1}$			6.5	V
	Short-Circuit Current Limit			20		mA
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below V_{OREG}	100	120	150	mV
	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		130		ms
STAT Output						
$V_{STAT(OL)}$	STAT Output Low	I_{STAT}=10 mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT}=5 V			1	µA
Battery Detection						
I_{DETECT}	Battery Detection Current before Charge Done (Sink Current)(4)	Begins after Termination Detected and $V_{BAT} \leq V_{OREG} - V_{RCH}$		-0.80		mA
t_{DETECT}	Battery Detection Time			262		ms
Sleep Comparator						
V_{SLP}	Sleep-Mode Entry Threshold, $V_{BUS} - V_{BAT}$	2.3 V $\leq V_{BAT} \leq V_{OREG}$, V_{BUS} Falling	0	0.04	0.10	V
t_{SLP_EXIT}	Deglitch Time for VBUS Rising Above V_{BAT} by V_{SLP}	Rising Voltage		30		ms
Power Switches *(See Figure 2)*						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID)	I_{INLIM}=500 mA		180	250	mΩ
	Q1 On Resistance (PMID to SW)			130	225	mΩ
	Q2 On Resistance (SW to GND)			150	225	mΩ
Charger PWM Modulator						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			0		%
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold(5)	Low-Side MOSFET (Q2) Cycle-by-Cycle Current Limit		140		mA
Boost Mode Operation (OPA_MODE=1, HZ_MODE=0)						
V_{BOOST}	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 200 mA	4.80	5.07	5.17	V
		3.0 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 500 mA	4.77	5.07	5.17	V
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT}=3.6 V, I_{OUT}=0		140	300	µA
$I_{LIMPK(BST)}$	Q2 Peak Current Limit		1440	1700	1960	mA
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.30		V
		To Start Boost Regulator		2.50	2.70	V

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for T_J=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VBUS Load Resistance						
R_{VBUS}	VBUS to PGND Resistance	Normal Operation		1500		kΩ
		Charger Validation		100		Ω
Protection and Timers						
$VBUS_{OVP}$	VBUS Over-Voltage Shutdown	V_{BUS} Rising	6.09	6.29	6.49	V
	Hysteresis	V_{BUS} Falling		100		mV
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle Peak Current Limit	Charge Mode		2.3		A
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	1.95	2.00	2.05	V
	Hysteresis	V_{BAT} Falling		100		mV
I_{SHORT}	Linear Charging Current	$V_{BAT} < V_{SHORT}$	20	30	40	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold(6)	T_J Rising		145		°C
	Hysteresis(6)	T_J Falling		10		
T_{CF}	Thermal Regulation Threshold(6)	Charge Current Reduction Begins		120		°C
t_{INT}	Detection Interval			2.1		s
t_{32S}	32-Second Timer(7)	Charger Enabled	20.5	25.2	28.0	s
		Charger Disabled	18.0	25.2	34.0	
t_{15MIN}	15-Minute Timer	15-Minute Mode	12.0	13.5	15.0	min
Δt_{LF}	Low-Frequency Timer Accuracy	Charger Inactive	-25		25	%

Notes:

4. Negative current is current flowing from the battery to GND (discharging the battery).
5. Q2 always turns on for 60 ns, then turns off if current is below I_{SYNC}.
6. Guaranteed by design; not tested in production.
7. This tolerance (%) applies to all timers on the IC, including soft-start and deglitching timers.

I²C Timing Specifications

Guaranteed by design, $V_{BAT}\geq 2.5$ V if valid VBUS not present.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, $C_B \leq 100$ pF			3400	
		High-Speed Mode, $C_B \leq 400$ pF			1700	
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		High-Speed Mode, $C_B \leq 100$ pF		160		ns
		High-Speed Mode, $C_B \leq 400$ pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \leq 100$ pF		60		ns
		High-Speed Mode, $C_B \leq 400$ pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \leq 100$ pF	0		70	ns
		High-Speed Mode, $C_B \leq 400$ pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	40	
		High-Speed Mode, $C_B \leq 400$ pF		20	80	
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	

Continued on the following page…

I²C Timing Specifications

Guaranteed by design, $V_{BAT} \geq 2.5$ V if valid VBUS not present.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA, SCL				400	pF

Timing Diagrams

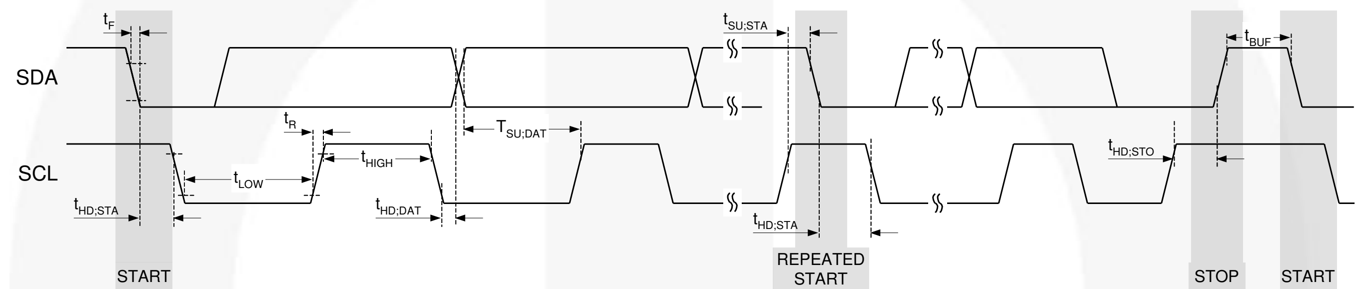
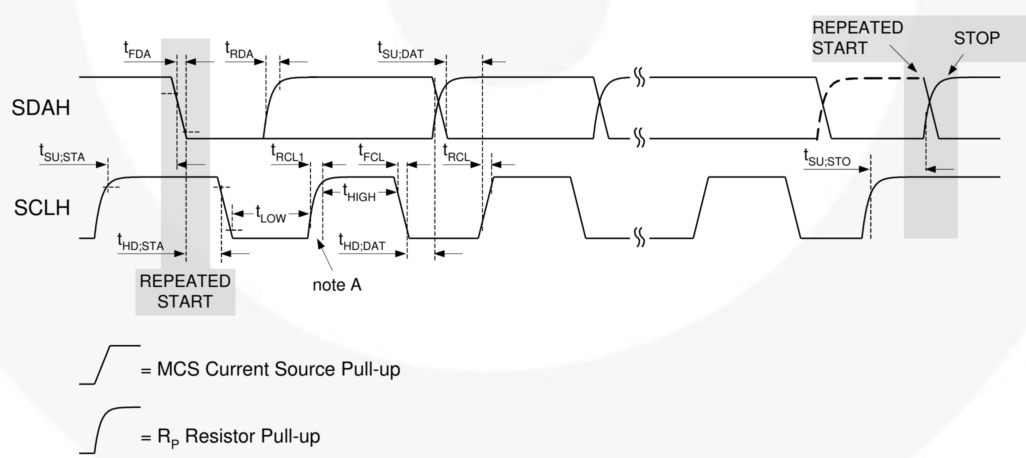


Figure 4. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 5. I²C Interface Timing for High-Speed Mode

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

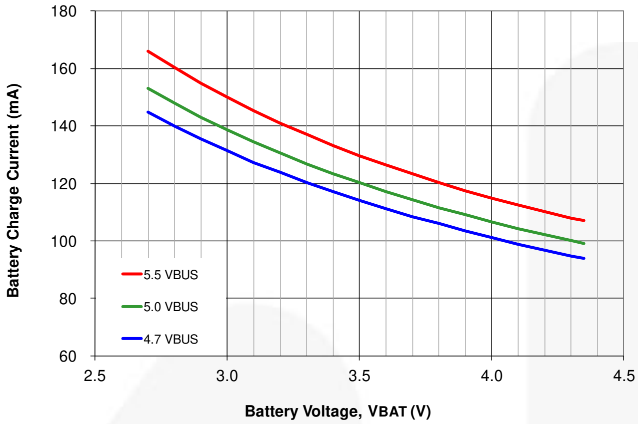


Figure 6. Battery Charge Current vs. V_{BUS} with I_{INLIM}=100 mA, V_{OREG}=4.35V

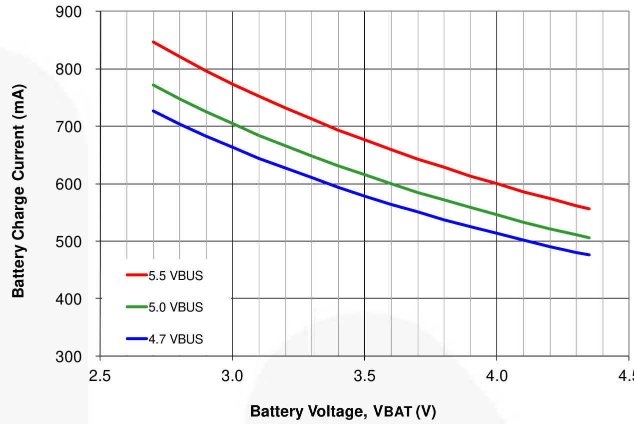


Figure 7. Battery Charge Current vs. V_{BUS} with I_{INLIM}=500 mA, V_{OREG}=4.35V

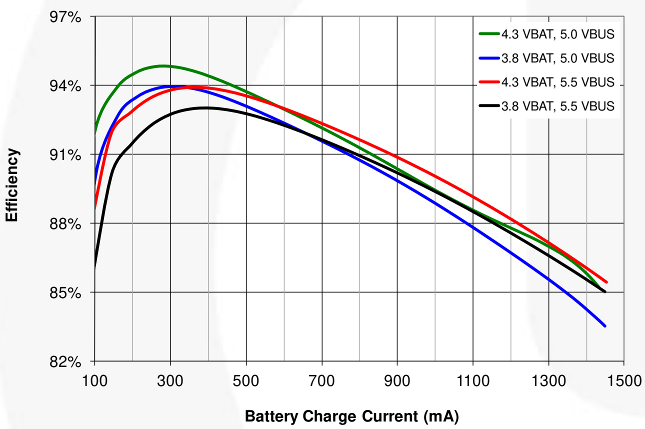


Figure 8. Charger Efficiency, No I_{INLIM},$I_{OCHARGE}$=1450 mA

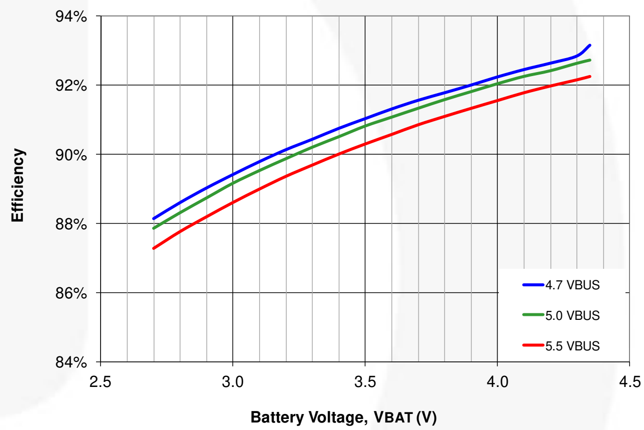


Figure 9. Charger Efficiency vs. V_{BUS}, I_{INLIM}=500 mA, V_{OREG}=4.35

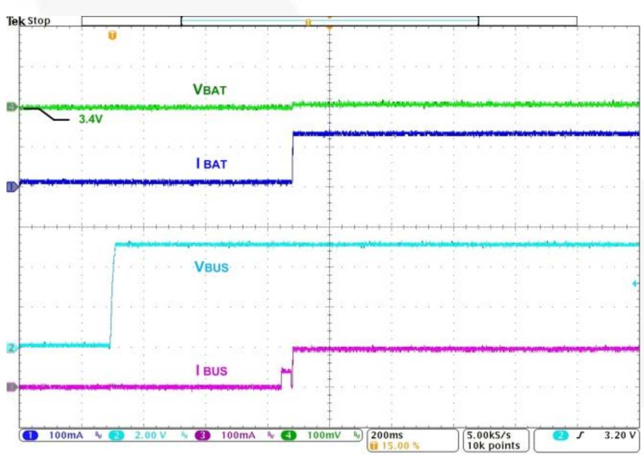


Figure 10. Auto-Charge Startup at VBUS Plug-in, OTG=0, V_{BAT}=3.4 V

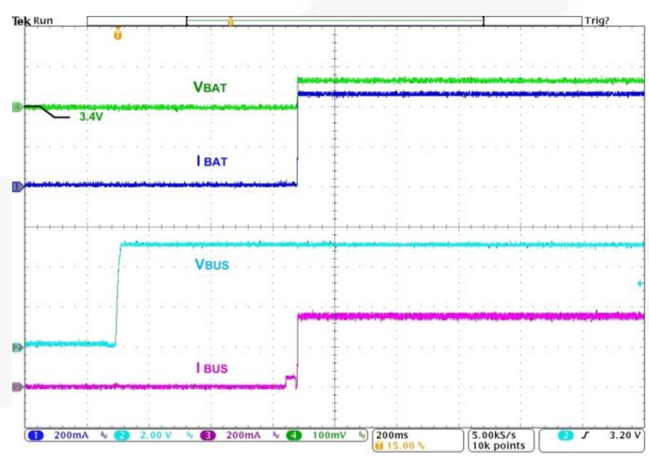


Figure 11. Auto-Charge Startup at VBUS Plug-in, OTG=1, V_{BAT}=3.4 V

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

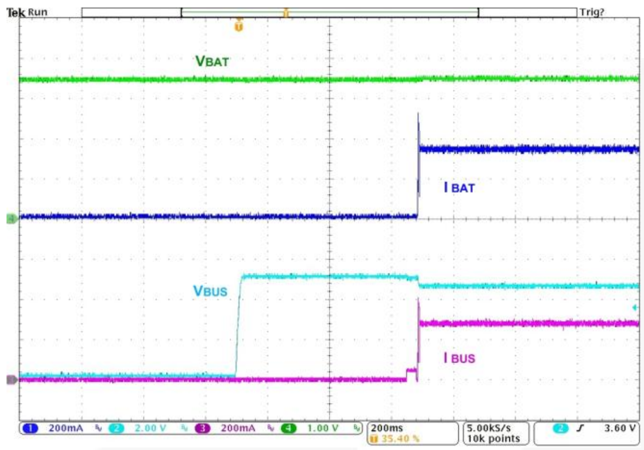


Figure 12. Auto-Charge Startup with 300 mA Limited Charger / Adaptor, OTG=1, V_{BAT}=3.4 V

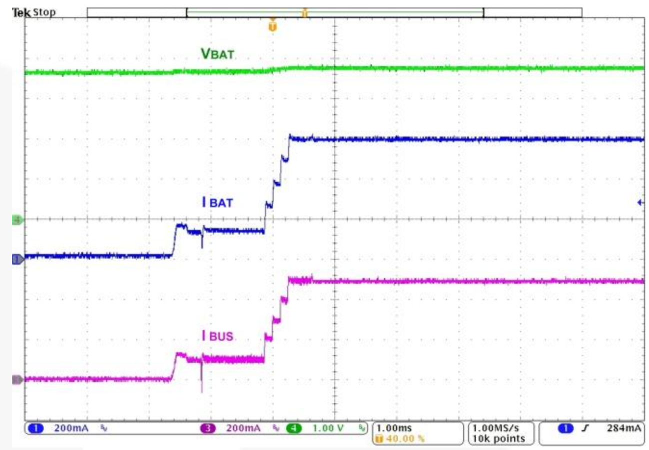


Figure 13. Charger Startup with HZ_MODE Bit Reset, I_{INLIM}=500 mA, $I_{OCHARGE}$=1050 mA, V_{OREG}=4.2 V, V_{BAT}=3.6 V

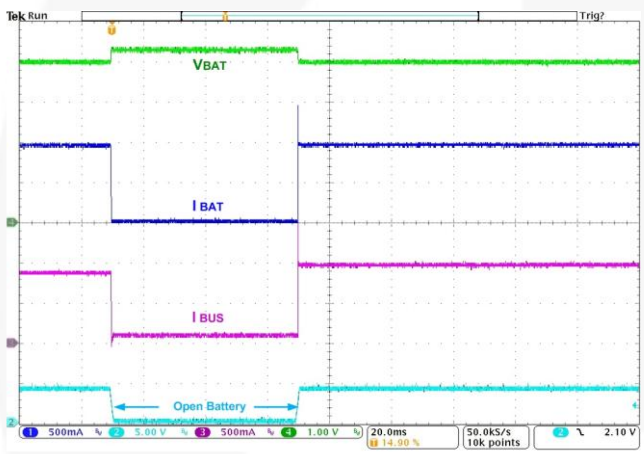


Figure 14. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=1050 mA, No I_{INLIM}, TE=0

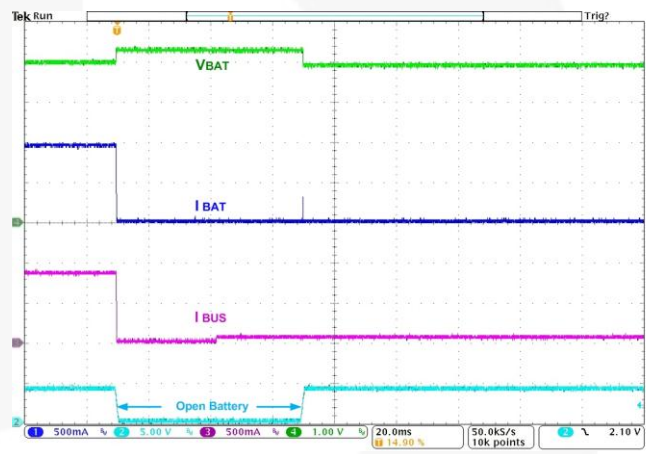


Figure 15. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=1050 mA, No I_{INLIM}, TE=1

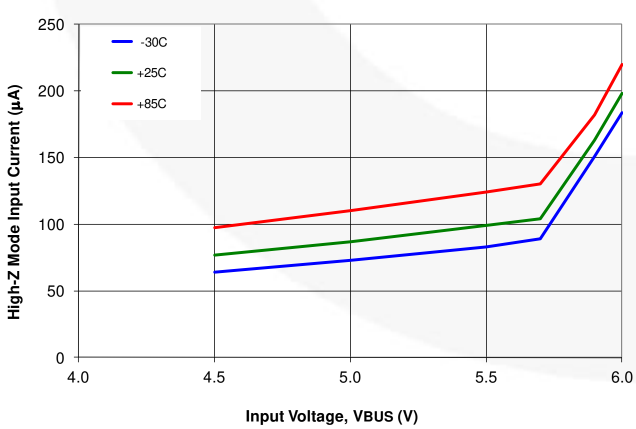


Figure 16. VBUS Current in High-Impedance Mode with Battery Open

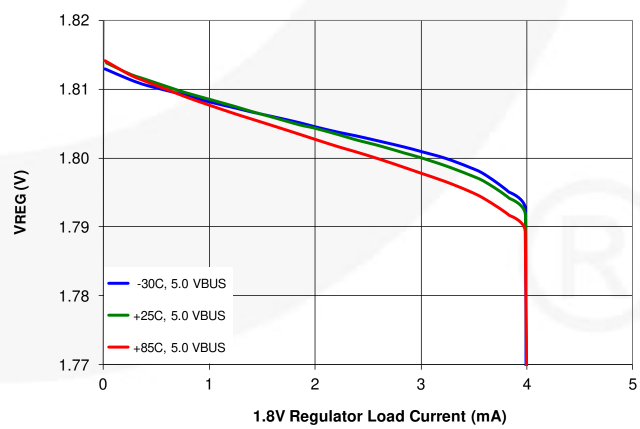


Figure 17. V_{REG} 1.8 V Output Regulation

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

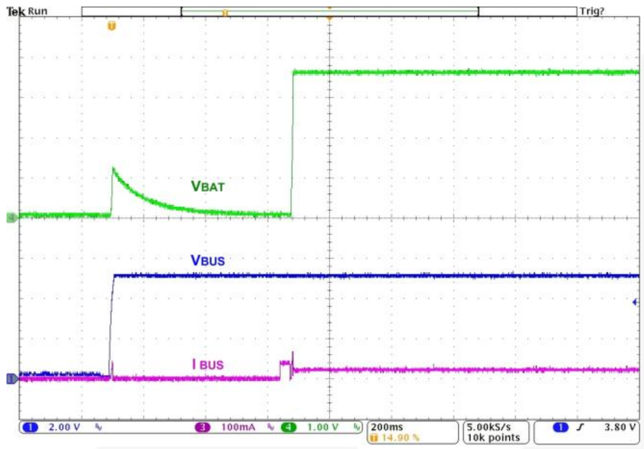


Figure 18. No Battery, TE=0, V_{BUS} Power Up

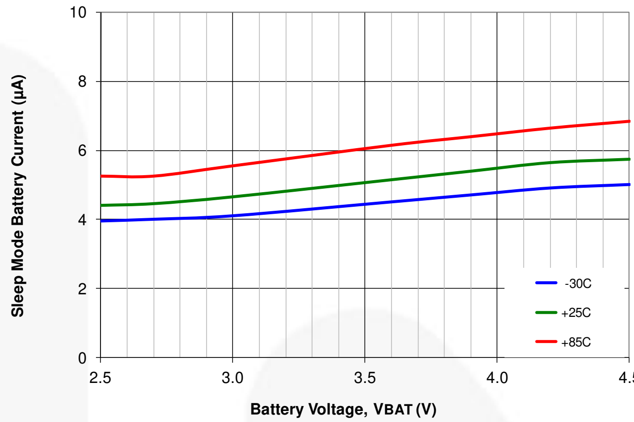


Figure 19. Sleep Mode Battery Discharge Current, SDA=SCL=0 V, VBUS open

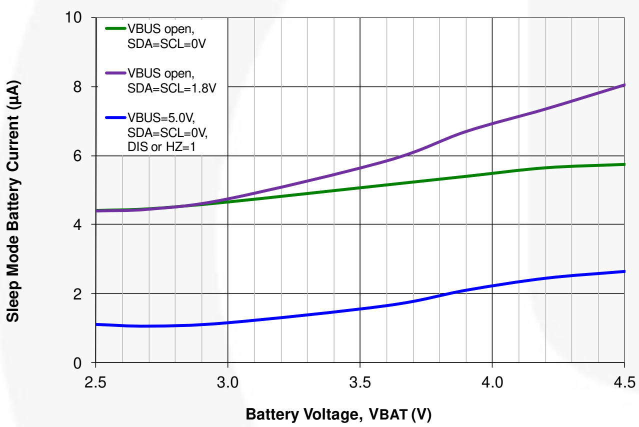


Figure 20. Battery Discharge Current vs. Mode

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1 V_{BAT}=3.6 V, T_A=25°C.

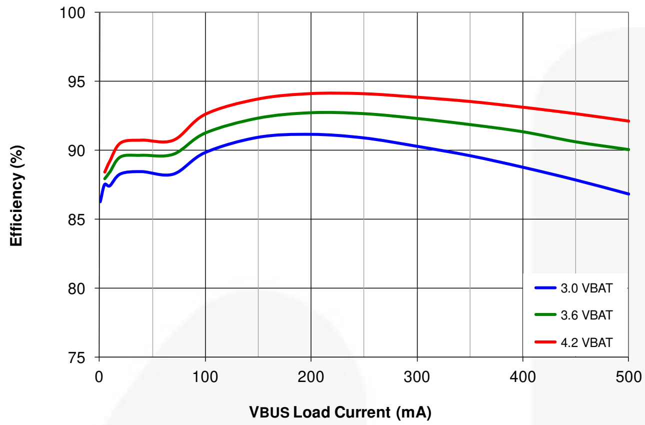


Figure 21. Efficiency vs. V_{BAT}

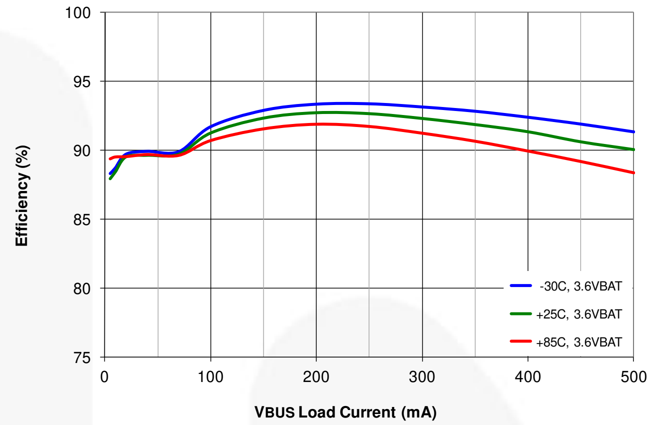


Figure 22. Efficiency Over-Temperature

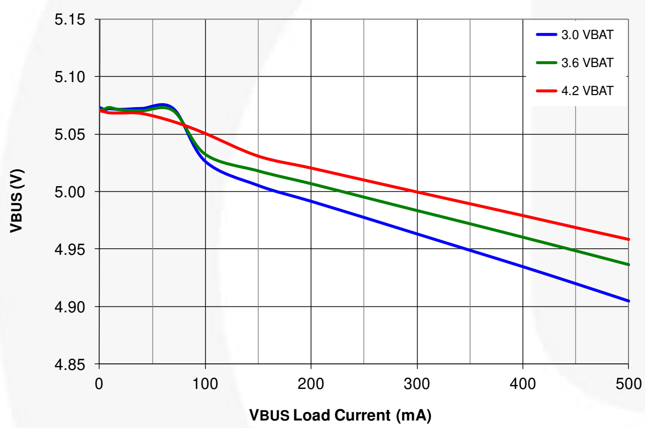


Figure 23. Output Regulation vs. V_{BAT}

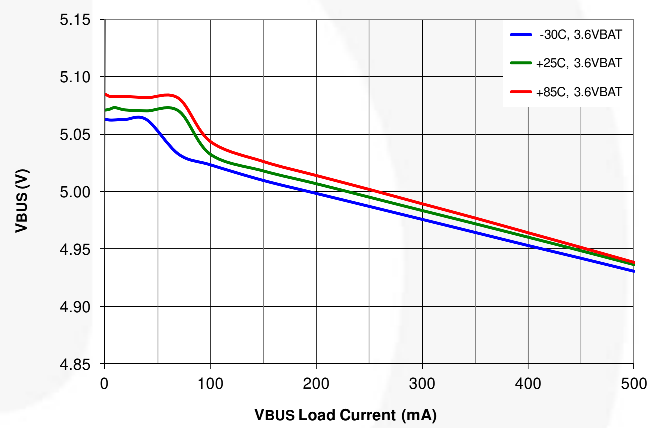


Figure 24. Output Regulation Over-Temperature

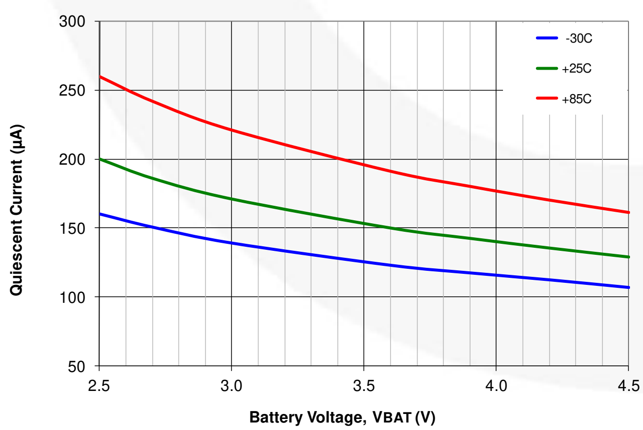


Figure 25. Quiescent Current

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1 V_{BAT}=3.6 V, T_A=25°C.

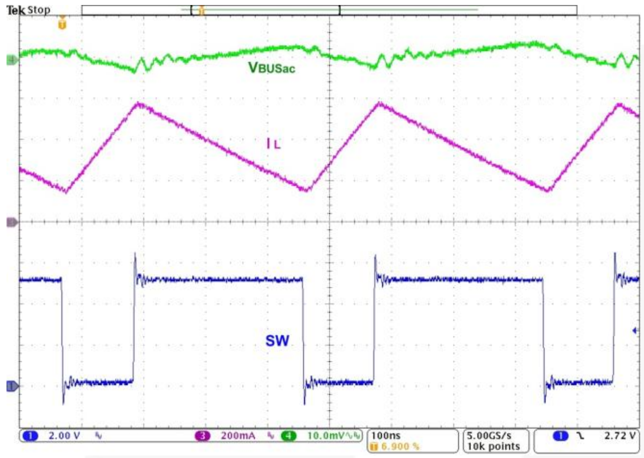


Figure 26. Boost PWM Waveform

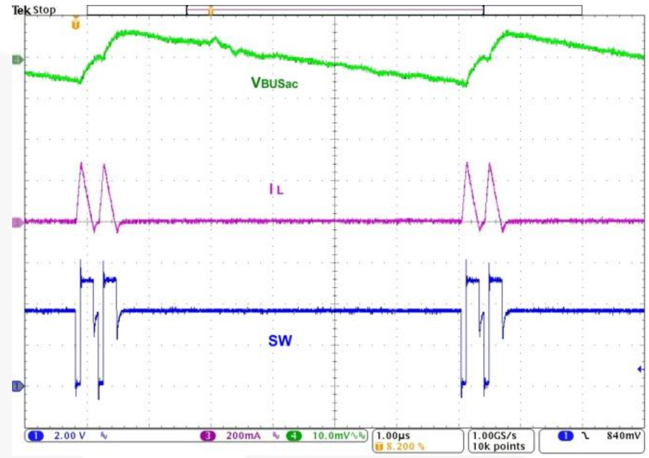


Figure 27. Boost PFM Waveform

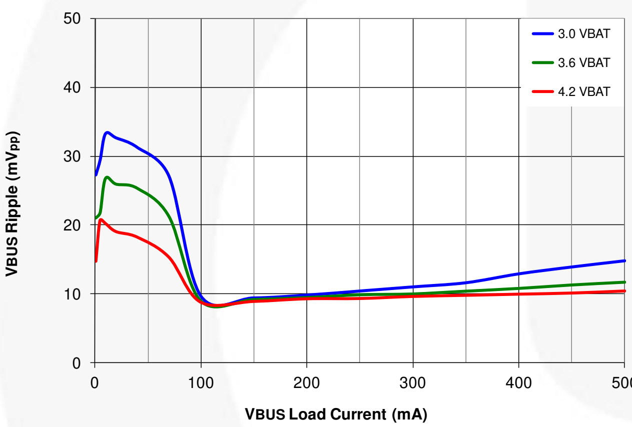


Figure 28. Output Ripple vs. V_{BAT}

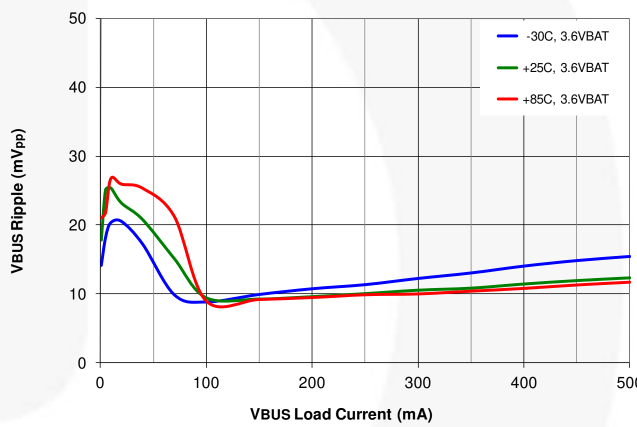


Figure 29. Output Ripple vs. Temperature

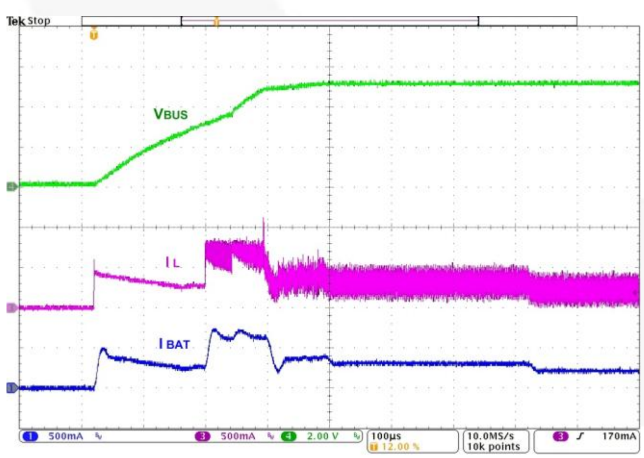


Figure 30. Startup, 3.6 V_{BAT}, 44 Ω Load, Additional 10 µF, X5R Across V_{BUS}

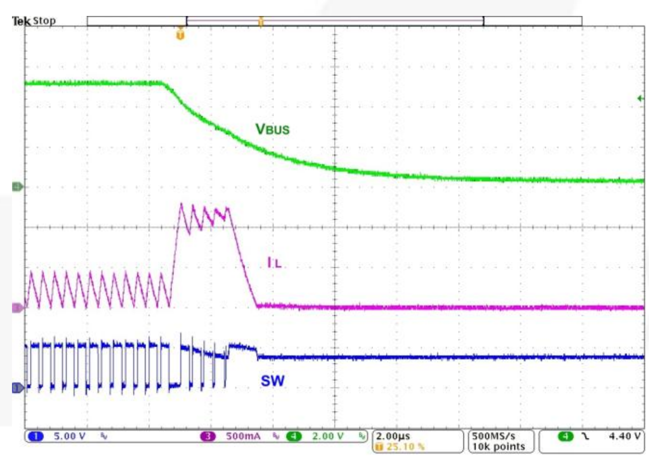


Figure 31. V_{BUS} Fault Response, 3.6 V_{BAT}

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1 V_{BAT}=3.6 V, T_A=25°C.

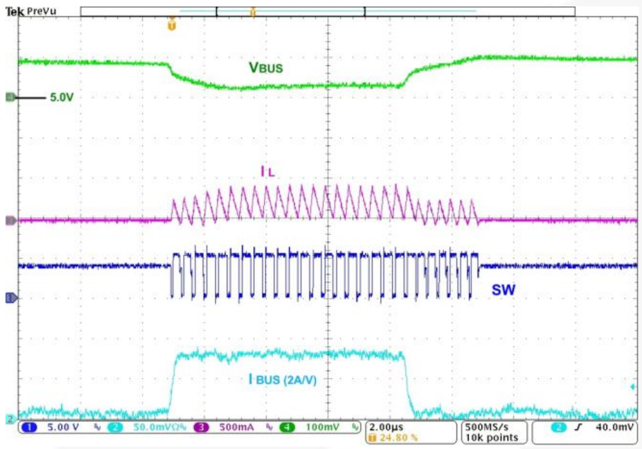


Figure 32. Load Transient, 5-155-5 mA, t_R=t_F=100 ns

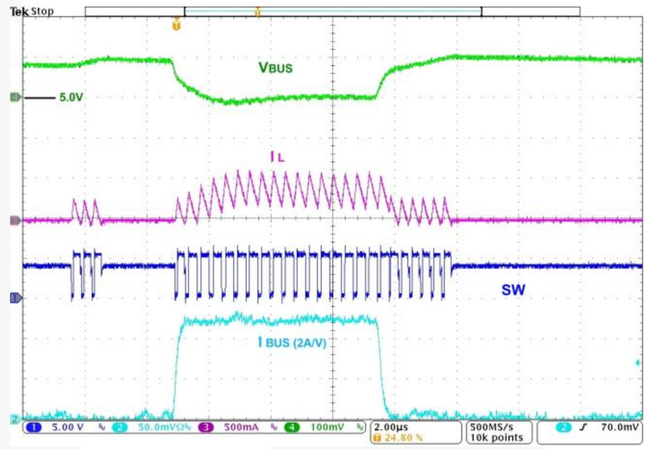


Figure 33. Load Transient, 5-255-5 mA, t_R=t_F=100 ns

Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

The FAN54005 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The FAN54005 employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN54005 has three operating modes:

1. Charge Mode:
   Charges a single-cell Li-ion or Li-polymer battery.
2. Boost Mode:
   Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
3. High-Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.

Charge Mode and Registers

Note: Default settings are denoted by **bold typeface**.

Charge Mode

In Charge Mode, FAN54005 employs four regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the threshold determined by I_{TERM}.
4. Temperature: If the IC's junction temperature reaches 120°C, charge current is reduced until the IC's temperature stabilizes at 120°C.
5. Dynamic Input Voltage Control (DIVC) limits the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate incompatible adapters that limit current to a lower current than might be available from a "normal" USB adapter.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

During the current regulation phase of charging, I_{INLIM} or the programmed charging current limits the amount of current available to charge the battery and power the system. The effect of I_{INLIM} on $I_{OCHARGE}$ can be seen in *Figure 35*.

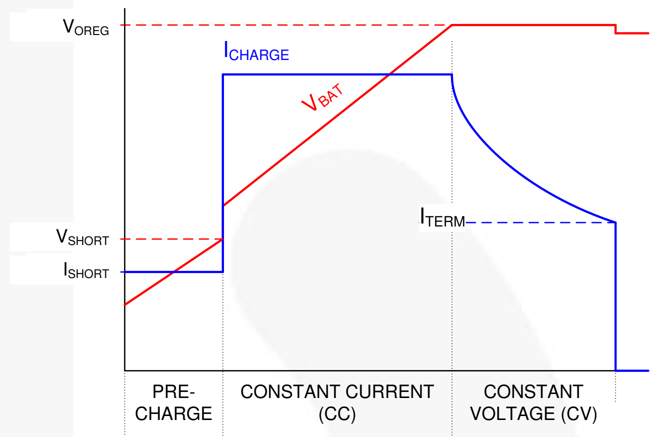


Figure 34. Charge Curve, $I_{OCHARGE}$ Not Limited by I_{INLIM}

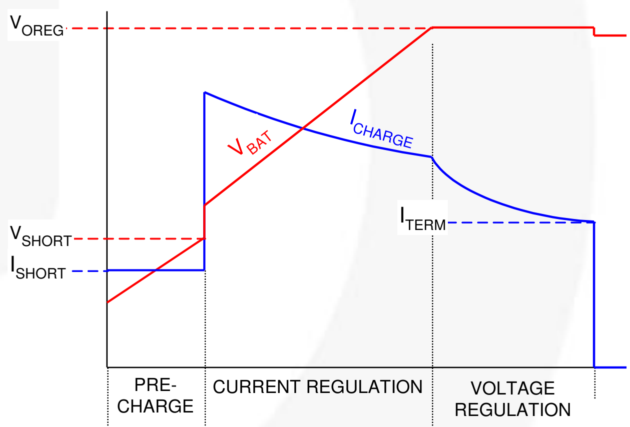


Figure 35. Charge Curve, I_{INLIM} Limits $I_{OCHARGE}$

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG 01[3]).

The charger output or "float" voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments as shown in Table 2.

Table 2. OREG Bits (REG 02[7:2]) vs. Charger V_{OUT} (V_{OREG}) Float Voltage

OREG Decimal	Hex	V_{OREG}	Decimal	Hex	V_{OREG}
0	00	3.50	32	20	4.14
1	01	3.52	33	21	4.16
2	**02**	**3.54**	34	22	4.18
3	03	3.56	35	23	4.20
4	04	3.58	36	24	4.22
5	05	3.60	37	25	4.24
6	06	3.62	38	26	4.26
7	07	3.64	39	27	4.28
8	08	3.66	40	28	4.30
9	09	3.68	41	29	4.32
10	0A	3.70	42	2A	4.34
11	0B	3.72	43	2B	4.36
12	0C	3.74	44	2C	4.38
13	0D	3.76	45	2D	4.40
14	0E	3.78	46	2E	4.42
15	0F	3.80	47	2F	4.44
16	10	3.82	48	30	4.44
17	11	3.84	49	31	4.44
18	12	3.86	50	32	4.44
19	13	3.88	51	33	4.44
20	14	3.90	52	34	4.44
21	15	3.92	53	35	4.44
22	16	3.94	54	36	4.44
23	17	3.96	55	37	4.44
24	18	3.98	56	38	4.44
25	19	4.00	57	39	4.44
26	1A	4.02	58	3A	4.44
27	1B	4.04	59	3B	4.44
28	1C	4.06	60	3C	4.44
29	1D	4.08	61	3D	4.44
30	1E	4.10	62	3E	4.44

The following charging parameters can be programmed by the host through I^{2}C:

Table 3. Programmable Charging Parameters

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG 02[7:2]
Battery Charging Current Limit	$I_{OCHARGE}$	REG 04[6:4]
Input Current Limit	I_{INLIM}	REG 01[7:6]
Charge Termination Limit	I_{TERM}	REG 04[2:0]
Weak Battery Voltage	V_{LOWV}	REG 01[5:4]

A new charge cycle begins when one of the following occurs:

- The battery voltage falls below $V_{OREG} - V_{RCH}$
- VBUS Power on Reset (POR)
- $\overline{CE}$ or HZ_MODE is reset through I^{2}C write to CONTROL1 (REG 01) register.

Charge Current Limit ($I_{OCHARGE}$)

Charge current is limited by the IO_LEVEL (Reg 05[5]) bit by default (IO_LEVEL=1). This limits charge current to 500 mA when R_{SENSE}=68 mΩ and 340 mA when R_{SENSE}=100 mΩ. When IO_LEVEL=0 charge current is limited by the IOCHARGE bits.

Table 4. $I_{OCHARGE}$ Current as Function of IOCHARGE (REG 04 [6:4]) Bits and R_{SENSE} Resistor Values

IOCHARGE Decimal	HEX	V_{RSENSE} (mV)	$I_{OCHARGE}$ (mA) 68 mΩ	100 mΩ
0	**00**	**37.4**	**550**	**374**
1	01	44.2	650	442
2	02	51.0	750	510
3	03	57.8	850	578
4	04	71.4	1050	714
5	05	78.2	1150	782
6	06	91.8	1350	918
7	07	98.6	1450	986

Termination Current Limit

Current charge termination is enabled when TE (REG 01[3])=1.

Table 5. I_{TERM} Current as Function of ITERM Bits (REG 04[2:0]) and R_{SENSE} Resistor Values

ITERM Decimal	HEX	V_{RSENSE} (mV)	I_{TERM} (mA) 68 mΩ	100 mΩ
0	00	3.3	49	33
1	**01**	**6.6**	**97**	**66**
2	02	9.9	146	99
3	03	13.2	194	132
4	04	16.5	243	165
5	05	19.8	291	198
6	06	23.1	340	231
7	07	26.4	388	264

When the charge current falls below I_{TERM}, PWM charging stops and the STAT bits change to READY (00) for about 500 ms while the IC determines whether the battery and charging source are still connected. STAT then changes to CHARGE DONE (10), provided the battery and charger are still connected.

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a current limit that which off the FET when the current is negative by more than 140 mA peak. This prevents current flow from the battery.

Charger Operation

V_{BUS} Plug In

When the IC detects that V_{BUS} has risen above $V_{IN(MIN)1}$ (4.4 V), the IC applies a 100 Ω load from VBUS to GND. To clear the VBUS Power-On-Reset (POR) and begin charging, VBUS must remain above $V_{IN(MIN)1}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (30 ms) before the IC initiates charging.

The VBUS validation sequence always occurs before charging is initiated or re-initiated (for example, after a VBUS OVP fault or a V_{RCH} recharge initiation).

T_{VBUS_VALID} ensures that unfiltered 50 / 60 Hz chargers and other non-compliant chargers are rejected.

Safety Timer

Section references Figure 39.

At the beginning of charging, the IC starts a 15-minute timer (t_{15MIN}). When this times out, charging is terminated. Writing to any register through I^2C stops and resets the t_{15MIN} timer, which in turn starts a 32-second timer (t_{32S}). Setting the TMR_RST bit (REG 00[7]) resets the t_{32S} timer. If the t_{32S} timer times out; charging is terminated, all registers (except Safety) are set to their default values, the FAULT bits are set to 110, STAT is pulsed HIGH and returns LOW, and charging resumes using the default values with the t_{15MIN} timer running.

Normal charging is controlled by the host with the t_{32S} timer running to ensure that the host is alive. Charging with the t_{15MIN} timer running is used for charging that is unattended by the host. If the t_{15MIN} timer expires; the IC turns off the charger, sets the $\overline{CE}$ bit, and indicates a timer fault (110) on the FAULT bits (REG 00[2:0]). This sequence prevents overcharge if the host fails to reset the t_{32S} timer.

USB-Friendly Boot Sequence

At VBUS POR, the IC operates in accordance with its I^2C register settings. If no registers have been written (including Safety, and the TMR_RST bit), typically due to an absence of host communication, the chargers input current limit is controlled by the OTG pin (100 mA if OTG is LOW and 500 mA if OTG is HIGH).

Once the host processor begins writing to the IC, charging parameters are set by the host, which must continually reset the t_{32S} timer to continue charging using the programmed charging parameters.

Input Current Limiting

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the IINLIM bits (REG 01[7:6]).

Table 6. Input Current Limit

IINLIM REG 01[7:6]	Input Current Limit
00	100 mA
01	**500 mA**
10	800 mA
11	No limit

The OTG pin establishes the input current limit when t_{15MIN} is running.

Flow Charts

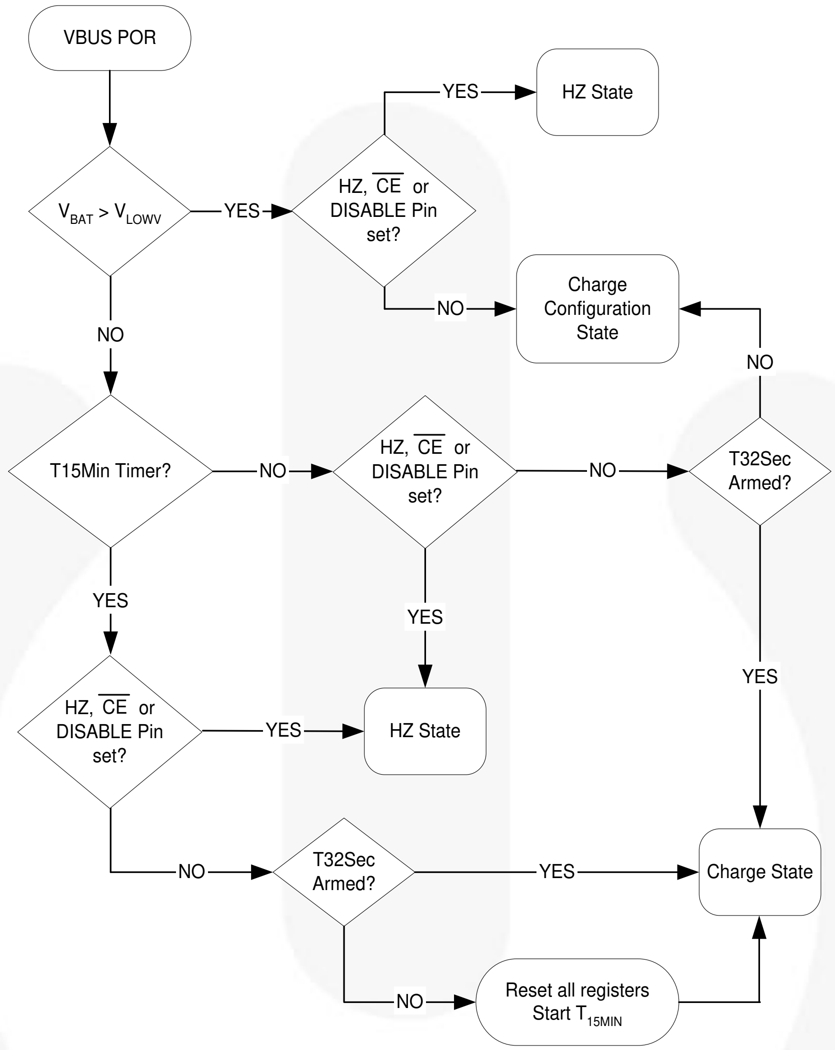


Figure 36. Charger VBUS POR

Flow Charts (Continued)

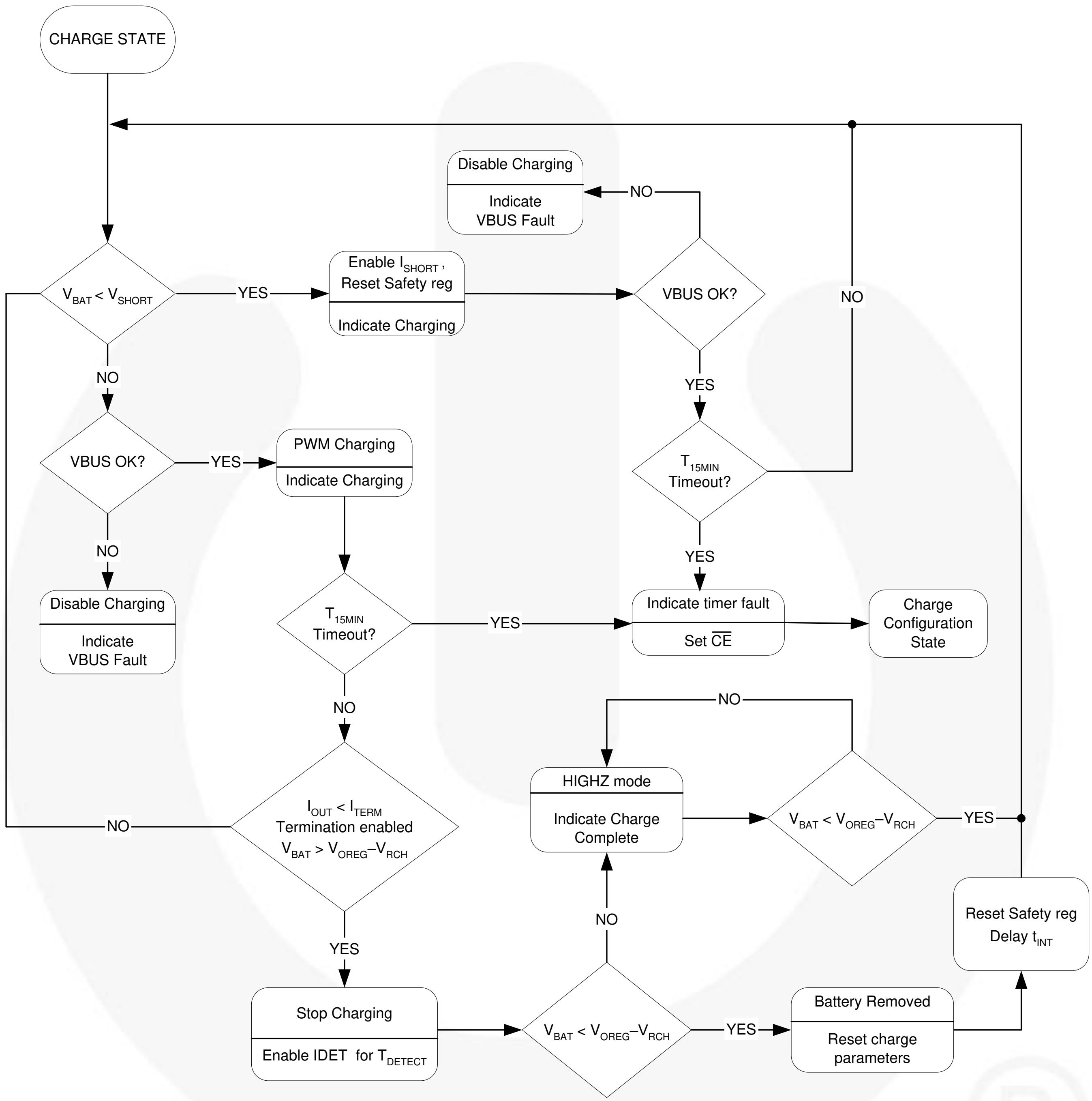


Figure 37. Charge Mode

Flow Charts (Continued)

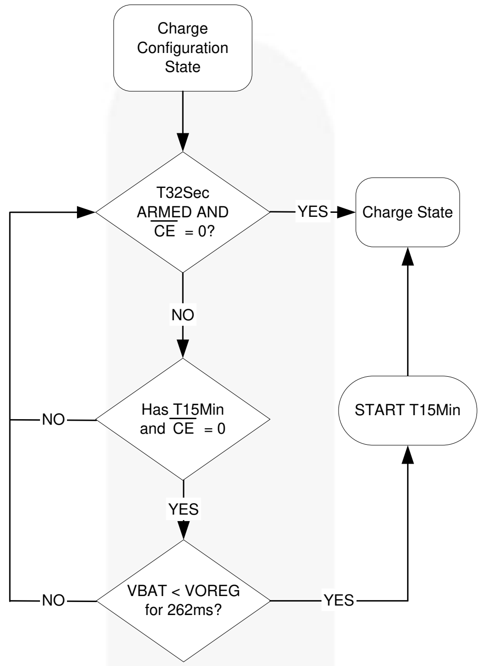


Figure 38. Charge Configuration

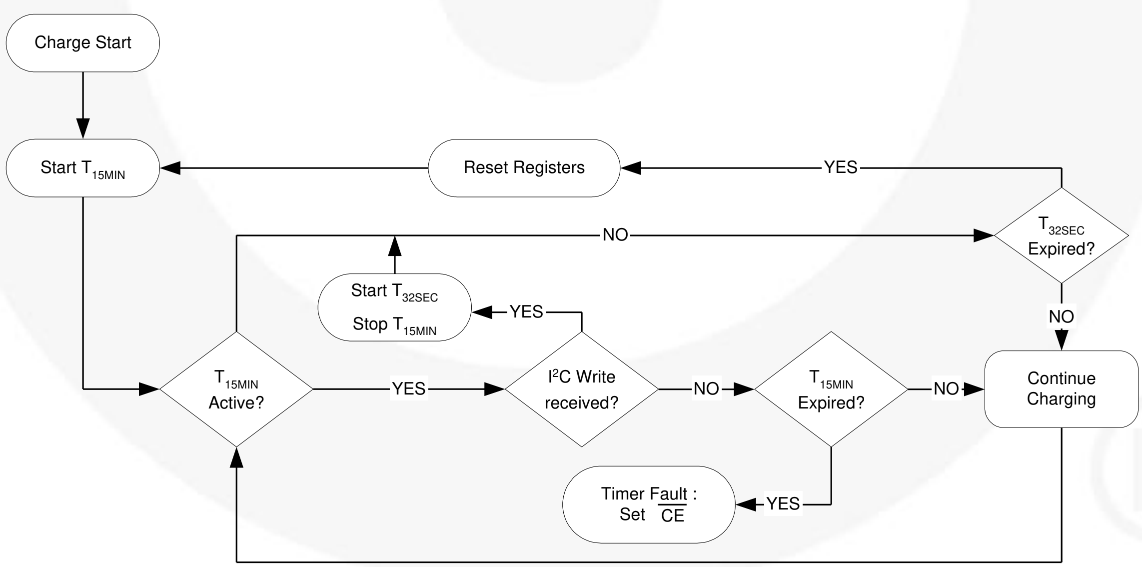


Figure 39. Timer Flow Chart

Dynamic Input Voltage Control

The FAN54005 has functionality that limits input current in case a current-limited incompatible adapter is supplying VBUS. These slowly increase the charging current until either:

- I_{INLIM} or $I_{OCHARGE}$ is reached

or

- $V_{BUS}=V_{SP}$.

If V_{BUS} collapses to V_{SP} when the current is ramping up, the FAN54005 charges with an input current that keeps $V_{BUS}=V_{SP}$. When the V_{SP} control loop is limiting the charge current, the SP bit (REG 05[4]) is set.

Table 7. V_{SP} as Function of VSP Bits (REG 05[2:0])

VSP		
Decimal	HEX	V_{SP}
0	00	4.213
1	01	4.293
2	02	4.373
3	03	4.453
4	**04**	4.533
5	05	4.613
6	06	4.693
7	07	4.773

Safety Settings

FAN54005 contain a SAFETY register (REG 06) that prevents the values in OREG (REG 02[7:2]) and IOCHARGE (REG 04[6:4]) from exceeding the values of the VSAFE and ISAFE values. *Refer to Table 8 and Table 9 for details*.

After V_{BAT} exceeds V_{SHORT}, the SAFETY register is loaded with its default value and may be written only before any other register is written. The entire desired Safety register value should be written twice to ensure the register bits are set. After writing to any other register, the SAFETY register is locked until V_{BAT} falls below V_{SHORT}.

The ISAFE (REG 06[6:4]) and VSAFE (REG 06[3:0]) registers establish values that limit the maximum values of $I_{OCHARGE}$ and V_{OREG} used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.

Table 8. I_{SAFE} ($I_{OCHARGE}$ Limit) as Function of ISAFE Bits (REG 06[6:4])

ISAFE				
Decimal	HEX	V_{RSENSE} (mV)	I_{SAFE} (mA)	
			68 mΩ	100 mΩ
0	00	37.4	550	374
1	01	44.2	650	442
2	02	51.0	750	510
3	03	57.8	850	578
4	**04**	**71.4**	**1050**	**714**
5	05	78.2	1150	782
6	06	91.8	1350	918
7	07	98.6	1450	986

Table 9. V_{SAFE} (V_{OREG} Max. Limit) as Function of VSAFE Bits (REG 06[3:0])

VSAFE			
Decimal	HEX	Max. OREG (REG 02[7:2])	V_{OREG} Max. (V)
0	**00**	**100011**	**4.20**
1	01	100100	4.22
2	02	100101	4.24
3	03	100110	4.26
4	04	100111	4.28
5	05	101000	4.30
6	06	101001	4.32
7	07	101010	4.34
8	08	101011	4.36
9	09	101100	4.38
10	0A	101101	4.40
11	0B	101110	4.42
12	0C	101111	4.44
13	0D	110000	4.44
14	0E	110001	4.44
15	0F	110010	4.44

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{CF} (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.

Additional θ_{JA} data points, measured using the FAN54005 evaluation board, are given in Table 10 (measured with T_A=25°C). Note that as power dissipation increases, the effective θ_{JA} decreases due to the larger difference between the die temperature and ambient.

Table 10. Evaluation Board Measured θ_{JA}

Power (W)	θ_{JA}
0.504	54°C/W
0.844	50°C/W
1.506	46°C/W

Charge Mode Input Supply Protection

Sleep Mode

When V_{BUS} falls below V_{BAT} + V_{SLP}, and V_{BUS} is above $V_{IN(MIN)1}$, the IC enters Sleep Mode to prevent the battery from draining into VBUS. During Sleep Mode, reverse current is disabled by body switching Q1.

Input Supply Low-Voltage Detection

The IC continuously monitors VBUS during charging. If V_{BUS} falls below $V_{IN(MIN)2}$, the IC:

1. Terminates charging
2. Pulses the STAT pin, sets the STAT bits to 11, and sets the FAULT bits to 011.

If V_{BUS} recovers above the $V_{IN(MIN)1}$ rising threshold after time t_{INT} (about two seconds), the charging process is repeated. This function prevents the USB power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

Input Over-Voltage Detection

When V_{BUS} exceeds $VBUS_{OVP}$, the IC:

1. Turns off Q3
2. Suspends charging
3. Sets the FAULT bits to 001, sets the STAT bits to 11, and pulses the STAT pin.

When V_{BUS} falls about 100 mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after V_{BUS} is revalidated.

VBUS Short While Charging

If VBUS is shorted with a very low impedance while the IC is charging with $I_{INLIMIT}$ =100 mA, the IC may not meet datasheet specifications until power is removed. To trigger this condition, V_{BUS} must be driven from 5 V to GND with a high slew rate. Achieving this slew rate requires a 0 Ω short from GND to the USB cable that is less than 10 cm from the connector.

Charge Mode Battery Detection & Protection

VBAT Over-Voltage Protection

The OREG voltage regulation loop prevents V_{BAT} from overshooting the OREG voltage by more than 50 mV when the battery is removed. When the PWM charger runs with no battery, the TE bit is not set, and a battery is inserted that is charged to a voltage higher than V_{OREG}; PWM pulses stop. If no further pulses occur for 30 ms, the IC sets the FAULT bits to 100, sets the STAT bits to 11, and pulses the STAT pin.

Battery Detection during Charging

The IC can detect the presence, absence, or removal of a battery if the termination bit (TE) is set. During normal charging, once V_{BAT} is close to V_{OREG} and the termination charge current is detected, the IC terminates charging and sets the STAT bits to 10. It then turns on a discharge current, I_{DETECT}, for t_{DETECT}. If V_{BAT} is still above V_{OREG} – V_{RCH}, the battery is present and the IC sets the FAULT bits to 000. If V_{BAT} is below V_{OREG} – V_{RCH}, the battery is absent and the IC:

1. Sets the registers to their default values.
2. Sets the FAULT bits to 111.
3. Resumes charging with default values after t_{INT}.

Battery Short-Circuit Protection

If the battery voltage is below the short-circuit threshold (V_{SHORT}); a linear current source, I_{SHORT}, supplies V_{BAT} until V_{BAT} > V_{SHORT}.

System Operation with No Battery

The FAN54005 continues charging after VBUS POR with the default parameters, regulating the V_{BAT} line to 3.54 V until the host processor issues commands or the t_{15MIN} timer expires. In this way, the FAN54005 can start the system without a battery.

The FAN54005 soft-start function can interfere with the system supply with battery absent. The soft-start activates whenever V_{OREG}, I_{INLIM}, or $I_{OCHARGE}$ are set from a lower to higher value. During soft-start, the I_{IN} limit drops to 100 mA for about 1 ms unless IINLIM is set to 11 (no limit). This could cause the system processor to fail to start. To avoid this behavior, use the following sequence.

1. Set the OTG pin HIGH. When VBUS is plugged in, I_{INLIM} is set to 500 mA until the system processor powers up and can set parameters through I^2C.
2. Program the Safety Register.
3. Set IINLIM to 11 (no limit).
4. Set OREG to the desired value (typically 4.18).
5. Reset the IO_LEVEL bit, then set IOCHARGE.
6. Set I_{INLIM} to 500 mA if a USB source is connected.

During the initial system startup, while the charger IC is being programmed, the system current is limited to 500 mA for 1 ms during steps 4 and 5. This is the value of the soft-start $I_{OCHARGE}$ current used when I_{INLIM} is set to No Limit.

If the system is powered up without a battery present, the CV bit should be set. When a battery is inserted, the CV bit is cleared.

Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 11. STAT Pin Function

EN_STAT	Charge State	STAT Pin
0	X	OPEN
X	Normal Conditions	OPEN
1	Charging	LOW
X	Fault (Charging or Boost)	128 µs Pulse, then OPEN

The FAULT bits (REG 00[2:0]) indicate the type of fault in Charge Mode. *See Table 12 for details.*

Table 12. Fault Status Bits During Charge Mode

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (No Fault)
0	0	1	VBUS OVP
0	1	0	Sleep Mode
0	1	1	Poor Input Source
1	0	0	Battery OVP
1	0	1	Thermal Shutdown
1	1	0	Timer Fault
1	1	1	No Battery

Charge Mode Control Bits

Setting either HZ_MODE or $\overline{CE}$ through I²C disables the charger and puts the IC into High-Impedance Mode. The t_{32S} timer will continue to run. If it is allowed to expire, all registers (except SAFETY) reset, which enables t_{15MIN} charging. When the t_{15MIN} expires, the IC sets the $\overline{CE}$ bit and the IC enters High-Impedance Mode. If $\overline{CE}$ was set by t_{15MIN} overflow, a new charge cycle can only be initiated through I²C or VBUS POR.

Setting the RESET bit clears all registers (except Safety).

Table 13. DISABLE Pin and $\overline{CE}$ Bit Functionality

Charging	DISABLE Pin	$\overline{CE}$	HZ_MODE
ENABLE	0	0	0
DISABLE	X	1	X
DISABLE	X	X	1
DISABLE	1	X	X

Raising the DISABLE pin does stop the t_{32S} from advancing. If the DISABLE pin is raised during t_{15MIN} charging, the t_{15MIN} timer is reset.

Operational Mode Control

OPA_MODE (REG 01[0]) and the HZ_MODE (REG 01[1]) bits in conjunction with the FAULT state define the operational mode of the charger.

Table 14. Operation Mode Control

HZ_MODE	OPA_MODE	FAULT	Operation Mode
0	0	0	Charge
0	X	1	Charge Configure
0	1	0	Boost
1	X	X	High Impedance

The IC resets the OPA_MODE bit whenever the boost is deactivated, whether due to a fault or being disabled by setting the HZ_MODE bit.

Boost Mode

Boost Mode can be enabled if the IC is in 32-Second Mode with the OTG pin and OPA_MODE bits as indicated in Table 15. The OTG pin ACTIVE state is 1 if OTG_PL=1 and 0 when OTG_PL=0.

If boost is active using the OTG pin, Boost Mode is initiated even if the HZ_MODE=1. The HZ_MODE bit overrides the OPA_MODE bit.

Table 15. Enabling Boost

OTG_EN	OTG Pin	HZ_ MODE	OPA_ MODE	BOOST
1	ACTIVE	X	X	Enabled
X	X	0	1	Enabled
X	$\overline{\text{ACTIVE}}$	X	0	Disabled
0	X	1	X	Disabled
1	$\overline{\text{ACTIVE}}$	1	1	Disabled
0	ACTIVE	0	0	Disabled

To remain in Boost Mode, the TMR_RST must be set by the host before the t_{32S} timer times out. If t_{32S} times out in Boost Mode; the IC resets all registers, pulses the STAT pin, sets the FAULT bits to 110, and resets the BOOST bit. VBUS POR or reading REG00 clears the fault condition.

Boost PWM Control

The IC uses a minimum on-time and computed minimum off-time to regulate VBUS. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During PWM Mode, the output voltage drops slightly as the input current rises. With a constant V_{BAT}, this appears as a constant output resistance.

The “droop” caused by the output resistance when a load is applied allows the regulator to respond smoothly to load transients with no undershoot from the load line. *This can be seen in Figure 32 and Figure 40.*