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FAIRCHILD SEMICONDUCTOR®

July 2012

FAN54010 / FAN54011 / FAN54012 / FAN54013 / FAN54014 USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: ±0.5% at 25°C; ±1% from 0 to 125°C
- ±5% Input Current Regulation Accuracy
- ±5% Charge Current Regulation Accuracy
- 20 V Absolute Maximum Input Voltage
- 6 V Maximum Input Operating Voltage
- 1.45 A Maximum Charge Rate
- Programmable through High-Speed I^2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Charger Voltage
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1µH External Inductor
- Safety Timer with Reset Control
- 1.8 V Regulated Output from VBUS for Auxiliary Circuits
- Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum VBUS Voltage
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5 V, 500 mA Boost Mode for USB OTG for 3.0 V to 4.5 V Battery Input

Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

All trademarks are the property of their respective owners.

Description

The FAN54010 family (FAN5401X) combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I^2C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3MHz to minimize the size of external passive components.

The FAN5401X provides battery charging in three phases: conditioning, constant current, and constant voltage.

To ensure USB compliance and minimize charging time, the input current is limited to the value set through the I^2C host. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I^2C host.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode with leakage from the battery to the input prevented. Charge status is reported back to the host through the I^2C port. Charge current is reduced when the die temperature reaches 120°C.

The FAN5401X can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The FAN5401X is available in a 1.96 x 1.87 mm, 20-bump, 0.4 mm pitch, WLCSP package.

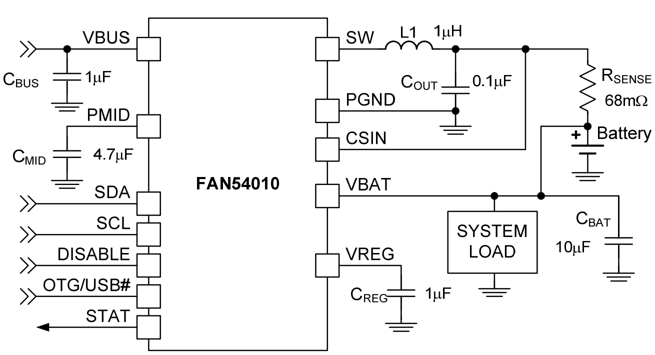


Figure 1. Typical Application

Ordering Information

Part Number	Temperature Range	Package	PN Bits: IC_INFO[4:2]	Packing Method
FAN54010UCX[(1)]	-40 to 85°C	20-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch, Estimated Size: 1.96 x 1.87 mm	011	Tape and Reel
FAN54011UCX[(1)]	-40 to 85°C		001	Tape and Reel
FAN54012UCX[(1)]	-40 to 85°C		011	Tape and Reel
FAN54013UCX	-40 to 85°C		101	Tape and Reel
FAN54014UCX[(1)]	-40 to 85°C		111	Tape and Reel

Note:
1. Preliminary release only; please contact a Fairchild representative for information about part availability.

Table 1. Feature Comparison Summary

Part Number	PN Bits: REG3[4:2]	Slave Address	Automatic Charge	Special Charger[(2)]	Safety Limits	Battery Absent Behavior	E2 Pin	VREG (E3 Pin)
FAN54010UCX	011	1101011	Yes	No	No	OFF	AUXPWR (Connect to VBAT)	PMID
FAN54011UCX	001	1101011	No	No	No	OFF		
FAN54012UCX	011	1101011	Yes	No	No	ON		
FAN54013UCX	101	1101011	Yes	Yes	Yes	OFF	DISABLE	1.8V
FAN54014UCX	111	1101011	No	Yes	Yes	OFF		

Note:
2. A "special charger" is a current-limited charger that is not a USB compliant source.

Table 2. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Unit
L1	1 µH ±20%, 1.6 A DCR=55 mΩ, 2520	Murata: LQM2HPN1R0	L	1.0	µH
	1 µH ±30%, 1.4A DCR=85 mΩ, 2016	Murata: LQM2MPN1R0			
C_{BAT}	10 µF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M TDK: C1608X5R0J106M	C	10	µF
C_{MID}	4.7 µF, 10%, 6.3 V, X5R, 0603	Murata: GRM188R60J475K TDK: C1608X5R0J475K	C[(3)]	4.7	µF
C_{BUS}	1.0 µF, 10%, 25 V, X5R, 0603	Murata GRM188R61E105K TDK:C1608X5R1E105M	C	1.0	µF

Note:
3. A 6.3 V rating is sufficient for C_{MID} since PMID is protected from over-voltage surges on VBUS by Q3 (Figure 3).

Block Diagram

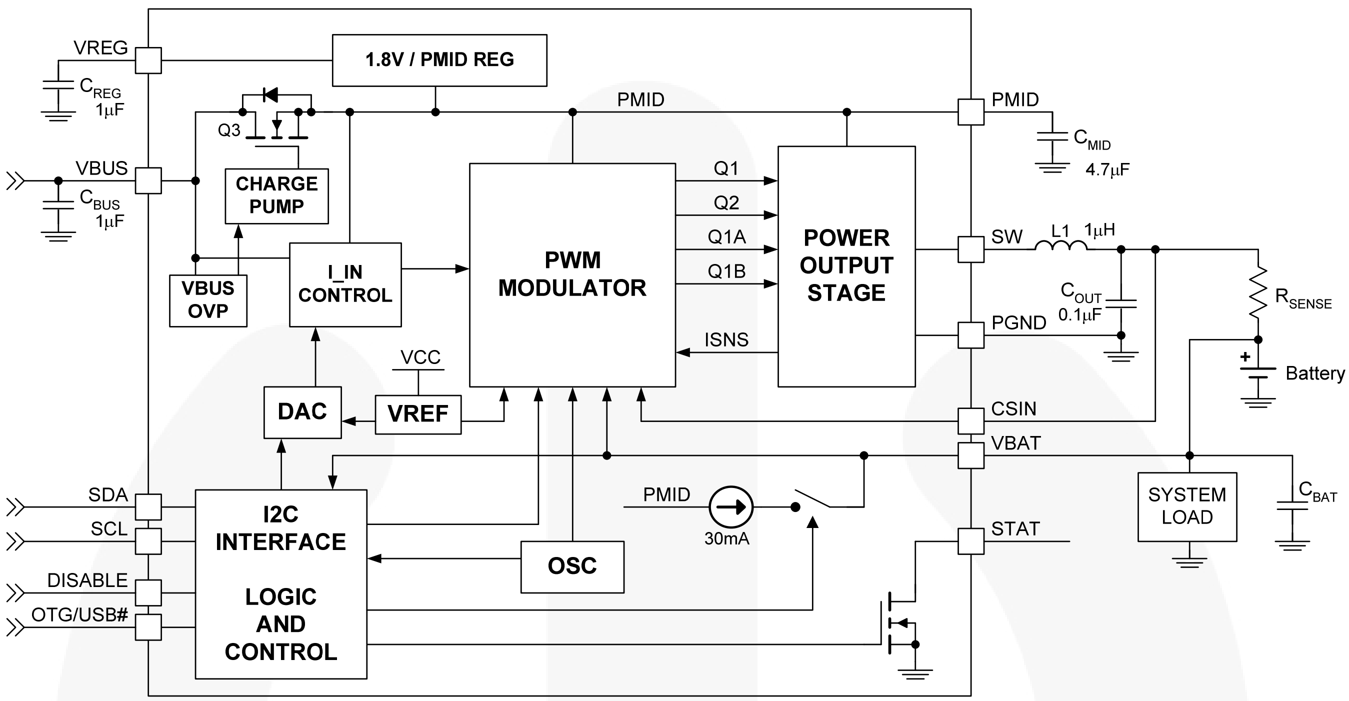
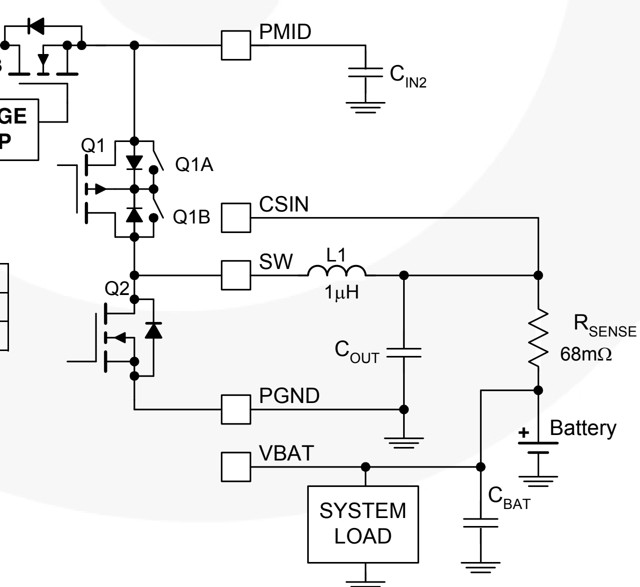


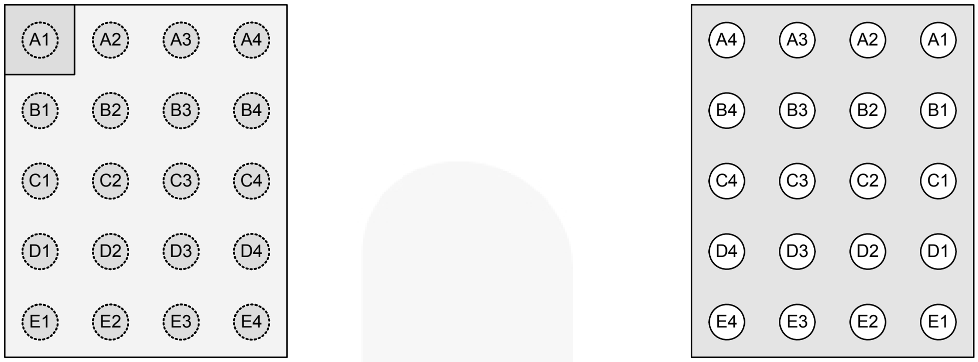
Figure 2. IC and System Block Diagram



PMID	Q1A	Q1B
Greater than V_{BAT}	ON	OFF
Less than V_{BAT}	OFF	ON

Figure 3. Power Stage

Pin Configuration



Top View **Bottom View**

Figure 4. WLCSP-20 Pin Assignments

Pin Definitions

Pin #	Name	Part #	Description
A1, A2	VBUS	ALL	**Charger Input Voltage** and USB-OTG output voltage. Bypass with a 1 μF capacitor to PGND.
A3	NC	ALL	**No Connect**. No external connection is made between this pin and the IC's internal circuitry.
A4	SCL	ALL	**I^2C Interface Serial Clock**. This pin should not be left floating.
B1-B3	PMID	ALL	**Power Input Voltage**. Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 μF, 6.3 V capacitor to PGND.
B4	SDA	ALL	**I^2C Interface Serial Data**. This pin should not be left floating.
C1-C3	SW	ALL	**Switching Node**. Connect to output inductor.
C4	STAT	ALL	**Status**. Open-drain output indicating charge status. The IC pulls this pin LOW when charging.
D1-D3	PGND	ALL	**Power Ground**. Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{MID} should be as short as possible.
D4	OTG	ALL	**On-The-Go**. Enables boost regulator in conjunction with OTG_EN and OTG_PL bits *(see Table 16)*. On VBUS Power-On Reset (POR), this pin sets the input current limit for t_{15MIN} charging.
E1	CSIN	ALL	**Current-Sense Input**. Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1μF capacitor to PGND.
E2	AUXPWR	10, 11, 12	**Auxiliary Power**. Connect to the battery pack to provide IC power during High-Impedance Mode. Bypass with a 1 μF capacitor to PGND.
E2	DISABLE	13, 14,	**Charge Disable**. If this pin is HIGH, charging is disabled. When LOW, charging is controlled by the I^2C registers. When this pin is HIGH, the 15-minute timer is reset. This pin does not affect the 32-second timer.
E3	VREG	ALL	**Regulator Output**. Connect to a 1 μF capacitor to PGND. This pin can supply up to 2 mA of DC load current. For FAN54010-FAN54012, the output voltage is PMID, which is limited to 6.5 V. For FAN54013-FAN54014, the output voltage is regulated to 1.8 V.
E4	VBAT	ALL	**Battery Voltage**. Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1 μF capacitor to PGND if the battery is connected through long leads.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	VBUS Voltage	Continuous	–1.4	20.0	V
		Pulsed, 100 ms Maximum Non-Repetitive	–2.0		
V_{STAT}	STAT Voltage		–0.3	16.0	V
V_I	PMID Voltage			7.0	V
	SW, CSIN, VBAT, AUXPWR, DISABLE Voltage		–0.3	7.0	
V_O	Voltage on Other Pins		–0.3	6.5[4]	V
$\frac{dV_{BUS}}{dt}$	Maximum V_{BUS} Slope above 5.5 V when Boost or Charger are Active			4	V/µs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2000		V
		Charged Device Model per JESD22-C101	500		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
4. Lesser of 6.5 V or V_I + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	Supply Voltage		4	6	V
$V_{BAT(MAX)}$	Maximum Battery Voltage when Boost enabled			4.5	V
$-\frac{dV_{BUS}}{dt}$	Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \leq 4.7$ µF *(see VBUS Short While Charging)*	$T_A \leq 60°C$		4	V/µs
		$T_A \geq 60°C$		2	
T_A	Ambient Temperature		–30	+85	°C
T_J	Junction Temperature *(see Thermal Regulation and Protection section)*		–30	+120	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A. *For measured data, see Table 11.*

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	60	°C/W
θ_{JB}	Junction-to-PCB Thermal Resistance	20	°C/W

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for T_J=25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Power Supplies							
I_{VBUS}	VBUS Current	V_{BUS} > $V_{BUS(min)}$, PWM Switching			10		mA
		V_{BUS} > $V_{BUS(min)}$; PWM Enabled, Not Switching (Battery OVP Condition); I_IN Setting=100mA			2.5		mA
		0°C < T_J < 85°C, HZ_MODE=1 V_{BAT} < V_{LOWV}, 32S Mode			63	90	µA
I_{LKG}	VBAT to VBUS Leakage Current	0°C < T_J < 85°C, HZ_MODE=1, V_{BAT}=4.2 V, V_{BUS}=0 V			0.2	5.0	µA
I_{BAT}	Battery Discharge Current in High-Impedance Mode	0°C < T_J < 85°C, HZ_MODE=1, V_{BAT}=4.2 V				20	µA
		FAN54013-14, DISABLE=1, 0°C < T_J < 85°C, V_{BAT}=4.2 V				10	
Charger Voltage Regulation							
V_{OREG}	Charge Voltage Range			3.5		4.4	V
	Charge Voltage Accuracy	T_A=25°C		–0.5%		+0.5%	
		T_J=0 to 125°C		–1%		+1%	
Charging Current Regulation							
I_{OCHRG}	Output Charge Current Range	V_{LOWV} < V_{BAT} < V_{OREG} R_{SENSE}=68mΩ		550		1450	mA
	Charge Current Accuracy Across R_{SENSE}	20 mV ≤ V_{IREG} ≤ 40 mV	FAN54010-12	95	100	105	%
			FAN54013-14	92	97	102	
		V_{IREG} > 40 mV	FAN54010-12	97	100	103	
			FAN54013-14	94	97	100	
Weak Battery Detection							
V_{LOWV}	Weak Battery Threshold Range			3.4		3.7	V
	Weak Battery Threshold Accuracy			–5		+5	%
	Weak Battery Deglitch Time	Rising Voltage			30		ms
Logic Levels: DISABLE, SDA, SCL, OTG							
V_{IH}	High-Level Input Voltage			1.05			V
V_{IL}	Low-Level Input Voltage					0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{IN}			0.01	1.00	µA
Charge Termination Detection							
$I_{(TERM)}$	Termination Current Range	V_{BAT} > V_{OREG} – V_{RCH}, R_{SENSE}=68 mΩ		50		400	mA
	Termination Current Accuracy	[V_{CSIN} – V_{BAT}] from 3 mV to 20 mV		–25		+25	%
		[V_{CSIN} – V_{BAT}] from 20 mV to 40 mV		–5		+5	
	Termination Current Deglitch Time	2 mV Overdrive			30		ms
1.8V Linear Regulator							
V_{REG}	1.8 V Regulator Output	I_{REG} from 0 to 2 mA, FAN54013-14		1.7	1.8	1.9	V

Continued on the following page…

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for T_J=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Power Source Detection						
$V_{IN(MIN)1}$	VBUS Input Voltage Rising	To Initiate and Pass VBUS Validation		4.29	4.42	V
$V_{IN(MIN)2}$	Minimum VBUS During Charge	During Charging		3.71	3.94	V
t_{VBUS_VALID}	VBUS Validation Time			30		ms
Special Charger (V_{BUS}) (FAN54013, FAN54014)						
V_{SP}	Special Charger Setpoint Accuracy		–3		+3	%
Input Current Limit						
I_{INLIM}	Input Current Limit Threshold	I_{IN} Set to 100 mA	88	93	98	mA
		I_{IN} Set to 500 mA	450	475	500	
V_{REF} Bias Generator						
V_{REF}	Bias Regulator Voltage	V_{BUS} > $V_{IN(MIN)}$ or V_{BAT} > $V_{BAT(MIN)}$			6.5	V
	Short-Circuit Current Limit			20		mA
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below $V_{(OREG)}$	100	120	150	mV
	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		130		ms
STAT Output						
$V_{STAT(OL)}$	STAT Output Low	I_{STAT}=10 mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT}=5 V			1	µA
Battery Detection						
I_{DETECT}	Battery Detection Current before Charge Done (Sink Current)[5]	Begins after Termination Detected and $V_{BAT} \leq V_{OREG} - V_{RCH}$		–0.80		mA
t_{DETECT}	Battery Detection Time			262		ms
Sleep Comparator						
V_{SLP}	Sleep-Mode Entry Threshold, $V_{BUS} - V_{BAT}$	2.3 V $\leq V_{BAT} \leq V_{OREG}$, V_{BUS} Falling	0	0.04	0.10	V
t_{SLP_EXIT}	Deglitch Time for VBUS Rising Above V_{BAT} by V_{SLP}	Rising Voltage		30		ms
Power Switches *(see Figure 3)*						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID)	$I_{IN(LIMIT)}$=500 mA		180	250	mΩ
	Q1 On Resistance (PMID to SW)			130	225	
	Q2 On Resistance (SW to GND)			150	225	
Charger PWM Modulator						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			0		%
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold[6]	Low-Side MOSFET (Q2) Cycle-by-Cycle Current Limit		140		mA

Continued on the following page…

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8 V; and typical values are for T_J=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Boost Mode Operation (OPA_MODE=1, HZ_MODE=0)						
V_{BOOST}	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 200 mA	4.80	5.07	5.17	V
		3.0 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 500 mA	4.77	5.07	5.17	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT}=3.6 V, I_{OUT}=0		140	300	µA
$I_{LIMPK(BST)}$	Q2 Peak Current Limit		1272	1590	1908	mA
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.42		V
		To Start Boost Regulator		2.58	2.70	
VBUS Load Resistance						
R_{VBUS}	VBUS to PGND Resistance	Normal Operation		1500		KΩ
		Charger Validation		100		Ω
Protection and Timers						
$VBUS_{OVP}$	VBUS Over-Voltage Shutdown	V_{BUS} Rising	6.09	6.29	6.49	V
	Hysteresis	V_{BUS} Falling		100		mV
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle Peak Current Limit	Charge Mode		2.3		A
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	1.95	2.00	2.05	V
	Hysteresis	V_{BAT} Falling		100		mV
I_{SHORT}	Linear Charging Current	V_{BAT} < V_{SHORT}	20	30	40	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold(7)	T_J Rising		145		°C
	Hysteresis(7)	T_J Falling		10		
T_{CF}	Thermal Regulation Threshold(7)	Charge Current Reduction Begins		120		°C
t_{INT}	Detection Interval			2.1		s
t_{32S}	32-Second Timer(8)	Charger Enabled	20.5	25.2	28.0	s
		Charger Disabled	18.0	25.2	34.0	
t_{15MIN}	15-Minute Timer	15-Minute Mode (FAN54013-14)	12.0	13.5	15.0	min
Δt_{LF}	Low-Frequency Timer Accuracy	Charger Inactive	–25		25	%

Notes:

5. Negative current is current flowing from the battery to VBUS (discharging the battery).
6. Q2 always turns on for 60 ns, then turns off if current is below I_{SYNC}.
7. Guaranteed by design; not tested in production.
8. This tolerance (%) applies to all timers on the IC, including soft-start and deglitching timers.

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, $C_B \le 100$ pF			3400	
		High-Speed Mode, $C_B \le 400$ pF			1700	
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		High-Speed Mode, $C_B \le 100$ pF		160		ns
		High-Speed Mode, $C_B \le 400$ pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \le 100$ pF		60		ns
		High-Speed Mode, $C_B \le 400$ pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \le 100$ pF	0		70	ns
		High-Speed Mode, $C_B \le 400$ pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100$ pF		10	80	
		High-Speed Mode, $C_B \le 400$ pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100$ pF		10	40	
		High-Speed Mode, $C_B \le 400$ pF		20	80	
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100$ pF		10	80	
		High-Speed Mode, $C_B \le 400$ pF		20	160	

Continued on the following page…

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \leq 100$ pF		10	80	ns
		High-Speed Mode, $C_B \leq 400$ pF		20	160	ns
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA, SCL				400	pF

Timing Diagrams

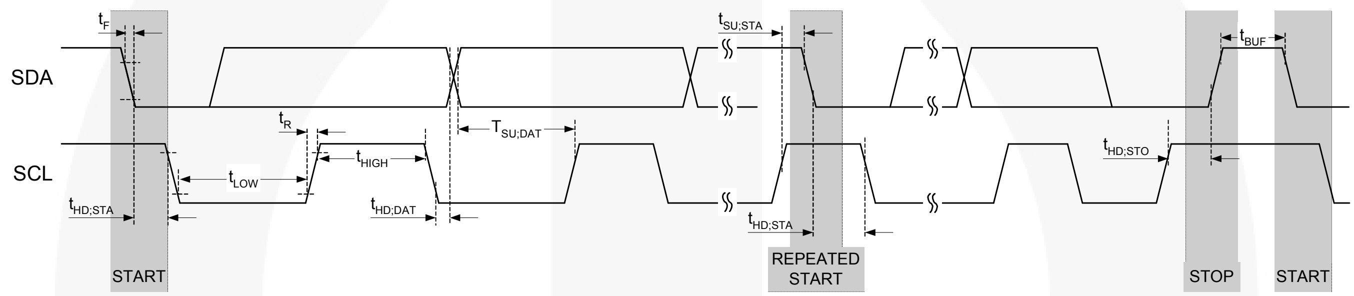
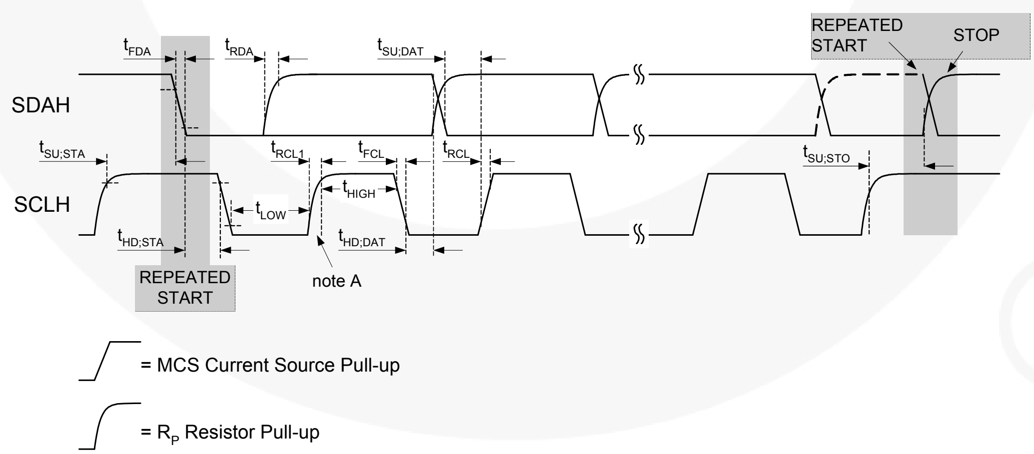


Figure 5. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 6. I²C Interface Timing for High-Speed Mode

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

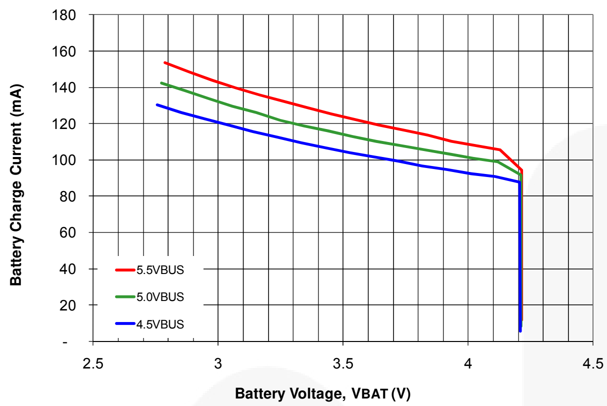


Figure 7. Battery Charge Current vs. V_{BUS} with I_{INLIM}=100 mA

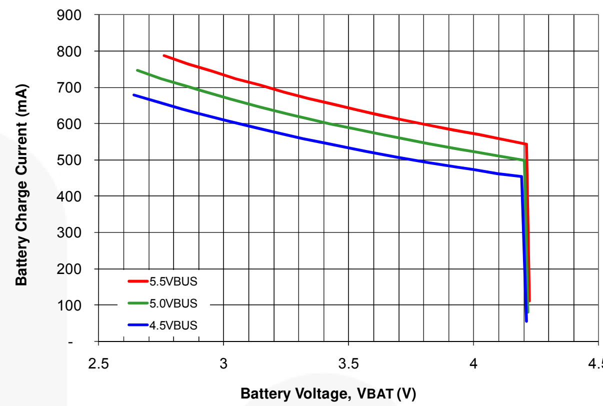


Figure 8. Battery Charge Current vs. V_{BUS} with I_{INLIM}=500 mA

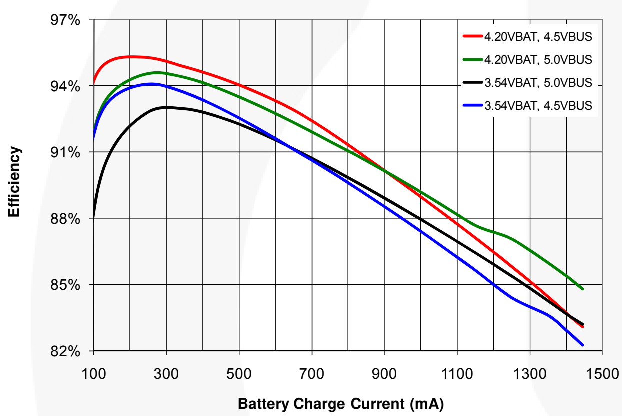


Figure 9. Charger Efficiency, No I_{INLIM}, $I_{OCHARGE}$=1,450 mA

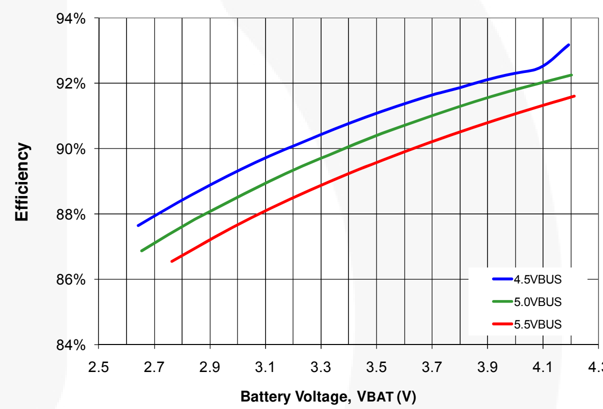


Figure 10. Charger Efficiency vs. V_{BUS}, I_{INLIM}=500 mA

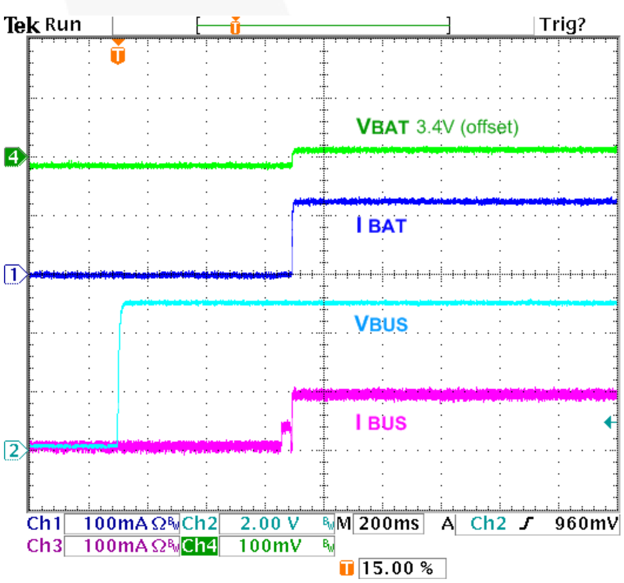


Figure 11. Auto-Charge Startup at V_{BUS} Plug-in, I_{INLIM}=100 mA, OTG=1, V_{BAT}=3.4 V

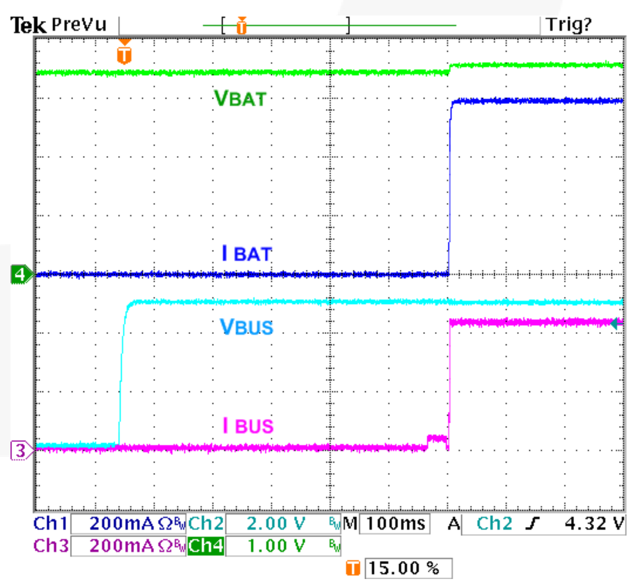


Figure 12. Auto-Charge Startup at V_{BUS} Plug-in, I_{INLIM}=500 mA, OTG=1, V_{BAT}=3.4 V

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

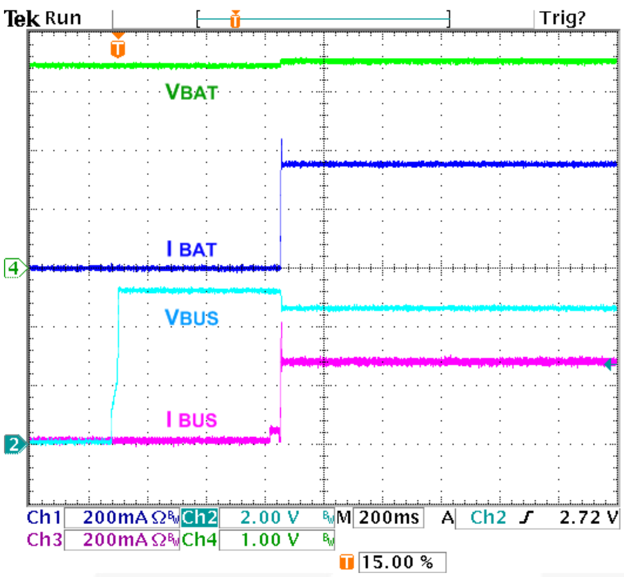


Figure 13. AutoCharge Startup with 300 mA Limited Charger / Adaptor, I_{INLIM}=500 mA, OTG=1, V_{BAT}=3.4 V

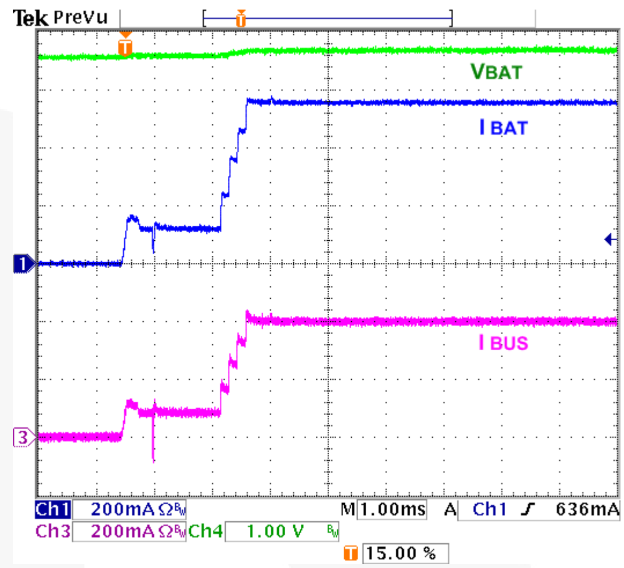


Figure 14. Charger Startup with HZ_MODE Bit Reset, I_{INLIM}=500 mA, $I_{OCHARGE}$=1,050 mA, OREG=4.2 V, V_{BAT}=3.6 V

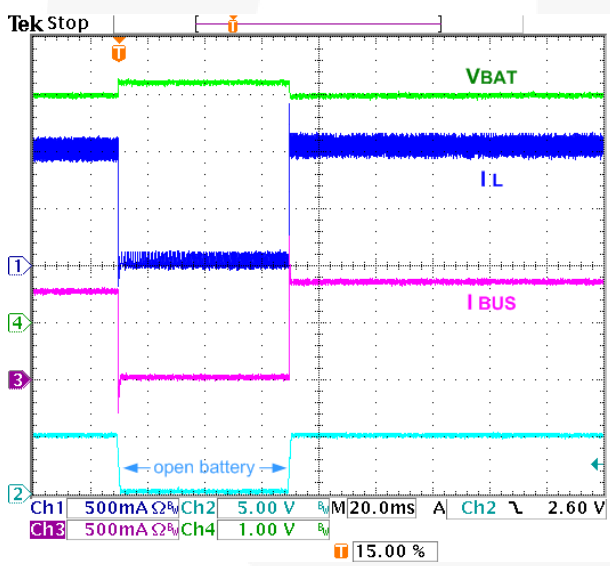


Figure 15. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=1,050 mA, No I_{INLIM}, TE=0

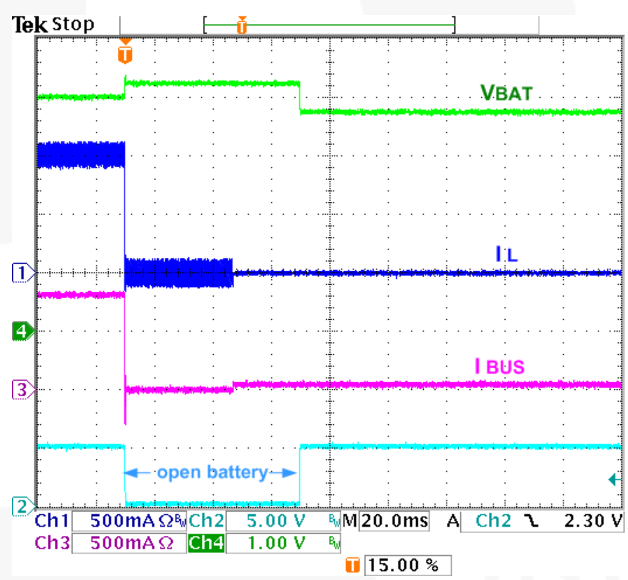


Figure 16. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=1,050 mA, No I_{INLIM}, TE=1

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

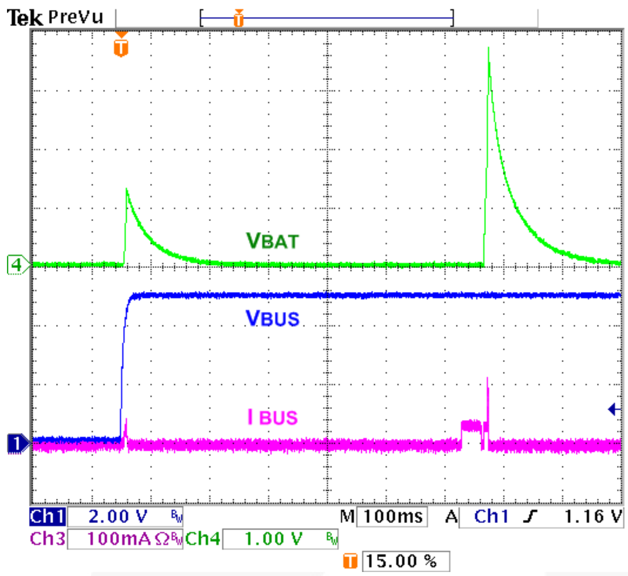


Figure 17. No Battery at V_{BUS} Power-up; FAN54010, FAN54013

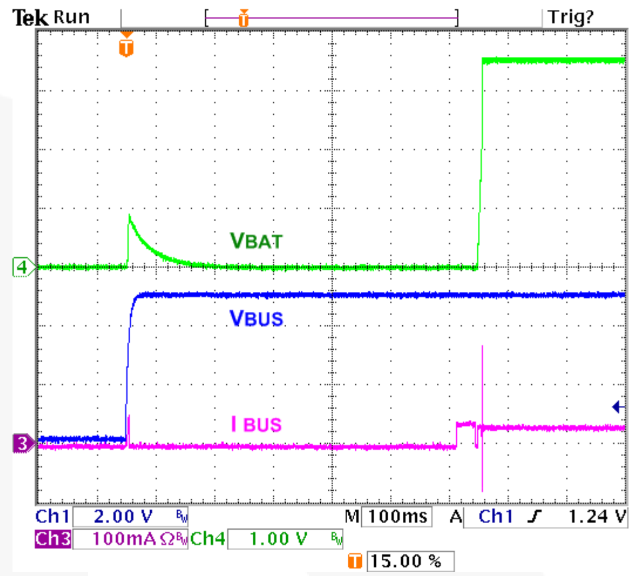


Figure 18. No Battery at V_{BUS} Power-up; FAN54012

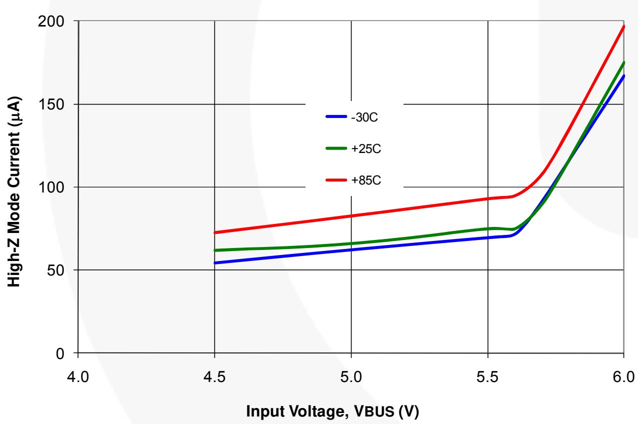


Figure 19. VBUS Current in High-Impedance Mode with Battery Open

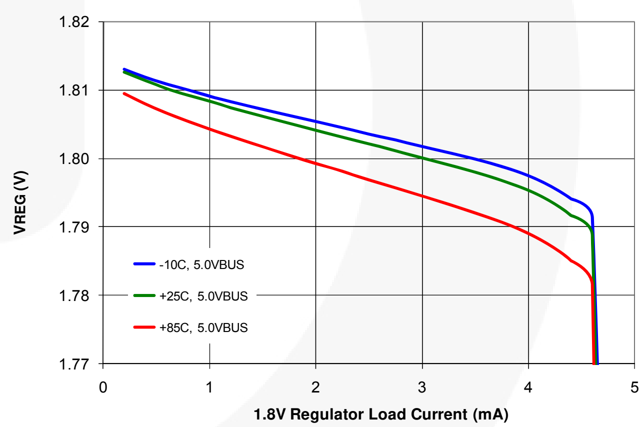


Figure 20. V_{REG} 1.8 V Output Regulation

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

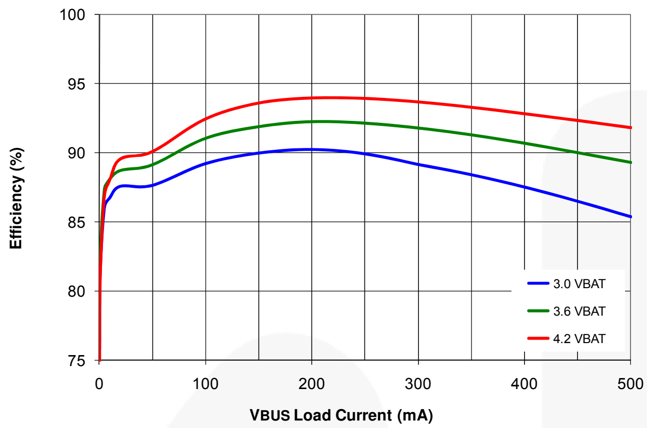


Figure 21. Efficiency vs. V_{BAT}

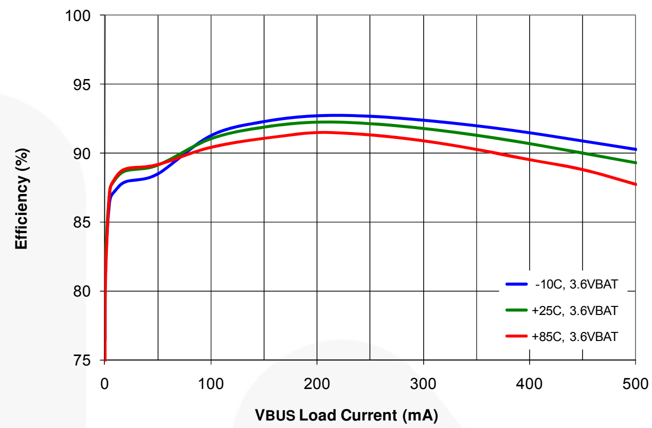


Figure 22. Efficiency Over Temperature

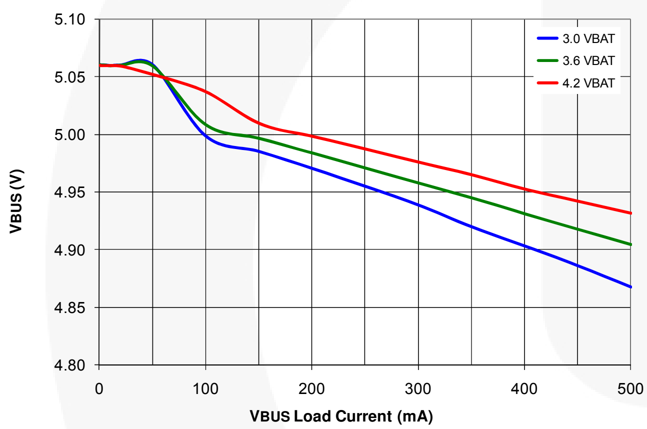


Figure 23. Output Regulation vs. V_{BAT}

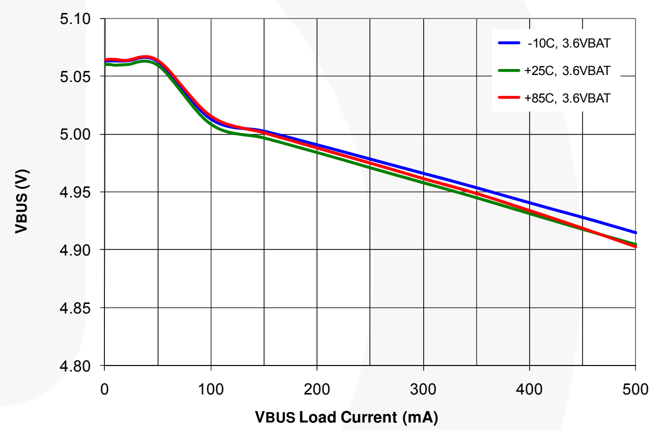


Figure 24. Output Regulation Over Temperature

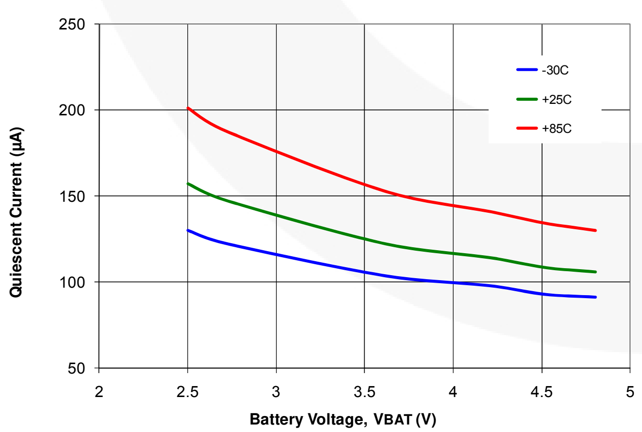


Figure 25. Quiescent Current

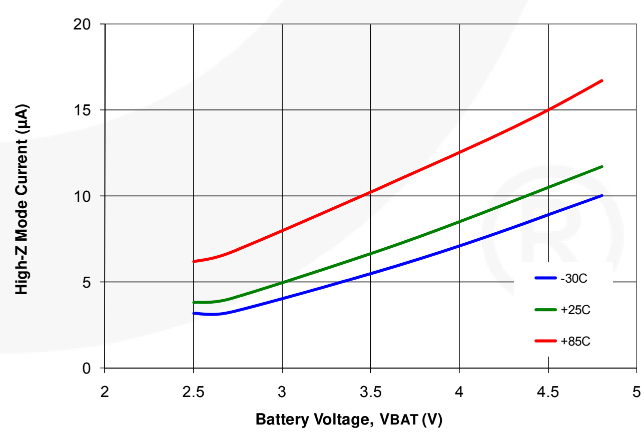


Figure 26. High-Impedance Mode Battery Current

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

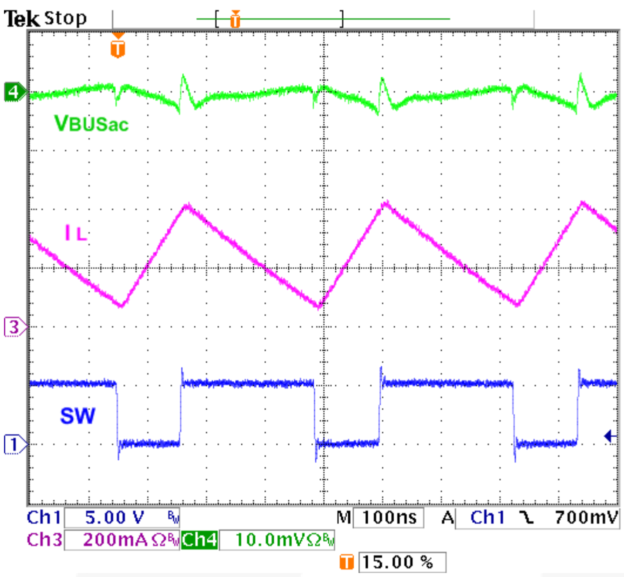


Figure 27. Boost PWM Waveform

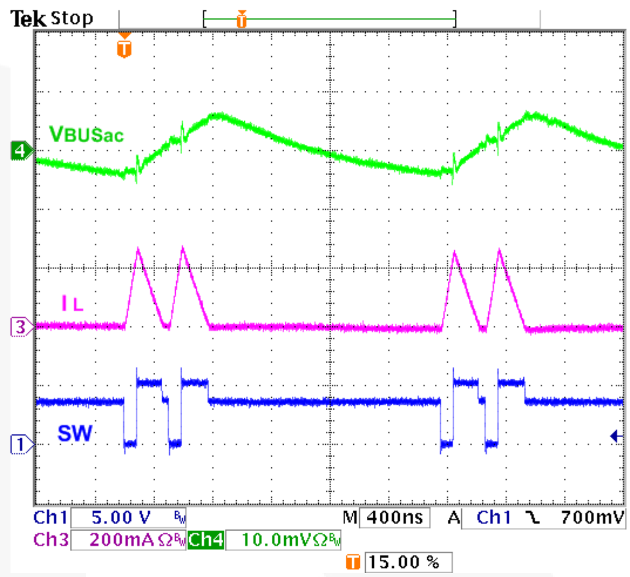


Figure 28. Boost PFM Waveform

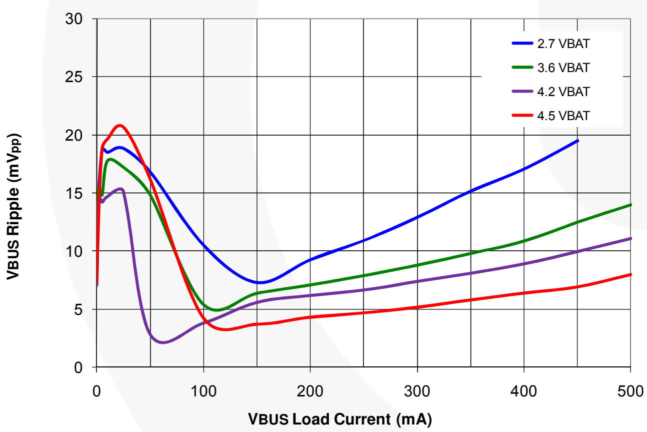


Figure 29. Output Ripple vs. V_{BAT}

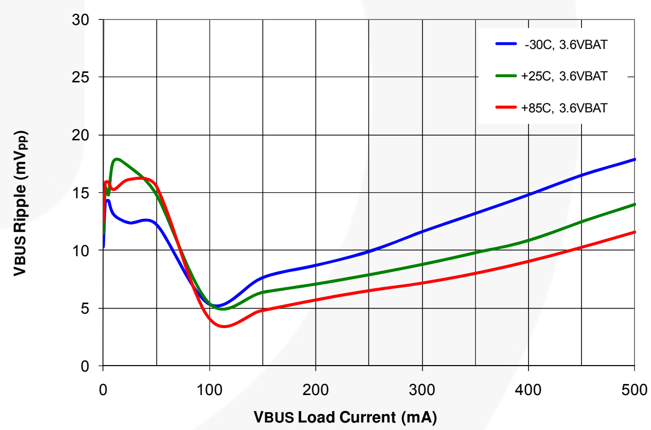


Figure 30. Output Ripple vs. Temperature

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

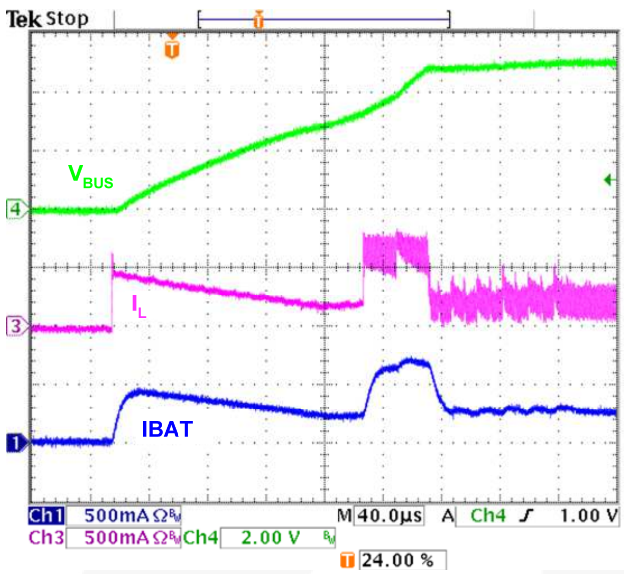


Figure 31. Startup, 3.6 V_{BAT}, 44 Ω Load, Additional 10 µF, X5R Across V_{BUS}

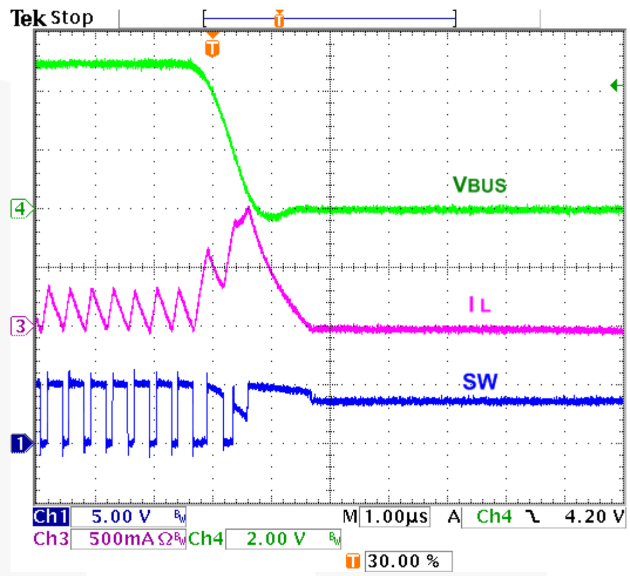


Figure 32. V_{BUS} Fault Response, 3.6 V_{BAT}

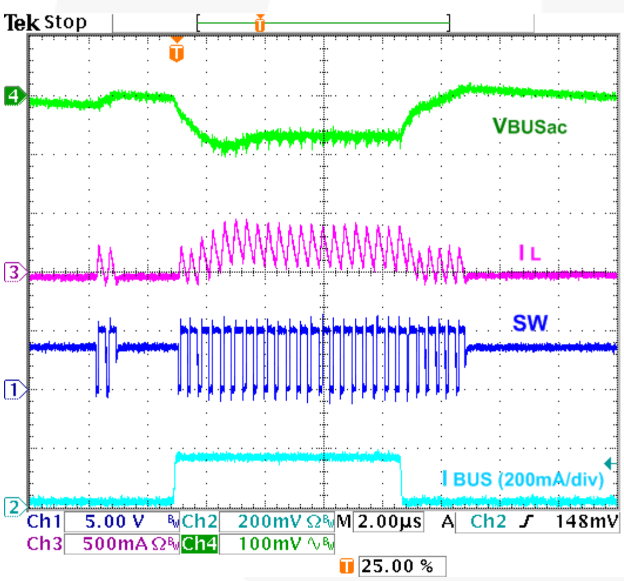


Figure 33. Load Transient, 5-155-5 mA, t_R=t_F=100 ns

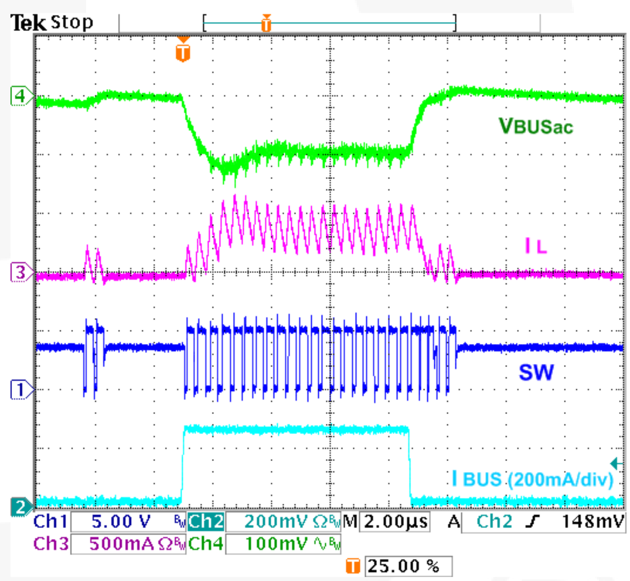


Figure 34. Load Transient, 5-255-5 mA, t_R=t_F=100 ns

Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

FAN5401X combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN5401X has three operating modes:

1. Charge Mode:
   Charges a single-cell Li-ion or Li-polymer battery.
2. Boost Mode:
   Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
3. High-Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.

Note: Default settings are denoted by **bold typeface**.

Charge Mode

In Charge Mode, FAN5401X employs four regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
4. Temperature: If the IC's junction temperature reaches 120°C, charge current is reduced until the IC's temperature stabilizes at 120°C.
5. An additional loop limits the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The FAN5401X is designed to work with a current-limited input source at VBUS. During the current regulation phase of charging, I_{INLIM} or the programmed charging current limits the amount of current available to charge the battery and power the system. The effect of I_{INLIM} on I_{CHARGE} can be seen in Figure 36.

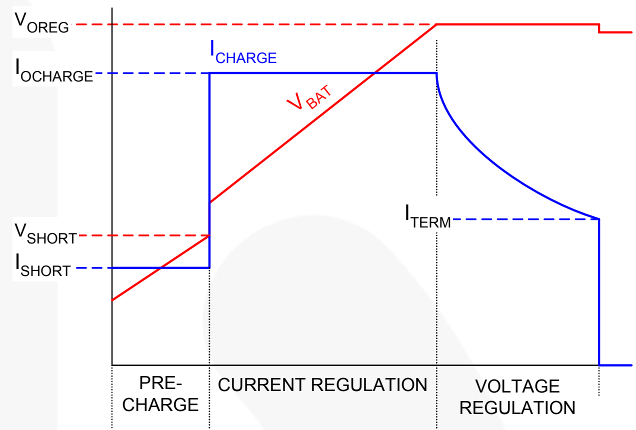


Figure 35. Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

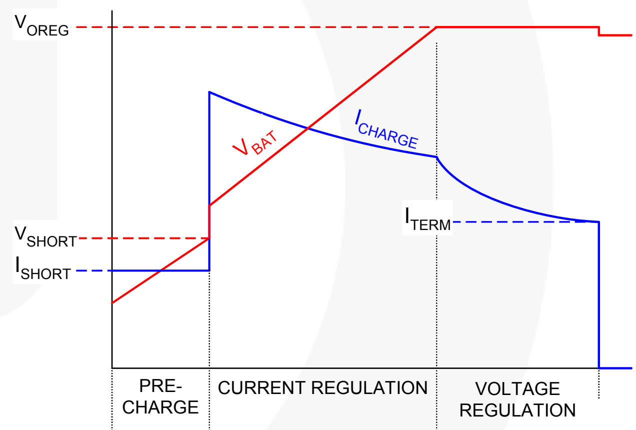


Figure 36. Charge Curve, I_{INLIM} Limits I_{CHARGE}

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG1[3]).

The charger output or "float" voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments, as shown in Table 3.

Table 3. OREG Bits (OREG[7:2]) vs. Charger V_{OUT} (V_{OREG}) Float Voltage

Decimal	Hex	VOREG	Decimal	Hex	VOREG
0	00	3.50	32	20	4.14
1	01	3.52	33	21	4.16
2	**02**	**3.54**	34	22	4.18
3	03	3.56	35	23	4.20
4	04	3.58	36	24	4.22
5	05	3.60	37	25	4.24
6	06	3.62	38	26	4.26
7	07	3.64	39	27	4.28
8	08	3.66	40	28	4.30
9	09	3.68	41	29	4.32
10	0A	3.70	42	2A	4.34
11	0B	3.72	43	2B	4.36
12	0C	3.74	44	2C	4.38
13	0D	3.76	45	2D	4.40
14	0E	3.78	46	2E	4.42
15	0F	3.80	47	2F	4.44
16	10	3.82	48	30	4.44
17	11	3.84	49	31	4.44
18	12	3.86	50	32	4.44
19	13	3.88	51	33	4.44
20	14	3.90	52	34	4.44
21	15	3.92	53	35	4.44
22	16	3.94	54	36	4.44
23	17	3.96	55	37	4.44
24	18	3.98	56	38	4.44
25	19	4.00	57	39	4.44
26	1A	4.02	58	3A	4.44
27	1B	4.04	59	3B	4.44
28	1C	4.06	60	3C	4.44
29	1D	4.08	61	3D	4.44
30	1E	4.10	62	3E	4.44

The following charging parameters can be programmed by the host through I^2C:

Table 4. Programmable Charging Parameters

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG2[7:2]
Battery Charging Current Limit	I_{OCHRG}	REG4[6:4]
Input Current Limit	I_{INLIM}	REG1[7:6]
Charge Termination Limit	I_{TERM}	REG4[2:0]
Weak Battery Voltage	V_{LOWV}	REG1[5:4]

A new charge cycle begins when one of the following occurs:

- The battery voltage falls below V_{OREG} - V_{RCH}
- VBUS Power on Reset (POR) clears and the battery voltage is below the weak battery threshold (V_{LOWV}). **This occurs for all versions except the FAN54011.**
- $\overline{CE}$ or HZ_MODE is reset through I^2C write to CONTROL1 (R1) register.

Charge Current Limit ($I_{OCHARGE}$)

Table 5. $I_{OCHARGE}$ (REG4 [6:4]) Current as Function of $I_{OCHARGE}$ Bits and R_{SENSE} Resistor Values

DEC	BIN	HEX	V_{RSENSE} (mV)	$I_{OCHARGE}$ (mA)	
				68mΩ	100mΩ
0	**000**	**00**	**37.4**	**550**	**374**
1	001	01	44.2	650	442
2	010	02	51.0	750	510
3	011	03	57.8	850	578
4	100	04	71.4	1050	714
5	101	05	78.2	1150	782
6	110	06	91.8	1350	918
7	111	07	98.6	1450	986

Termination Current Limit

Current charge termination is enabled when TE (REG1[3])=1. Typical termination current values are given in Table 6.

Table 6. I_{TERM} Current as Function of I_{TERM} Bits (REG4[2:0]) and R_{SENSE} Resistor Values

	FAN54010-FAN54012			FAN54013-FAN54014		
I_{TERM}	V_{RSENSE} (mV)	I_{TERM} (mA)		V_{RSENSE} (mV)	I_{TERM} (mA)	
		68 mΩ	100 mΩ		68 mΩ	100 mΩ
0	3.4	50	34	3.3	49	33
1	**6.8**	**100**	**68**	**6.6**	**97**	**66**
2	10.2	150	102	9.9	146	99
3	13.6	200	136	13.2	194	132
4	17.0	250	170	16.5	243	165
5	20.4	300	204	19.8	291	198
6	23.8	350	238	23.1	340	231
7	27.2	400	272	26.4	388	264

When the charge current falls below I_{TERM}, PWM charging stops and the STAT bits change to READY (00) for about 500 ms while the IC determines whether the battery and charging source are still connected. STAT then changes to CHARGE DONE (10), provided the battery and charger are still connected.

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a negative current limit that turns off Q2 at 140 mA to prevent current flow from the battery.

Safety Timer

Section references Figure 41 and Figure 42.

At the beginning of charging, the IC starts a 15-minute timer (t_{15MIN}). When this timer times out, charging is terminated. Writing to any register through I^2C stops and resets the t_{15MIN} timer, which in turn starts a 32-second timer (t_{32S}). Setting the TMR_RST bit (REG0[7]) resets the t_{32S} timer. If the t_{32S} timer times out, charging is terminated, the registers are set to their default values, and charging resumes using the default values with the t_{15MIN} timer running.

Normal charging is controlled by the host with the t_{32S} timer running to ensure that the host is alive. Charging with the t_{15MIN} timer running is used for charging that is unattended by the host. If the t_{15MIN} timer expires, the IC turns off the charger, sets the $\overline{CE}$ bit, and indicates a timer fault (110) on the FAULT bits (REG0[2:0]). This sequence prevents overcharge if the host fails to reset the t_{32S} timer.

V_{BUS} POR / Non-Compliant Charger Rejection

When the IC detects that V_{BUS} has risen above $V_{IN(MIN)1}$ (4.4 V), the IC applies a 100Ω load from VBUS to GND. To clear the VBUS POR (Power-On-Reset) and begin charging, VBUS must remain above $V_{IN(MIN)1}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (30 ms) before the IC initiates charging. The VBUS validation sequence always occurs before charging is initiated or re-initiated (for example, after a VBUS OVP fault or a V_{RCH} recharge initiation).

t_{VBUS_VALID} ensures that unfiltered 50/60 Hz chargers and other non-compliant chargers are rejected.

USB-Friendly Boot Sequence

For FAN54010/12/13, NOT FAN54011/14

At VBUS POR, when the battery voltage is above the weak battery threshold (V_{LOWV}), the IC operates in accordance with its I^2C register settings. If $V_{BAT} < V_{LOWV}$, the IC sets all registers to their default values and enables the charger using an input current limit controlled by the OTG pin (100 mA if OTG is LOW and 500 mA if OTG is HIGH). This feature can revive a battery whose voltage is too low to ensure reliable host operation. Charging continues in the absence of host communication even after the battery has reached V_{OREG}, whose default value is 3.54 V, and the charger remains active until t_{15MIN} times out. Once the host processor begins writing to the IC, charging parameters are set by the host, which must continually reset the t_{32S} timer to continue charging using the programmed charging parameters. If t_{32S}.times out, the register defaults are loaded, the FAULT bits are set to 110, STAT is pulsed HIGH, and charging continues with default charge parameters.

The FAN54011 and FAN54014 do not automatically initiate charging at VBUS POR. Instead, they wait for the host to initiate charging through I^2C commands.

Input Current Limiting

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the I_{INLIM} bits (REG1[7:6]).

Table 7. Input Current Limit

I_{INLIM} REG1[7:6]	Input Current Limit
00	**100 mA**
01	500 mA
10	800 mA
11	No limit

For all versions except the FAN54011/14, the OTG pin establishes the input current limit when t_{15MIN} is running. For the FAN54011 and FAN54014, no charging occurs automatically at VBUS POR; the input current limit is established by the I_{INLIM} bits.

Flow Charts

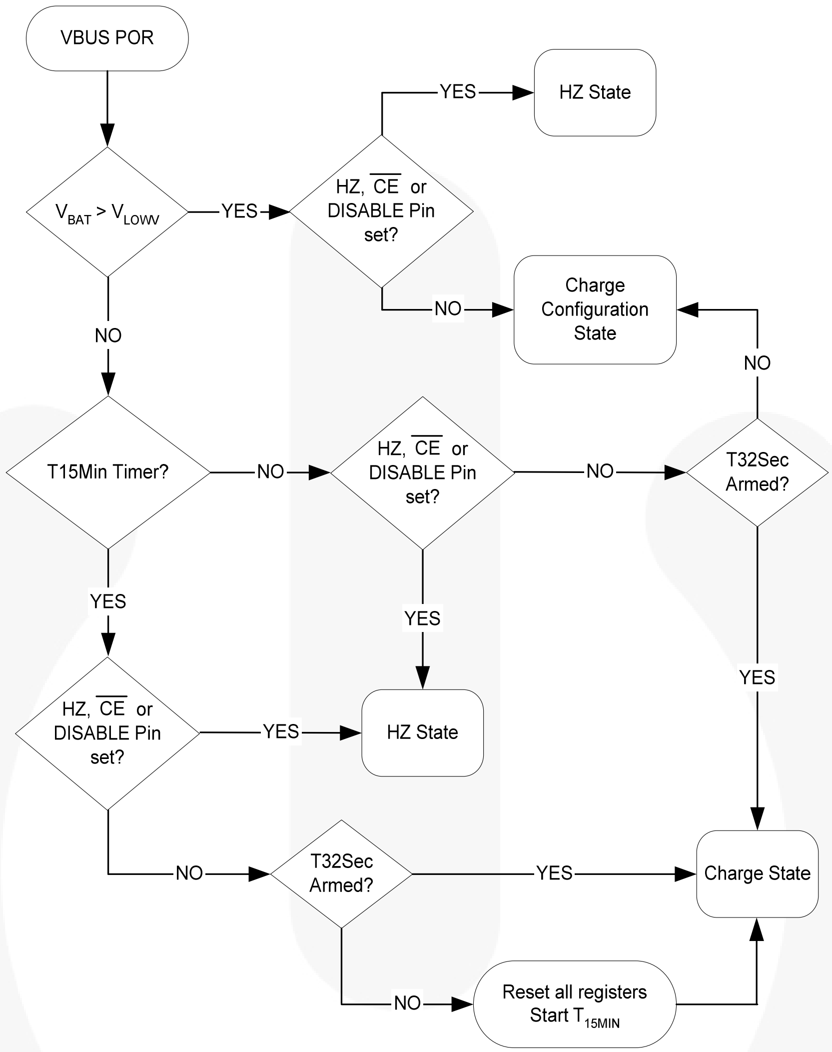


Figure 37. Charger VBUS POR

Flow Charts (Continued)

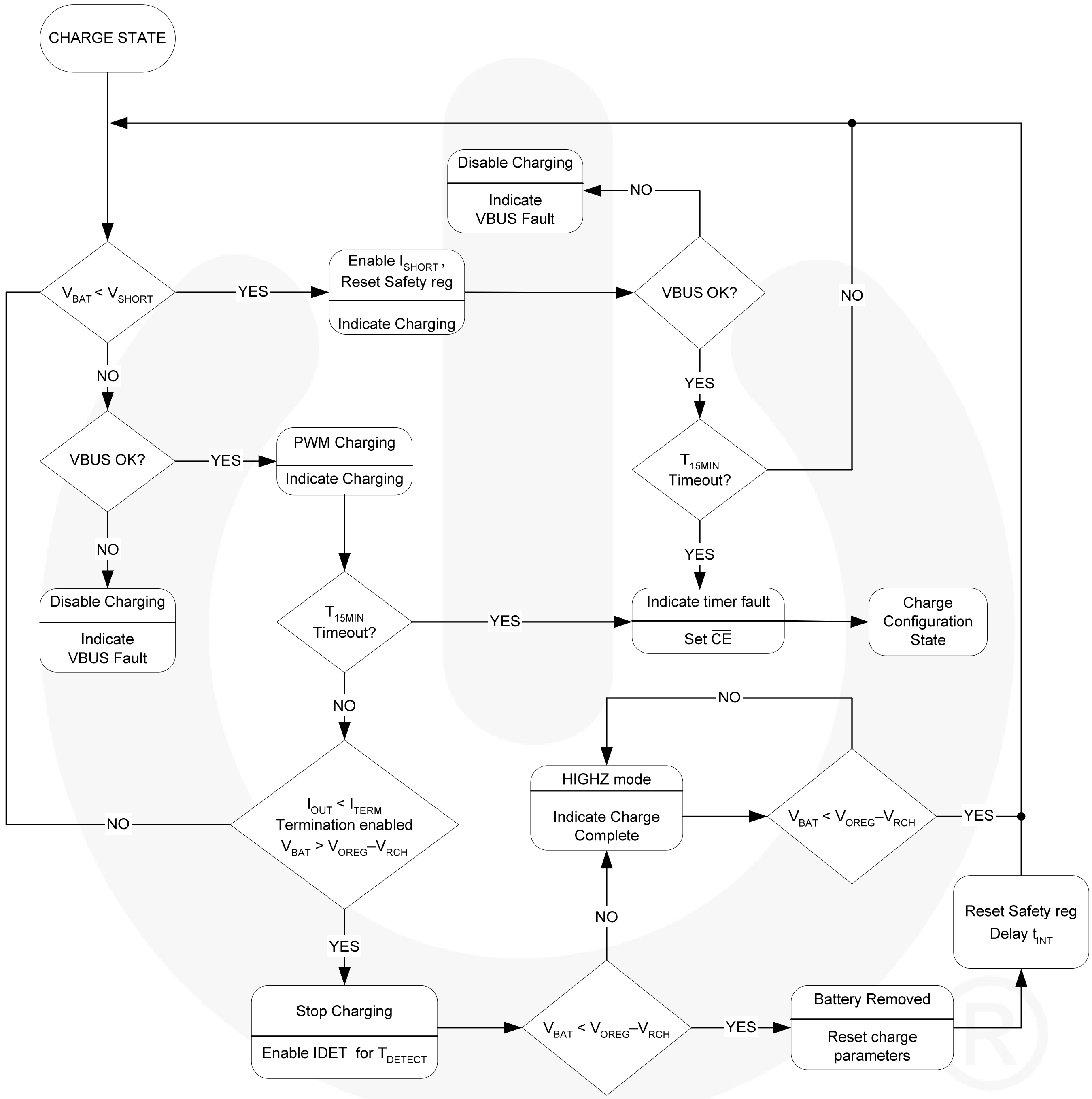


Figure 38. Charge Mode

Flow Charts (Continued)

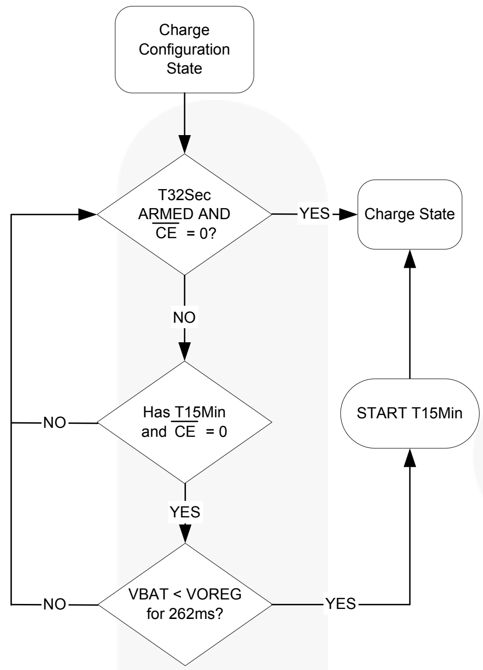


Figure 39. Charge Configuration

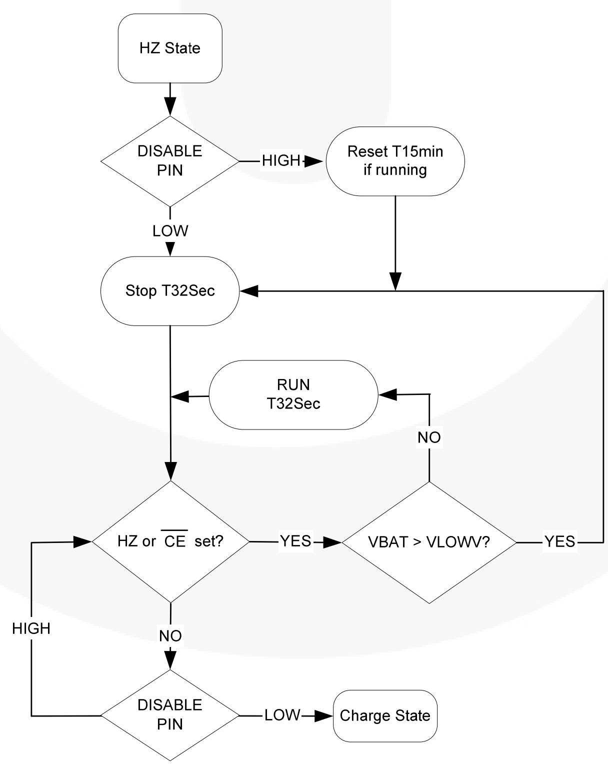


Figure 40. HZ-State

Flow Charts (Continued)

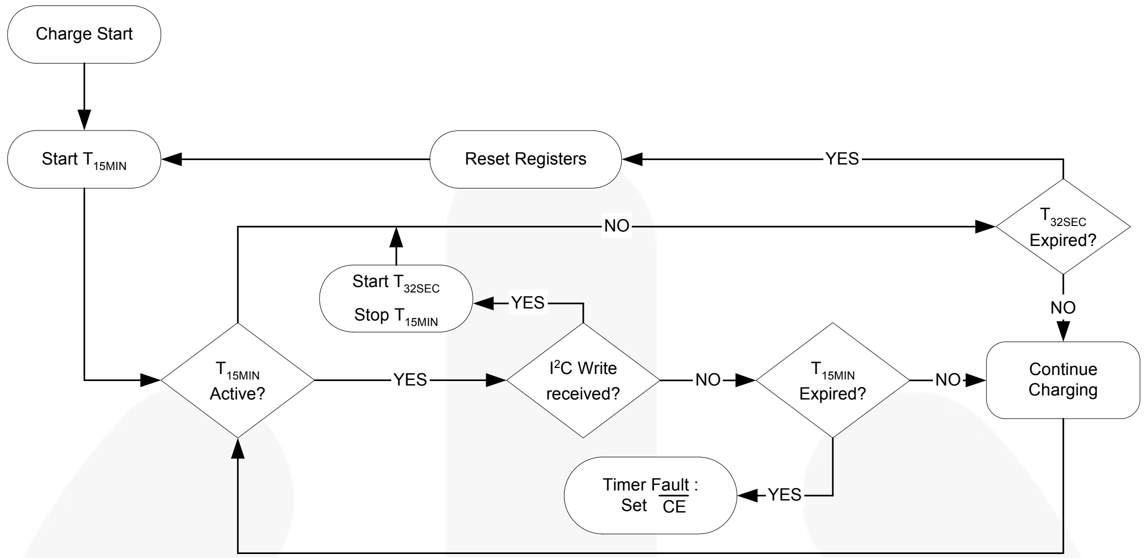


Figure 41. Timer Flow Chart for FAN54010, FAN54012, FAN54013

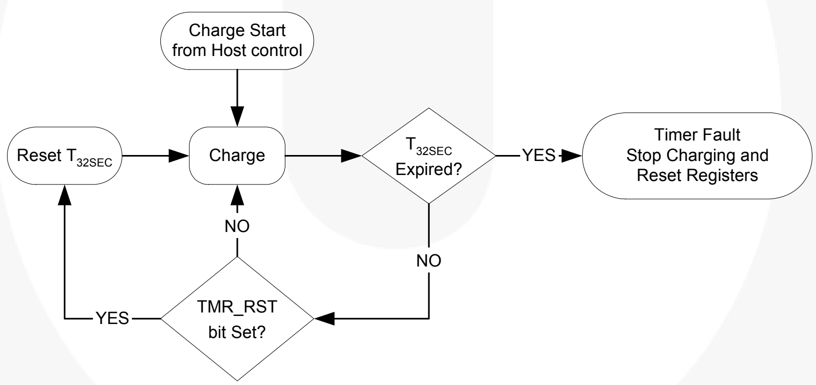


Figure 42. Timer Flow Chart for FAN54011 and FAN54014

Special Charger

FAN54013, FAN54014 Only

The FAN54013 and FAN54014 have additional functionality to limit input current in case a current-limited "special charger" is supplying VBUS. These slowly increase the charging current until either:

- I_{INLIM} or $I_{OCHARGE}$ is reached

or

- $V_{BUS}=V_{SP}$.

If V_{BUS} collapses to V_{SP} when the current is ramping up, the FAN54013 and FAN54014 charge with an input current that keeps $V_{BUS}=V_{SP}$. When the V_{SP} control loop is limiting the charge current, the SP bit (REG5[4]) is set.

Table 8. V_{SP} as Function of SP Bits (REG5[2:0])

SP (REG5[2:0])			
DEC	**BIN**	**HEX**	**V_{SP}**
0	000	00	4.213
1	001	01	4.293
2	010	02	4.373
3	011	03	4.453
4	**100**	**04**	**4.533**
5	101	05	4.613
6	110	06	4.693
7	111	07	4.773

Safety Settings

FAN54013 and FAN54014 Only

The FAN54013 and FAN54014 contain a SAFETY register (REG6) that prevents the values in OREG (REG2[7:2]) and IOCHARGE (REG4[6:4]) from exceeding the values of the VSAFE and ISAFE values.

After V_{BAT} exceeds V_{SHORT}, the SAFETY register is loaded with its default value and may be written only before any other register is written. After writing to any other register, the SAFETY register is locked until V_{BAT} falls below V_{SHORT}.

The ISAFE (REG6[6:4]) and VSAFE (REG6[3:0]) registers establish values that limit the maximum values of $I_{OCHARGE}$ and V_{OREG} used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively; the VSAFE, ISAFE value appears as the OREG, IOCHARGE register value, respectively.

Table 9. I_{SAFE} ($I_{OCHARGE}$ Limit) as Function of ISAFE Bits (REG6[6:4])

ISAFE (REG6[6:4])					
DEC	**BIN**	**HEX**	**V_{RSENSE} (mV)**	**I_{SAFE} (mA)**	
				68 mΩ	**100 mΩ**
0	000	00	37.4	550	374
1	001	01	44.2	650	442
2	010	02	51.0	750	510
3	011	03	57.8	850	578
4	**100**	**04**	**71.4**	**1050**	**714**
5	101	05	78.2	1150	782
6	110	06	91.8	1350	918
7	111	07	98.6	1450	986

Table 10. V_{SAFE} (V_{OREG} Limit) as Function of VSAFE Bits (REG6[3:0])

VSAFE (REG6[3:0])				
DEC	**BIN**	**HEX**	**Max. OREG (REG2[7:2])**	**VOREG Max.**
0	**0000**	**00**	**100011**	**4.20**
1	0001	00	100100	4.22
2	0010	01	100101	4.24
3	0011	02	100110	4.26
4	0100	03	100111	4.28
5	0101	04	101000	4.30
6	0110	05	101001	4.32
7	0111	06	101010	4.34
8	1000	07	101011	4.36
9	1001	08	101100	4.38
10	1010	09	101101	4.40
11	1011	0A	101110	4.42
12	1100	0B	101111	4.44
13	1101	0C	110000	4.44
14	1110	0D	110001	4.44
15	1111	0E	110010	4.44

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{CF} (about 120°C), the charger reduces its output current to 550 mA to prevent overheating. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes at programmed current after the die cools to about 120°C.