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April 2015

FAN54053
High Efficiency, 1.55 A, Li-Ion Switching Charger with Power Path, USB-OTG, in a Small Solution Footprint

Features

- Fully Integrated, High-Efficiency Switch-Mode Charger for Single-Cell Li-Ion and Li-Polymer Batteries
- Power Path Circuit Ensures Fast System Startup with a Dead Battery when VBUS is Connected
- 1.55 A Maximum Charge Current
- Programmable High Accuracy Float Voltage:
  - ±0.5% at 25°C
  - ±1% from 0 to 125°C
- ±5% Input and Charge Current Regulation Accuracy
- Temperature-Sense Input for JEITA Compliance
- Thermal Regulation and Shutdown
- 4.2 V at 2.3 A Production Test Support
- 5 V, 500 mA Boost Mode for USB OTG
- 28 V Absolute Maximum Input Voltage
- 6 V Maximum Input Operating Voltage
- Programmable through High-Speed I^2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Float Voltage
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1 μH External Inductor
- Safety Timer with Reset Control
- Dynamic Input Voltage Control
- Very Low Battery Current when Charger Inactive

Applications

- Cell Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

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Description

The FAN54053 is a 1.55 A USB-compliant switch-mode charger featuring power path operation, USB OTG boost support, JEITA temperature control, and production test mode support, in a small 25 bump, 0.4 mm pitch WLCSP package.

To facilitate fast system startup, the IC includes a power path circuit, which disconnects the battery from the system rail, ensuring that the system can power up quickly following a VBUS connection. The power path circuit ensures that the system rail stays up when the charger is plugged in, even if the battery is dead or shorted.

The charging parameters; float voltage, input voltage regulation, input current, charging current, and other operating modes are programmable through an I^2C Interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of external passive components.

The FAN54053 provides battery charging in three phases: conditioning, constant current and constant voltage. The IC automatically restarts the charge cycle when the battery falls below a voltage threshold. If the input source is removed, the IC enters a high-impedance mode blocking battery current from leaking to the input. Charge status is reported back to the host through the I^2C port.

Dynamic input voltage control prevents a weak adapter's voltage from collapsing, ensuring charging capability from such adapters.

The FAN54053 is available in a space saving 2.4 mm x 2.0 mm WLCSP package.

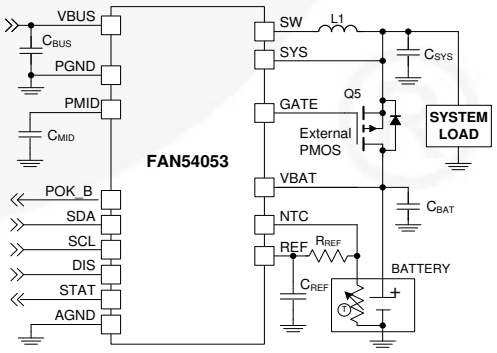


Figure 1. Typical Application

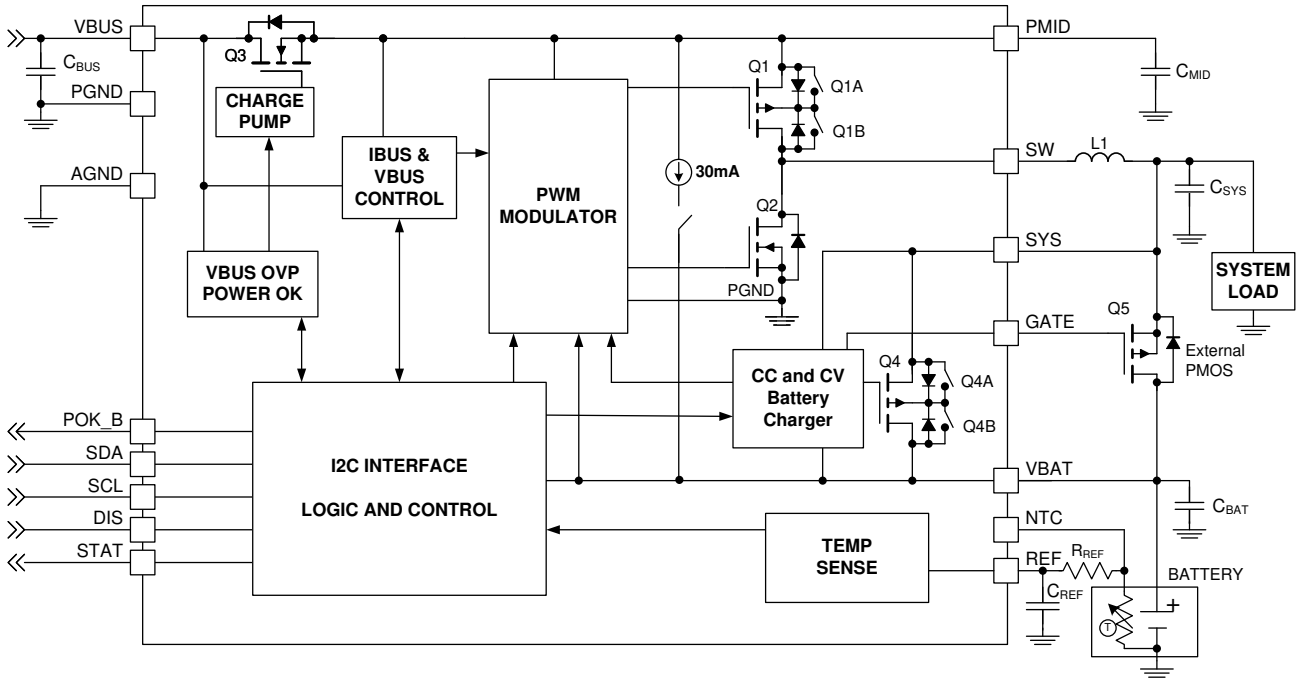
Ordering Information

Part Number	Temperature Range	Package	PN Bits: IC_INFO[5:3]	Packing Method
FAN54053UCX	-40 to 85°C	25-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.4 mm Pitch	010	Tape and Reel

Table 1. Feature Summary

Part Number	Slave Address	Automatic Charge	Battery Absent Behavior	E1 Pin	Watchdog Timer Default
FAN54053	1101011	No	On	POK_B	Disabled

Block Diagram



PMID	Q1A	Q1B
Greater than V_{BAT}	ON	OFF
Less than V_{BAT}	OFF	ON

SYS	Q4A	Q4B
Greater than V_{BAT}	ON	OFF
Less than V_{BAT}	OFF	ON

Figure 2. IC and System Block Diagram

Table 2. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Unit
L1	1 µH, 20%, 2.7 A, 2016	Toko DFE201610E-1R0M or Equivalent	L	1.0	µH
			DCR (Series R)	48	mΩ
C_{BAT}, C_{SYS}	10 µF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M TDK: C1608X5R0J106M	C	10	µF
C_{MID}	4.7 µF, 10%, 10 V, X5R, 0603	Murata: GRM188R61A475K TDK: C1608X5R1A475K	C(1)	4.7	µF
C_{BUS},	1.0 µF, 10%, 25 V, X5R, 0603	Murata GRM188R61E105K TDK:C1608X5R1E105M	C	1.0	µF
Q5	PMOS,12 V, 16 mΩ, MLP2x2	Fairchild FDMA905P	$R_{DS(ON)}$	16	mΩ
C_{REF}	1 µF, 10%, 6.3 V, X5R, 0402		C	1.0	µF

Note:

1. 10 V rating is sufficient for C_{MID} since PMID is protected from over-voltage surges on VBUS by Q3.

Pin Configuration

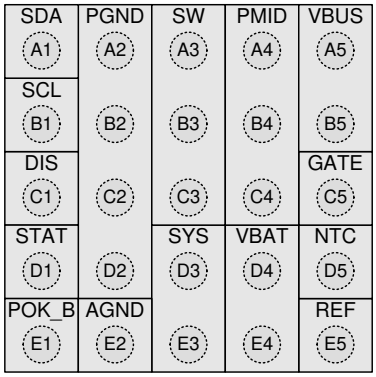


Figure 3. Top View

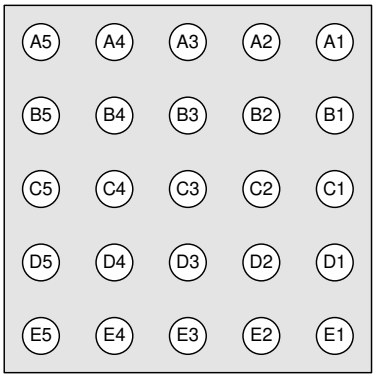


Figure 4. Bottom View

Pin Definitions

Pin #	Name	Description
A1	SDA	**I²C Interface Serial Data**. This pin should not be left floating.
B1	SCL	**I²C Interface Serial Clock**. This pin should not be left floating.
C1	DIS	**Disable**. If this pin is held HIGH, Q1 and Q3 are turned off, creating a HIGH Z condition at VBUS and the PWM converter is disabled.
D1	STAT	**Status**. Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in progress; can be used to signal the host processor when a fault condition occurs.
E1	POK_B	**Power OK**. Open-drain output that pulls LOW when VBUS is plugged in and the battery has risen above V_{LOWV}. This signal is used to signal the host processor that it can begin to draw significant current.
A2 – D2	PGND	**Power Ground**. Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{MID} should be as short as possible.
E2	AGND	**Analog Ground**. All IC signals are referenced to this node.
A3 – C3	SW	**Switching Node**. Connect to output inductor.
D3 – E3	SYS	**System Supply**. Output voltage of the switching charger and input to the power path controller. Bypass SYS to PGND with a 10 µF capacitor.
A4 – C4	PMID	**Power Input Voltage**. Power input to the charger regulator, bypass point for the input current sense. Bypass with a minimum of a 4.7 µF, 6.3 V capacitor to PGND.
D4 – E4	VBAT	**Battery Voltage**. Connect to the positive (+) terminal of the battery pack. Bypass with a 10 µF capacitor to PGND. VBAT is a power path connection.
A5 – B5	VBUS	**Charger Input Voltage** and USB-OTG output voltage. Bypass with a 1 µF capacitor to PGND.
C5	GATE	**External MOSFET Gate**. This pin controls the gate of an external P-channel MOSFET transistor used to augment the internal ideal diode. The source of the P-channel MOSFET should be connected to SYS and the drain should be connected to VBAT.
D5	NTC	**Thermistor input**. The IC compares this node with taps on a resistor divider from REF to inhibit auto-charging when the battery temperature is outside of permitted fast-charge limits.
E5	REF	**Reference Voltage**. REF is a 1.8 V regulated output.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BUS}	Voltage on VBUS Pin	Continuous		-0.3	28.0	V
		Pulsed, 100 ms Maximum Non-Repetitive		-1.0		
V_I	Voltage on PMID Voltage Pin			–0.3	7.0	V
	Voltage on SW, SYS, VBAT, STAT, DIS Pins			–0.3	7.0	
V_O	Voltage on Other Pins			–0.3	6.5[2]	V
$\frac{dV_{BUS}}{dt}$	Maximum V_{BUS} Slope Above 5.5 V when Boost or Charger Active				4	V/µs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114		2000		V
		Charged Device Model per JESD22-C101		500		
	IEC 61000-4-2 System ESD[3]	USB Connector Pins (V_{BUS} to GND)	Air Gap	15		kV
			Contact	8		
T_J	Junction Temperature			–40	+150	°C
T_{STG}	Storage Temperature			–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds				+260	°C

Notes:

2. Lesser of 6.5 V or V_I + 0.3 V.
3. Guaranteed if C_{BUS} ≥1 µF and C_{MID} ≥ 4.7 µF.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	Supply Voltage		4	6	V
$V_{BAT(MAX)}$	Maximum Battery Voltage when Boost enabled			4.5	V
$-\frac{dV_{BUS}}{dt}$	Negative VBUS Slew Rate during VBUS Short Circuit, $C_{MID} \leq 4.7$ µF, *see VBUS Short While Charging*	$T_A \leq 60°C$		4	V/µs
		$T_A \geq 60°C$		2	
T_A	Ambient Temperature		–30	+85	°C
T_J	Junction Temperature *(see Register Bit section)*		–30	+120	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	50	°C/W
θ_{JB}	Junction-to-PCB Thermal Resistance	20	°C/W

Electrical Specifications

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE="0"; OPA_MODE="0" (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for T_J=25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Power Supplies							
I_{VBUS}	VBUS Current	PWM Switching			25		mA
		$V_{BAT} > V_{OREG}$ I_{BUSLIM} = 500 mA			6		mA
		0°C < T_J < 85°C, HZ_MODE = "1", $V_{BAT} > V_{LOWV}$			190	280	µA
I_{BAT_HZ}	Battery Discharge Current in High-Impedance Mode	DIS pin HIGH, or HZ_MODE = "1", V_{BAT}=4.35 V			<1.25	10	µA
I_{BUS_HZ}	Battery Leakage Current to V_{BUS} in High-Impedance Mode	DIS pin HIGH, or HZ_MODE = "1", V_{BUS} Shorted to Ground, V_{BAT}=4.35 V		-5.0	-0.2		µA
Charger Voltage Regulation							
V_{OREG}	Charge Voltage Range			3.51		4.45	V
	Charge Voltage Accuracy	T_A = 25°C, V_{OREG} = 4.35 V		–0.5		+0.5	%
		T_J=0 to 125°C		–1		+1	%
Charging Current Regulation (Fast Charge)							
I_{OCHRG}	Output Charge Current Range	V_{LOWV} < V_{BAT} < V_{OREG}	IO_LEVEL = "0"	550		1550	mA
			IO_LEVEL = "1" (default)	165	200	230	mA
	Charge Current Accuracy	IO_LEVEL = "0"		–5		+5	%
Weak Battery Detection							
V_{LOWV}	Weak Battery Threshold Range			3.35		3.75	V
	Weak Battery Threshold Accuracy			–5		+5	%
	Weak Battery Deglitch Time	Rising Voltage, 2 mV Overdrive			32		ms
PWM Charging Threshold							
V_{BATMIN}	Rising PWM Charging Threshold			3.1	3.2	3.3	V
$V_{BATFALL}$	Falling PWM Charging Threshold				3.0		V
Logic Levels: DIS, SDA, SCL							
V_{IH}	High-Level Input Voltage			1.05			V
V_{IL}	Low-Level Input Voltage					0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{BUS}			0.01	1.00	µA
R_{PD}	DIS Pull-Down Resistance				1		MΩ
Charge Termination Detection							
$I_{(TERM)}$	Termination Current Range	$V_{BAT} > V_{OREG} – V_{RCH}$, $V_{BUS} > V_{SLP}$		50		400	mA
	Termination Current Accuracy	I_{TERM} Setting ≤ 100 mA		–15		+15	%
		I_{TERM} Setting ≥ 200 mA		–5		+5	
	Termination Current Deglitch Time[4]				32		ms

Electrical Specifications (Continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE="0"; OPA_MODE="0" (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for T_J=25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Path (Q4) Control (Precharge)						
I_{PP}	Power Path Maximum Charge Current	IO_LEVEL = "1" (default)	165	200	235	mA
		IO_LEVEL = "0", $I_{BUSLIM} \le$ "01"	165	200	235	mA
		IO_LEVEL = "0", I_{BUSLIM} > "01", $I_{OCHARGE} \le$ "02"	375	450	520	mA
		IO_LEVEL = "0", I_{BUSLIM} > "01", $I_{OCHARGE}$ > "02"	610	730	840	mA
V_{THSYS}	VBAT to SYS Threshold for Q4 and Gate Transition While Charging	(SYS-VBAT) Falling	–6	–5	–3	mV
		(SYS-VBAT) Rising	-1	+1	2	mV
Production Test Mode						
$V_{BAT(PTM)}$[4]	Production Test Output Voltage	1 mA < I_{BAT} < 2 A, V_{BUS}=5.5 V	4.116	4.200	4.284	V
$I_{BAT(PTM)}$[4]	Production Test Output Current	20% Duty with Max. Period 10 ms	2.3			A
Battery Temperature Monitor (NTC)						
T1	T1 (0°C) Temperature Threshold		71.9	73.9	75.9	% of V_{REF}
T2	T2 (10°C) Temperature Threshold		62.6	64.6	66.6	
T3	T3 (45°C) Temperature Threshold		31.9	32.9	34.9	
T4	T4 (60°C) Temperature Threshold		21.3	23.3	25.3	
Input Power Source Detection						
$V_{IN(MIN)1}$	VBUS Input Voltage Rising	To Initiate and Pass VBUS Validation		4.35	4.45	V
$V_{IN(MIN)2}$	Minimum VBUS during Charge	During Charging		3.71	3.94	V
t_{VBUS_VALID}[4]	VBUS Validation Time			30		ms
V_{BUS} Control Loop						
V_{BUSLIM}	VBUS Loop Setpoint Accuracy		–3		+3	%
Input Current Limit						
I_{BUSLIM}	Charger Input Current Limit Threshold	I_{BUSLIM} = "00"	450	475	500	mA
		I_{BUSLIM} = "01"		760		
		I_{BUSLIM} = "10"	972	1080	1188	
V_{REF} Bias Generator						
V_{REF}	Bias Regulator Voltage	V_{BUS} > $V_{IN(MIN)1}$		1.8		V
	Short-Circuit Current Limit			2.5		mA
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below V_{OREG}	100	120	150	mV
	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		130		ms
STAT, POK_B Output						
$V_{STAT(OL)}$	STAT Output Low	I_{STAT} = 10 mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT} = 5 V			1	µA

Electrical Specifications (Continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE="0"; OPA_MODE="0" (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for T_J=25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Battery Detection						
I_{DETECT}	Battery Detection Current before Charge Done (Sink Current)[5]	Begins after Termination Detected and $V_{BAT} \le V_{OREG} - V_{RCH}$		–1.9		mA
t_{DETECT}	Battery Detection Time			262		ms
Sleep Comparator						
V_{SLP}	Sleep-Mode Entry Threshold, $V_{BUS} - V_{BAT}$	2.3 V ≤ V_{BAT} ≤ V_{OREG}, V_{BUS} Falling	0	0.04	0.10	V
Power Switches *(see Figure 2)*						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID)	$I_{IN(LIMIT)}$ = 500 mA		180	400	mΩ
	Q1 On Resistance (PMID to SW)			130	225	
	Q2 On Resistance (SW to GND)			150	225	
	Q4 On Resistance (SYS to VBAT)	V_{BAT}=4.35 V		70	100	mΩ
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold[6]	Low-Side MOSFET (Q2) Cycle-by-Cycle Current Limit		180		mA
Charger PWM Modulator						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			0		%
Boost Mode Operation (OPA_MODE=1)						
V_{BOOST}	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 200 mA	4.80	5.07	5.20	V
		3.0 V < V_{BAT} < 4.5 V, I_{LOAD} from 0 to 500 mA	4.77	5.07	5.20	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{BAT} = 3.6 V, I_{LOAD} = 0 A		250	350	μA
$I_{LIMPK(BST)}$	Q2 Peak Current Limit		1350	1550	1950	mA
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.32		V
		To Start Boost Regulator		2.48	2.70	
VBUS Load Resistance						
R_{VBUS}	VBUS to PGND Resistance	Normal Operation		500		kΩ
		VBUS Validation		100		Ω
Protection and Timers						
$VBUS_{OVP}$	VBUS Over-Voltage Shutdown	V_{BUS} Rising	6.09	6.29	6.49	V
	Hysteresis	V_{BUS} Falling		100		mV
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle Peak Current Limit	Charge Mode		3		A
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	1.95	2.00	2.07	V
	Hysteresis			100		mV
I_{SHORT}	Linear Charging Current	V_{BAT} < V_{SHORT}		30		mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold[4]	T_J Rising		145		°C
	Hysteresis[4]	T_J Falling		25		
T_{CF}	Thermal Regulation Threshold[4]	Charge Current Reduction Begins		120		°C
t_{INT}	Detection Interval			2.1		s

Electrical Specifications (Continued)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0 V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA=0 or 1.8 V; and typical values are for T_J=25°C. Min. and Max. values are not tested in production, but are determined by characterization.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{32S}	32-Second Timer[7]	Charger Enabled	20.5	25.2	28.0	s
		Charger Disabled	18.0	25.2	34.0	
t_{15MIN}	15-Minute Timer	15-Minute Mode	12.0	13.5	15.0	min
Δt_{LF}	Low-Frequency Timer Accuracy	Charger Inactive	–23		27	%

Notes:

4. Guaranteed by design; not tested in production.
5. Negative current is current flowing from the battery to VBUS (discharging the battery).
6. Q2 always turns on for 60 ns, then turns off if current is below I_{SYNC}.
7. This tolerance (%) applies to all timers on the IC, including soft-start and deglitching timers.

I^2C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High-Speed Mode, $C_B \leq 100$ pF			3400	
		High-Speed Mode, $C_B \leq 400$ pF			1700	
t_{BUF}	BUS-free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		Fast Mode Plus		0.5		µs
		High-Speed Mode, $C_B \leq 100$ pF		160		ns
		High-Speed Mode, $C_B \leq 400$ pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High-Speed Mode, $C_B \leq 100$ pF		60		ns
		High-Speed Mode, $C_B \leq 400$ pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		Fast Mode Plus	0		450	ns
		High-Speed Mode, $C_B \leq 100$ pF	0		70	ns
		High-Speed Mode, $C_B \leq 400$ pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	

I^2C Timing Specifications (Continued)

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FCL}	SCL Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High-Speed Mode, $C_B \leq 100$ pF		10	40	
		High-Speed Mode, $C_B \leq 400$ pF		20	80	
t_{RCL1}	Rise Time of SCL after a Repeated START Condition and after ACK Bit	High-Speed Mode, $C_B \leq 100$ pF		10	80	ns
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
t_{RDA}	SDA Rise Time	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
t_{FDA}	SDA Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

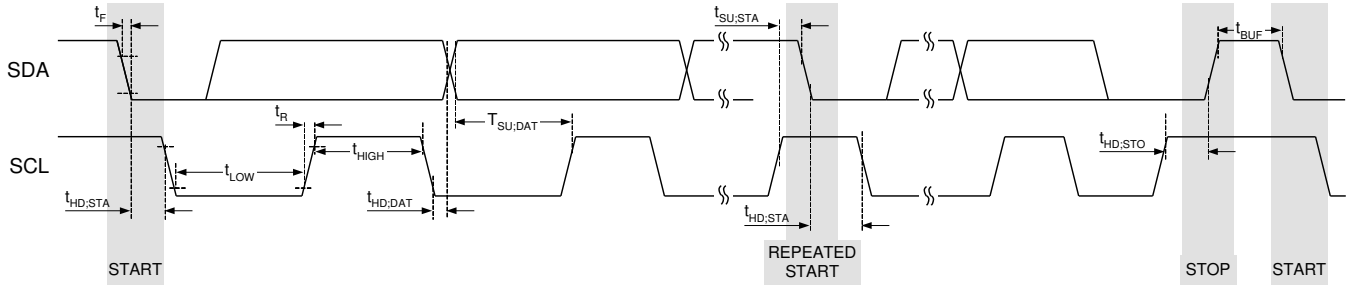
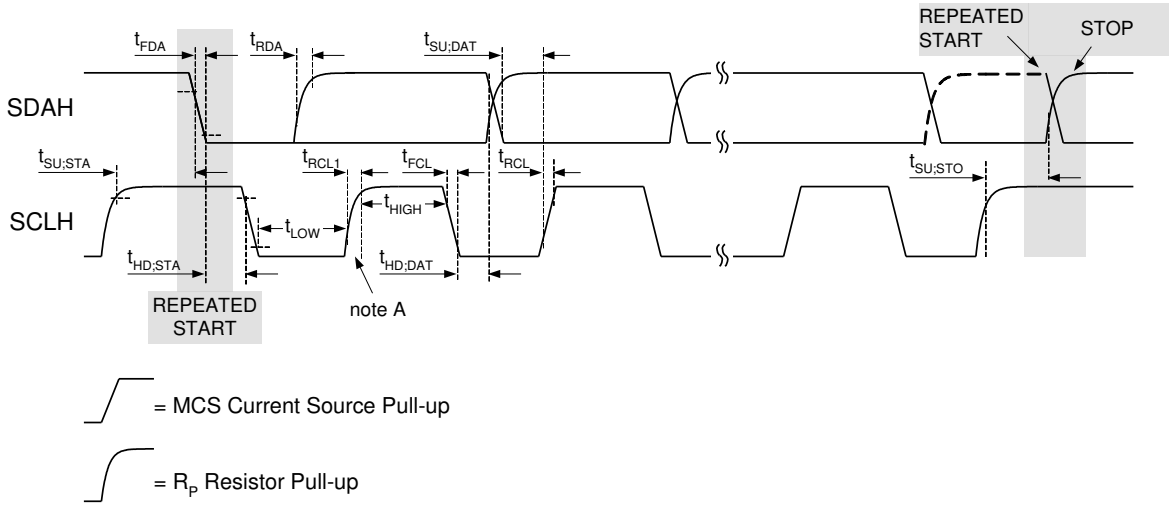


Figure 5. I^2C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 6. I^2C Interface Timing for High-Speed Mode

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.35 V, $I_{OCHARGE}$=950 mA, V_{BUS}=5.0 V, and T_A=25°C.

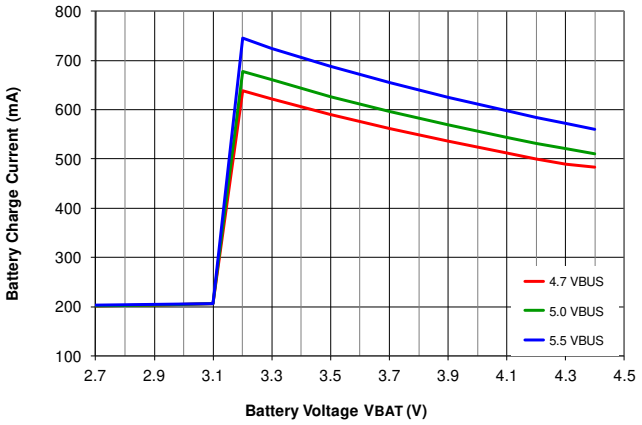


Figure 7. Battery Charge Current vs. V_{BUS} with I_{BUSLIM}=500 mA

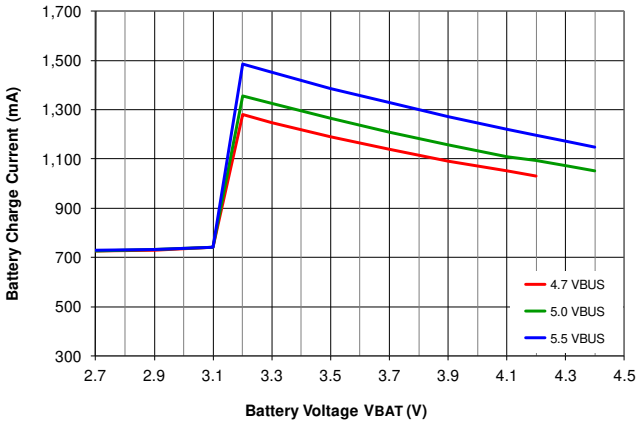


Figure 8. Battery Charge Current vs. V_{BUS} with I_{BUSLIM}=1100 mA

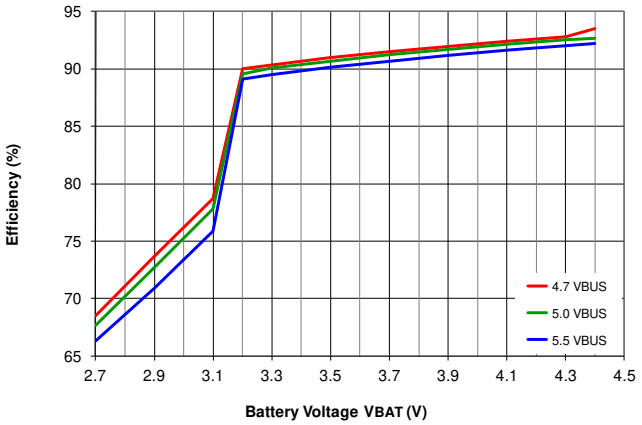


Figure 9. Efficiency vs. V_{BUS}, I_{BUSLIM}=500 mA, I_{SYS}=0

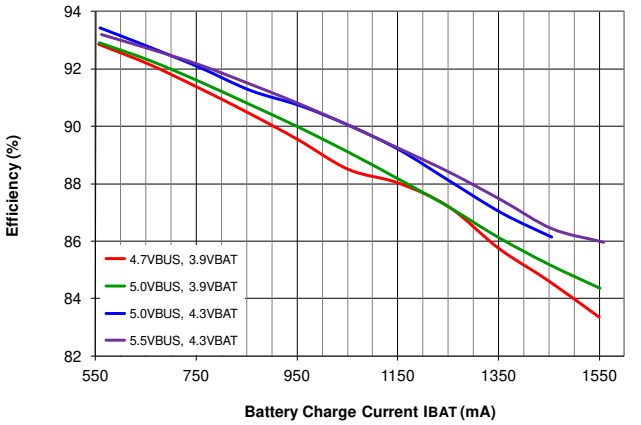


Figure 10. Efficiency vs. Charging Current, I_{BUSLIM}=No Limit

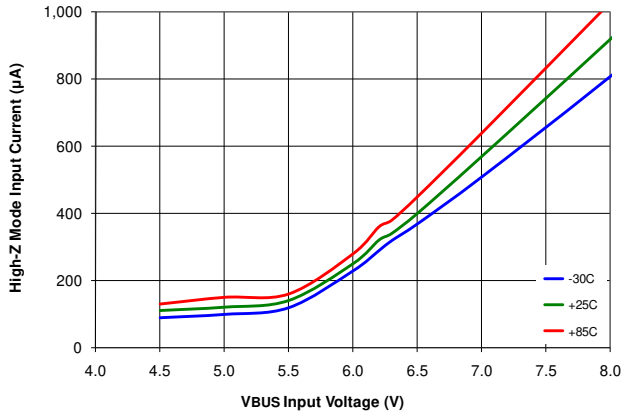


Figure 11. HZ Mode V_{BUS} Current vs. Temperature, 3.7 V_{BAT}

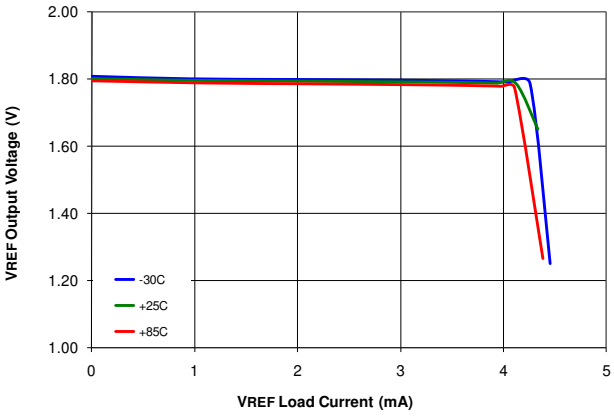


Figure 12. V_{REF} vs. Load Current, Over-Temperature

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.35 V, $I_{OCHARGE}$=950 mA, V_{BUS}=5.0 V, and T_A=25°C.

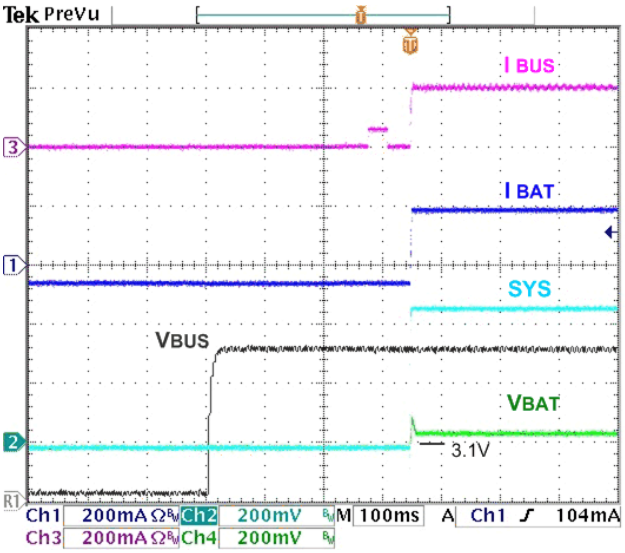


Figure 13. Charger Startup at V_{BUS} Plug-In, 500 mA I_{BUSLIM}, 3.1 V_{BAT}, 50 Ω SYS Load, CE# = 0, IO_LVL=1

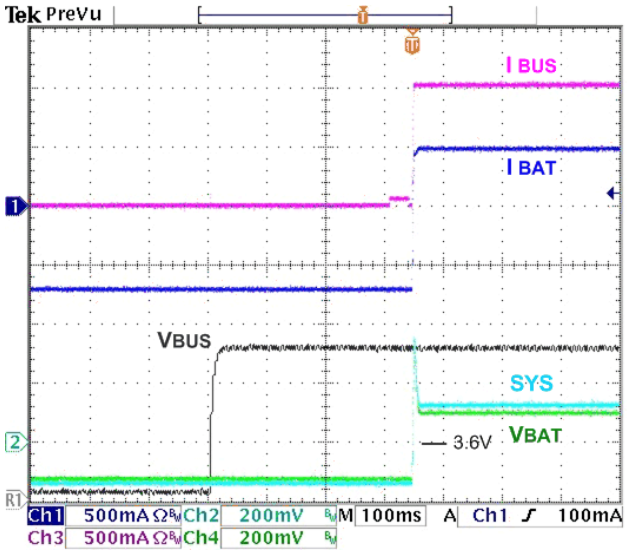


Figure 14. Charger Startup at V_{BUS} Plug-In, 1100 mA I_{BUSLIM}, 3.6 V_{BAT}, 700 mA SYS Load, CE# = 0, IO_LVL=0

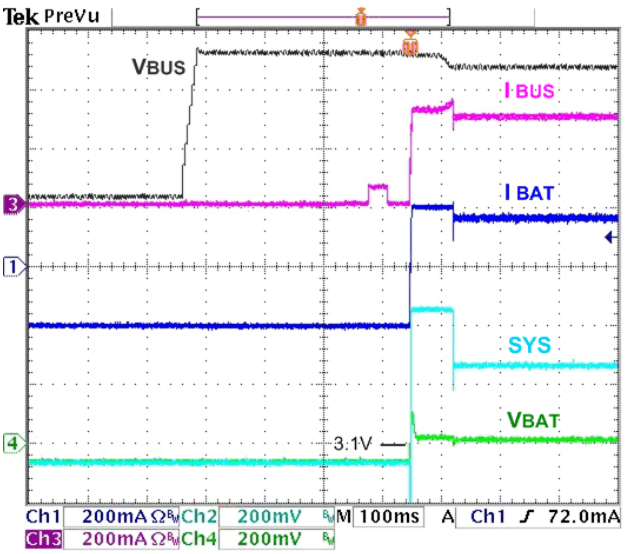


Figure 15. Charger Startup at V_{BUS} Plug-In Using 300 mA Current Limited Source, 500 mA I_{BUSLIM}, 3.1 V_{BAT}, 200 mA SYS Load, CE# = 0, IO_LVL=0

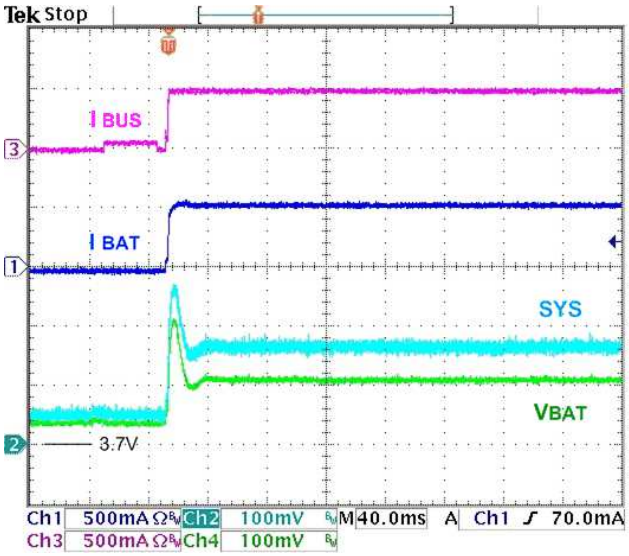


Figure 16. Charger Startup with HZ Bit Reset, 500 mA I_{BUSLIM}, 950 mA I_{CHARGE}, 50 Ω SYS Load, CE# = 0

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.35 V, $I_{OCHARGE}$=950 mA, V_{BUS}=5.0 V, and T_A=25°C.

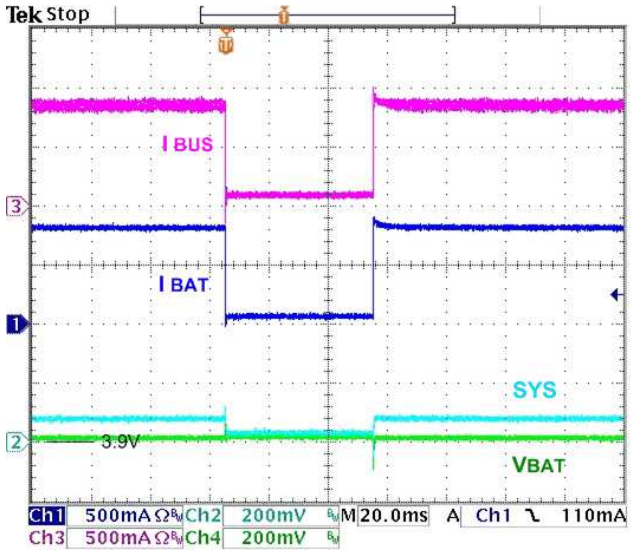


Figure 17. Battery Removal / Insertion while Charging, TE=0, 3.9 V_{BAT}, I_{CHRG}=950 mA, I_{BUSLIM}=No Limit, 50 Ω SYS Load

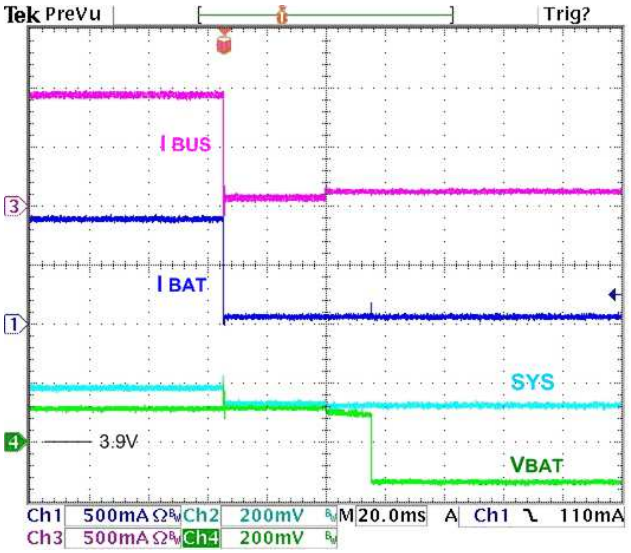


Figure 18. Battery Removal / Insertion when Charging, TE=1, 3.9 V_{BAT}, I_{BUSLIM}=No Limit, 50 Ω SYS Load

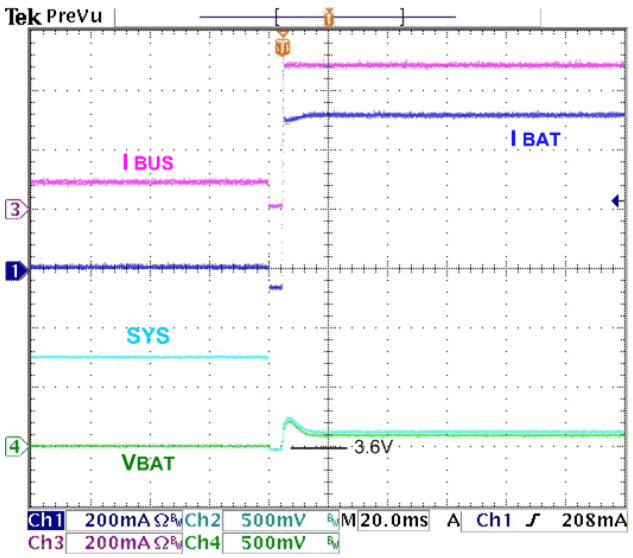


Figure 19. Charger Enable (CE# = 1 -0) with V_{BUS} Applied, I_{BUSLIM}=500 mA, 200 mA SYS Load, IO_LVL=0

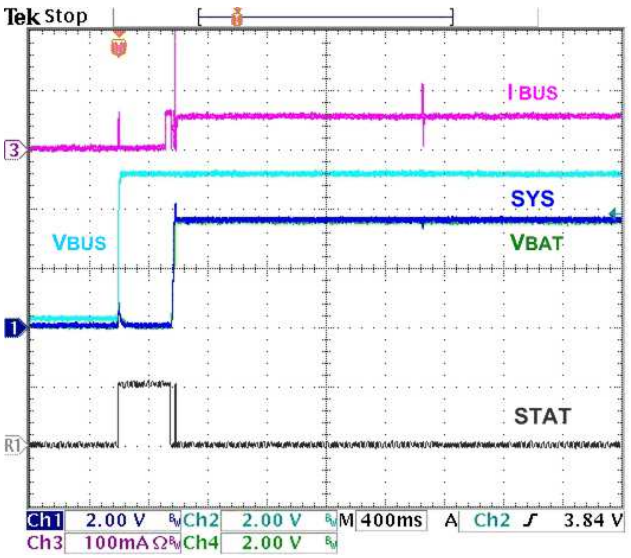


Figure 20. No Battery at V_{BUS} Power-Up, 100 Ω SYS Load, 1 kΩ V_{BAT} Load

GSM Typical Characteristics

A 2.0 A GSM pulse applied at V_{BAT} with 5 µs rise / fall time. Simultaneous to GSM pulse, 50 Ω additional load applied at SYS.

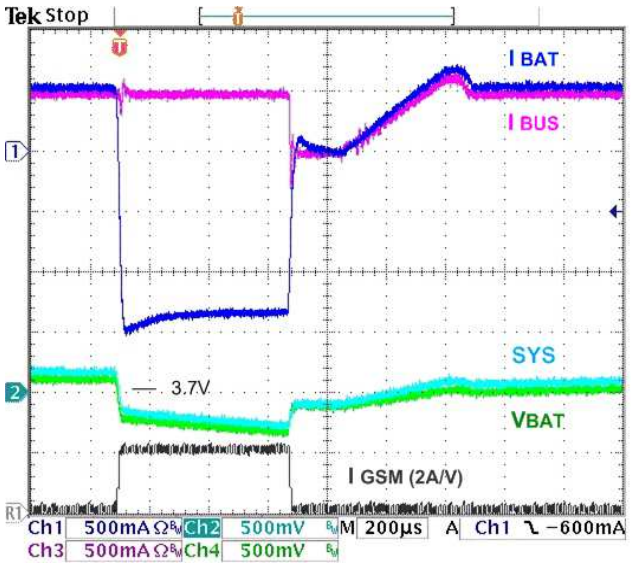


Figure 21. 2.0 A GSM Pulse Response, I_{BUSLIM}=500 mA Control, I_{CHRG}=950 mA, 3.7 V_{BAT}, OREG=4.35 V

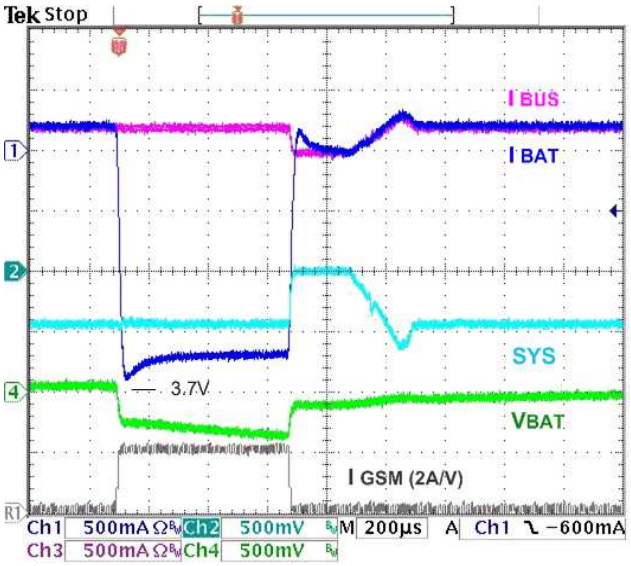


Figure 22. 2.0 A GSM Pulse Response, I_{BUSLIM}=500 mA, I_{CHRG}=950 mA, 3.7 V_{BAT}, OREG=4.35 V, 200 mA Source Current Limit

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

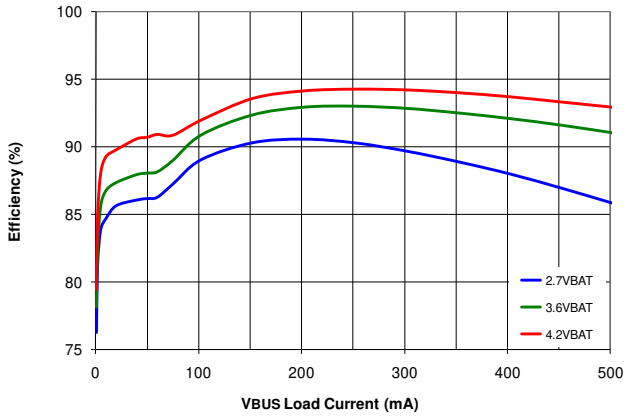


Figure 23. Efficiency vs. I_{BUS} Over V_{BAT}

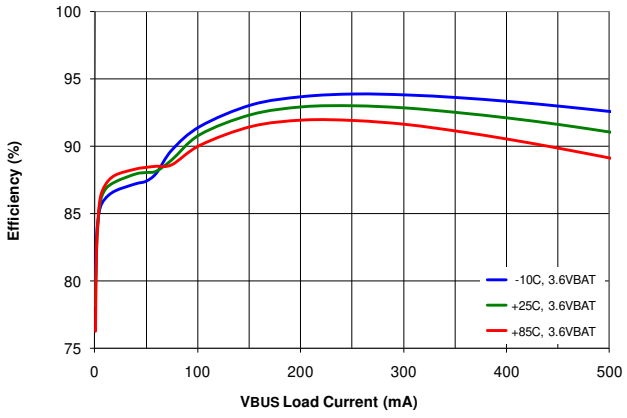


Figure 24. Efficiency vs. I_{BUS} Over-Temperature, 3.6 V_{BAT}

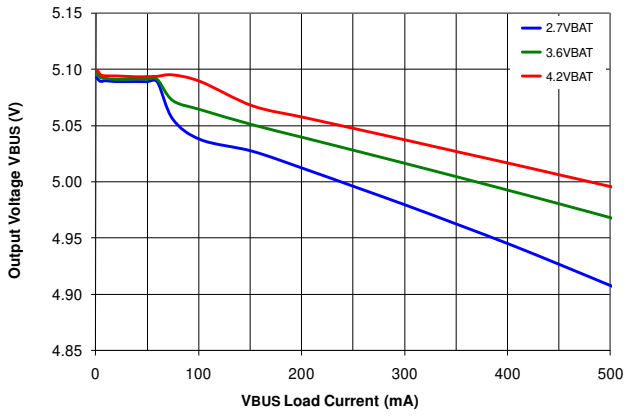


Figure 25. Regulation vs. I_{BUS} Over V_{BAT}

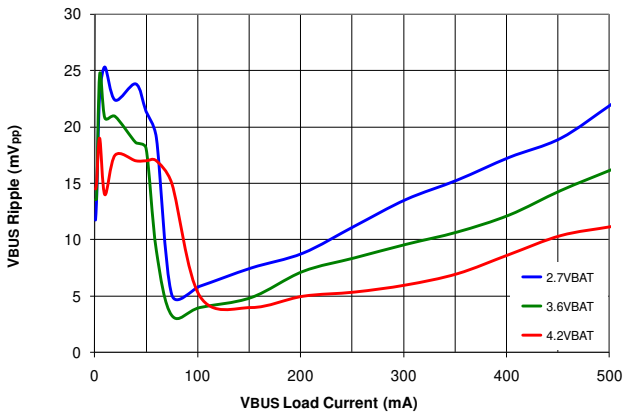


Figure 26. Output Ripple vs. I_{BUS} Over V_{BAT}

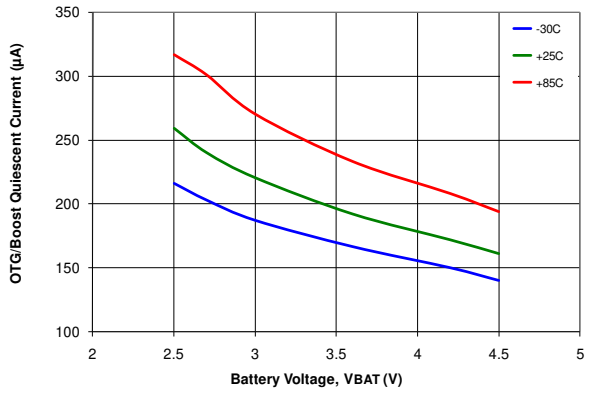


Figure 27. Quiescent Current (I_Q) vs. V_{BAT} Over-Temperature

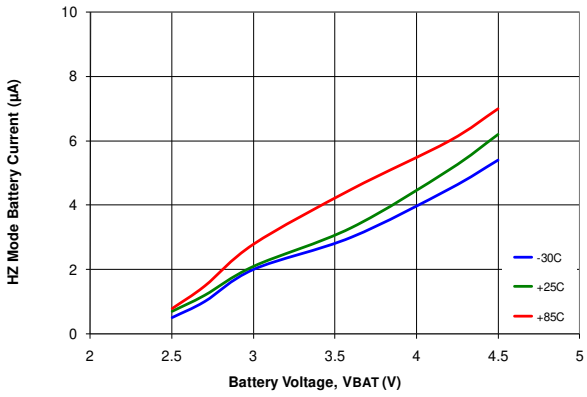


Figure 28. Battery Discharge Current vs. V_{BAT}, HZ / Sleep Mode

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

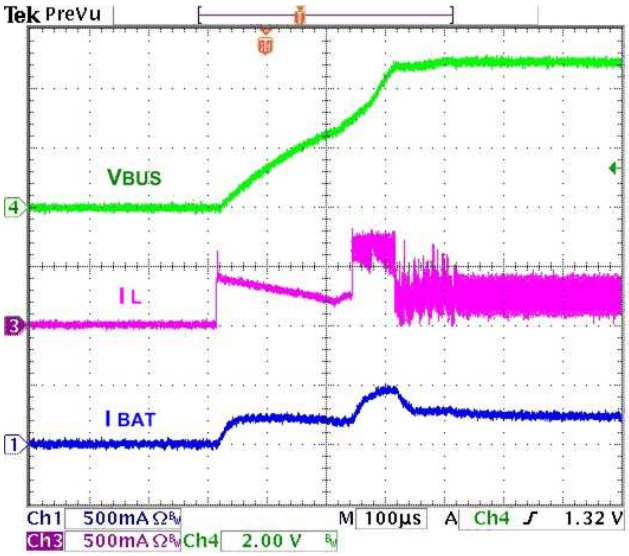


Figure 29. OTG Startup, 50 Ω Load, 3.6 V_{BAT} External / Additional 10 µf on V_{BUS}

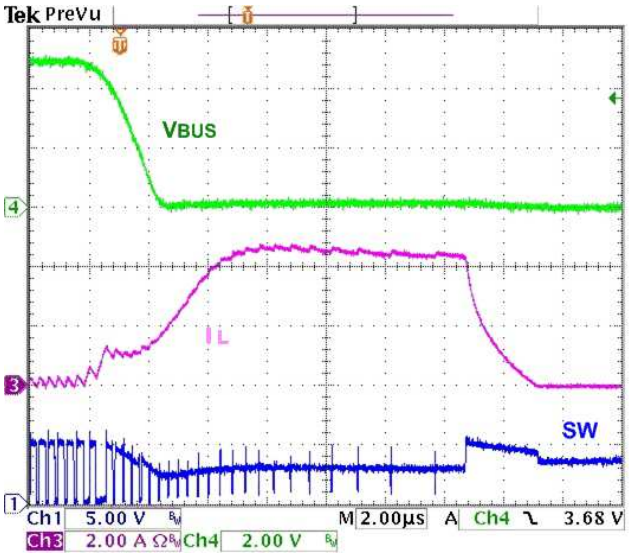


Figure 30. OTG V_{BUS} Overload Response

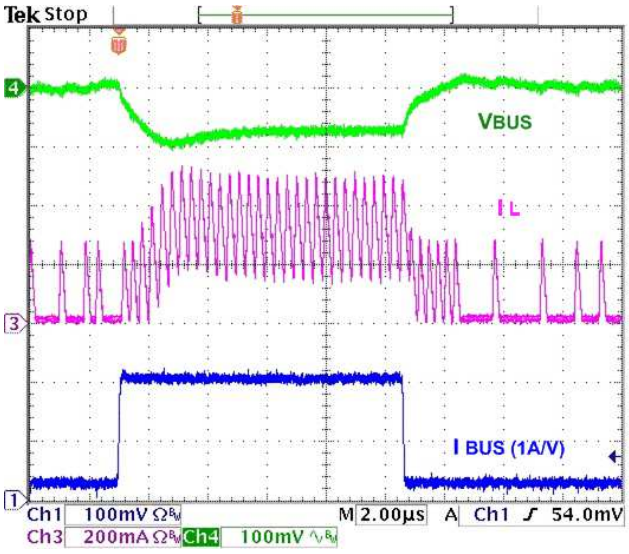


Figure 31. Load Transient, 20-200-20 mA I_{BUS}, $t_{RISE/FALL}$=100 ns

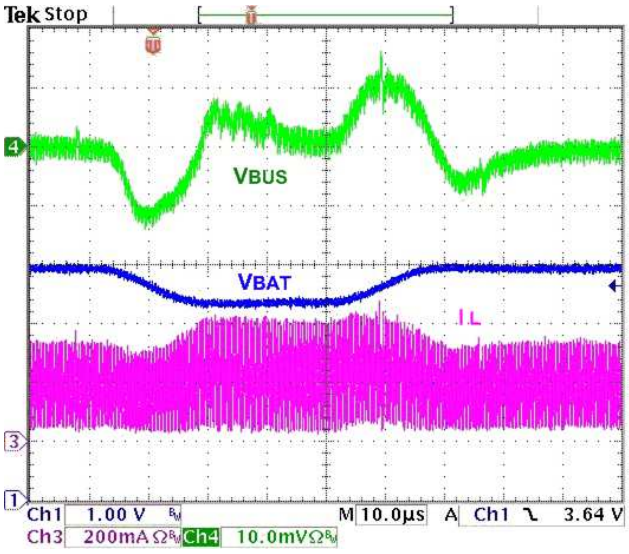


Figure 32. Line Transient, 50 Ω Load, 3.9-3.3-3.9 V_{BAT}, $t_{RISE/FALL}$=10 µs

Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

FAN54053 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The FAN54053 employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The FAN54053 has four operating modes:

1. Charge Mode:
   Charges a single-cell Li-ion or Li-polymer battery.
2. Boost Mode:
   Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator, using the battery as input.
3. High-Impedance Mode:
   Both the boost and charging circuits are OFF in this mode. Current flow from VBUS to the battery or from the battery to VBUS is blocked in this mode. This mode consumes very little current from VBUS or the battery.
4. Production Test Mode:
   This mode provides 4.35 V output on VBAT and supplies a load current of up to 2.3 A.

Charge Mode and Registers

Charge Mode

In Charge Mode, FAN54053 employs six regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an internal sense MOSFET.
3. VBUS Voltage: This loop is designed to prevent the input supply from being dragged below V_{BUSLIM} (typically 4.5 V) when the input power source is current limited. An example of this would be a travel charger. This loop cuts back the current when V_{BUS} approaches V_{BUSLIM}, allowing the input source to run in current limit.
4. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance works in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the current through Q4 drops below the I_{TERM} threshold.
5. Pre-charge: When V_{BAT} is below V_{BATMIN}, Q4 operates as a linear current source and modulates its current to ensure that the voltage on SYS stays above 3.4 V.
6. Temperature: If the IC's junction temperature reaches 120°C, charge current is reduced until the IC's temperature is below 120°C.

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. The synchronous rectifier (Q2) has a negative current limit that turns off Q2 at 140 mA to prevent current flow from the battery.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

During the current regulation phase of charging, I_{BUSLIM} or the programmed charging current limits the amount of current available to charge the battery and power the system.

During the voltage regulation phase of charging, assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines.

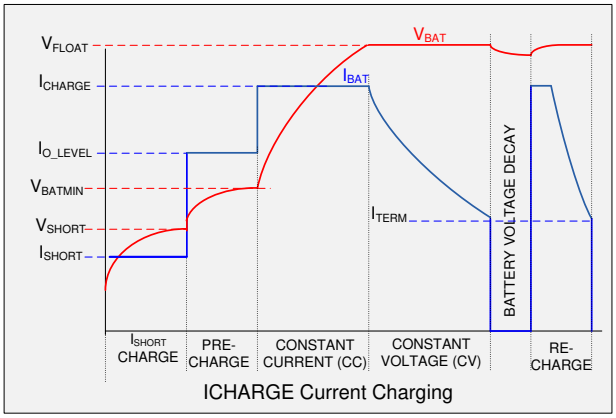


Figure 33. Charge Curve, I_{CHARGE} Not Limited by I_{BUSLIM}

The FAN54053 is designed to work with a current-limited input source at VBUS as shown below:

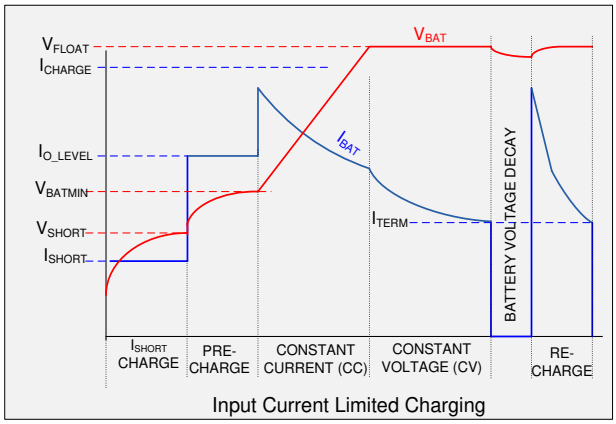


Figure 34. Charge Curve, I_{BUSLIM} Limits I_{CHARGE}

The following charging parameters can be programmed by the host through I^2C:

Table 3. Programmable Charging Parameters

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG2[7:2]
Battery Charging Current Limit	$I_{OCHARGE}$	REG4[6:3]
Input Current Limit	I_{BUSLIM}	REG1[7:6]
Charge Termination Limit	I_{TERM}	REG4[2:0]
Weak Battery Voltage	V_{LOWV}	REG1[5:4]
VBUS Control	V_{BUSLIM}	REG5[2:0]

Output Voltage Regulation (V_{OREG})

The charger output or "float" voltage can be programmed by the OREG (REG02[7:2]) bits from 3.51 V to 4.45 V in 20 mV increments. The defauilt setting is 3.55 V.

See OREG *Register Bit Definitions*

Battery Charging Current Limit ($I_{OCHARGE}$)

When the IO_LEVEL bit is set (default), the $I_{OCHARGE}$ bits are ignored and charge current is set to 200 mA.

See IOCHARGE *Register Bit Definitions*

Input Current Limiting (I_{BUSLIM})

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the I_{BUSLIM} (REG1[7:6]) bits.

For the FAN54053, no charging occurs automatically at V_{BUS} POR, so the input current limit is established by the I_{BUSLIM} bits.

See IBUSLIM *Register Bit Definitions*

Termination Limit (I_{TERM})

Charge current termination can be enabled or disabled using the TE (REG01h[3]) bit. By default TE = "0", therefore, termination is disabled and charging does not terminate at the programmed I_{TERM} level.

When TE = "1", and V_{BAT} reaches V_{OREG}, the charging current is reduced, limited by the battery's ESR and its internal cell voltage. When the charge current falls below I_{TERM}; PWM charging stops; but the STAT pin remains LOW. The STAT pin then goes HIGH and the STAT bits change to CHARGE DONE (10), provided the battery and charger are still connected. If V_{BAT} falls to V_{RCH} below V_{OREG}, the Fast Charge cycle starts again.

Post-charging can be enabled to "top-off" the battery to a lower termination current threshold than I_{TERM}. The PC_EN bit (REG07h[3]) must be set to "1" before the battery charging current reaches I_{TERM}. The lower termination current is set by the PC_IT (REG07h[2:0] bits. Post-charging begins after normal charging is ended (as described above) with the PC_ON (REG11h[2]) monitor bit set to "1".

During post-charging, the STAT pin is HIGH, indicating that the charge current is below the I_{TERM} level. Once the current reaches the threshold for post-charging completion (PC_IT), PWM charging stops and the PC_ON bit changes back to "0". If the charging current goes above I_{TERM} without first falling to PC_IT, the PC_ON bit can be reset by using any of these methods: V_{BAT} moving below and above V_{BATMIN}, a V_{BUS} POR, or the CE# or HZ_MODE bit cycled. If V_{BAT} falls to V_{RCH} below V_{OREG}, the Fast Charge cycle starts again.

See ITERM *Register Bit Definitions*

Weak Battery Voltage (V_{LOWV})

The FAN54053 monitors the level of the battery with respect to a programmable V_{LOWV} (REG01h<5:4>) threshold (default 3.7 V). The V_{LOWV} threshold defines the voltage level of the battery at which the system is guaranteed to be fully operational when only powered by the battery.

The POK_B pin pulls LOW once V_{BAT} reaches V_{LOWV}, and remains LOW as long as the IC is in Fast Charge. The IC will remain in Fast Charge as long as VBAT > 3.0 V.

See VLOWV *Register Bit Definitions*

VBUS Control loop (V_{BUSLIM})

The IC includes a control loop that limits input current in case a current-limited source is supplying V_{BUS}.

The control increases the charging current until either:

- I_{BUSLIM} or $I_{OCHARGE}$ is reached OR
- $V_{BUS} = V_{BUSLIM}$.

If V_{BUS} collapses to V_{BUSLIM}, the VBUS loop reduces its current to keep $V_{BUS} = V_{BUSLIM}$. When the VBUS control loop is limiting the charge current, the VLIM bit (REG05h[3]) is set.

See VBUSLIM *Register Bit Definitions*

Charger Operation

VBUS Plug In and Safety Timer

At VBUS plug in, the TMR_RST (Reg00h[7]) bit must be set within 2 seconds of V_{BUS} rising above $V_{(INMIN)1}$ or all registers, except for SAFETY (REG06h), are set to their default values. This functionality occurs regardless of the state of the CE# and WD_DIS bit. If plug in occurs with the device in a HZ or Charge Done state and the TMR_RST bit is not set within 2 seconds of V_{BUS} rising above $V_{(INMIN)1}$, all register, except for SAFETY, will reset when the device enters PWM Charging or Recharge.

By default, the safety timers do not run in the FAN54053. A Watchdog (t_{32s}) timer can be enabled by setting the WD_DIS register bit, (REG13h[1]) to "0". When WD_DIS = "0", charging is controlled by the host with the t_{32S} timer running to ensure that the host is alive. Setting the TMR_RST bit resets the t_{32S} timer. If the t_{32S} timer times out; all registers, except SAFETY, are set to their default values (including WD_DIS and CE#), the FAULT bits are set to "110", and STAT is pulsed.

V_{BUS} POR / Non-Compliant Charger Rejection

256 ms after VBUS is connected, the IC pulses the STAT pin and sets the VBUS_CON bit. Before starting to supply current, the IC applies a 110 Ω load from VBUS to GND. V_{BUS} must remain above $V_{IN(MIN)1}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (32 ms) before the IC initiates charging or supplies power to SYS.

The VBUS validation sequence always occurs before significant current is available to be drawn from VBUS (for example, after a VBUS OVP fault or a V_{RCH} (recharge initiation). t_{VBUS_VALID} ensures that unfiltered 50/60 Hz chargers and other non-compliant chargers are rejected.

USB-Friendly Boot Sequence

The FAN54053 does not automatically initiate charging at V_{BUS}POR. Instead, prior to receiving host commands, the buck is enabled to provide power to SYS while Q4 and Q5 remain off until register bit CE# (REG01[2]) is set to "0" through the I^2C interface, allowing charging through Q4.

Startup with No Battery

The FAN54053 has Battery Absent Behavior enabled. At V_{BUS} POR with the battery absent, the PWM will run, providing 3.55 V to the system from the input source with current limited by the default I_{BUSLIM} setting.

Startup with a Dead Battery

At V_{BUS} POR, if $V_{BAT} < V_{SHORT}$, all registers, including the SAFETY register, are reset to their default values and the DBAT_B (REG02h[1]) bit is reset. CE# = "1", so charging is disabled.

If the battery's protection switch is open, the PWM will run, providing 3.55 V to the system from the input source with current limited by the default I_{BUSLIM} setting. This allows the host processor to awaken and establish host control. Once this occurs, the host's low level software can program the CE# bit to "0" and a linear current source closes the battery protection switch. When V_{BAT} voltage rises above V_{SHORT} and sufficient power is available, PWM charging begins and the battery is charged through the BATFET, Q4. The IO_LEVEL (REG05h[5]) bit is set to "1" by default which limits charge current to 200 mA.

With CE# = "1" once V_{BAT} rises above V_{SHORT}, DBAT_B is set. With CE# = "0" once V_{BAT} rises above V_{BATMIN}, DBAT_B is set.

Power Path Operation

As long as $V_{BAT} < V_{BATMIN}$, Q4 operates as a linear current source, (Precharge) with its current (I_{PP}) limited to 200 mA when IO_LEVEL (REG05h[5]) is set to its default value of "1". If IO_LEVEL is set to "0" and I_{INLIM} > "01", charge current is limited to 450 mA when $I_{OCHARGE} \leq 750$ mA, and 730 mA when $I_{OCHARGE} > 750$ mA. Providing the input current is not limited by the I_{BUSLIM} setting or the current available from the source, during precharge, the IC regulates SYS to 3.55 V and provides the IO_LEVEL limited current to the battery.

System power always has the highest priority when power from the buck is limited ensuring SYS does not fall below 3.4 V. This is managed by folding back the current to charge the battery until charge current is reduced to 0 A.

After V_{BAT} reaches V_{BATMIN}, Q4 closes and is used as a current-sense element to limit current (I_{OCHRG}) per the I^2C register settings. This is accomplished by limiting the PWM modulator's current (Fast Charge). If SYS drops more than 5 mV (V_{THSYS}) below V_{BAT} and CE# = "0", Q4 and Q5 are turned on (GATE is pulled LOW). If CE# = "1", only Q5 is turned on. Once SYS voltage becomes higher than V_{BAT}, Q5 is turned off and Q4 again serves as the current-sense element to limit I_{OCHRG}.

If CE# = "1" and DIS pin is high or CE# = "1" and HZ_MODE = "1" while $V_{BAT} > V_{LOWV}$, so as to prevent the system from crashing, Q4 and Q5 are enabled. Q4 and Q5 are also both turned on when the IC enters SLEEP Mode ($V_{BUS} < V_{BAT}$).

POK_B (*see Table 4*)

The POK_B pin and POK_B (REG11h[5]) bit are intended to provide feedback to the baseband processor that the battery is strong enough to allow the device to fully function. Whenever the IC is operating in precharge, POK_B is HIGH. On exiting Precharge, POK_B remains HIGH until $V_{BAT} > V_{LOWV}$. REG01h[5:4] sets the V_{LOWV} threshold.POK_B pulls LOW once V_{BAT} reaches V_{LOWV}, and remains LOW as long as the IC is in Fast Charge and the IC will remain in Fast Charge as long as $V_{BAT} > 3.0$ V. If the battery voltage falls below 3.0 V the IC enters Precharge. If WD_DIS = "0" and the T_{32S} expires during charging, the POK_B pin will go high.

If the battery was above V_{LOWV} and has fallen below the level, the POK_B bit can be set to change the state of the pin to be high. This setting of the bit and pin can be used to signal the system into a low-power state, preventing excessive loading from the system while attempting to recharge a depleted battery.

The STAT pin pulses any time the POK_B pin changes.

Table 4. Q4, Q5, POK_B vs. Operating Mode

Operating Mode	V_{BUS}	V_{BAT}	CE#	PWM	V_{SYS}	Q4	Q5	GATE	POK_B
BUS Disconnected									
OFF	< $V_{BAT\ OR}$ < $V_{IN(MIN)2}$	> V_{SHORT}	X	OFF	≤ V_{BAT}	ON	ON	LOW	HIGH
VBUS Plug in with Battery Protection Switch Open									
PWM	Valid	OPEN	1	ON	V_{OREG}	OFF	OFF	HIGH	HIGH
			0						Indeterminate[8]
30 mA Linear Charging [9]	Valid	< V_{SHORT}	0	ON	3.55	OFF	OFF	HIGH	HIGH
Charge Mode									
Precharge	Valid	> V_{SHORT} and < V_{BATMIN}	0	ON	3.55	Linear	OFF	HIGH	HIGH
Precharge: $I_{SYS} + I_{pp} > I_{PWM}$, $I_{BAT} < I_{PP}$	Valid	< V_{BATMIN}	0	ON	< 3.55	Linear	OFF	HIGH	HIGH
Fast Charge	Valid	> V_{BATMIN} and < V_{LOWV}	0	ON	> V_{BAT}	ON	OFF	HIGH	HIGH
		> V_{LOWV}							LOW
Battery Voltage Falling from Fast Charge									
Precharge	Valid	$V_{BATFALL}$	0	ON	3.55	ON	OFF	HIGH	HIGH
Battery Supplementing SYS									
Supplemental Mode : $I_{SYS} > I_{PWM}$	Valid	> V_{SHORT}	1	ON	< V_{BAT}	X	ON	LOW	X
		> V_{BATMIN} and > V_{SYS} + V_{THSYS}	0	ON	< V_{BAT}	X	ON	LOW	X

Note:

8. When V_{BAT} is open it can float to V_{SYS}, and POK_B = HIGH when $V_{BAT} < V_{LOWV}$ and POK_B = LOW when $V_{BAT} > V_{LOWV}$.
9. 30 mA Linear Charging operating mode assumes the host has programmed CE# = "0" during PWM Operating Mode.

Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 5. STAT Pin Function

EN_STAT	Charge State	STAT Pin
0	X	OPEN
X	Normal Conditions	OPEN
1	Charging	LOW
X	Fault (Charging or Boost)	128 μs Pulse, then OPEN

The FAULT bits (REG00h[2:0]) indicate the type of fault in Charge Mode.

Monitor Registers (REG10h, REG11h)

Additional status monitoring bits enable the host processor to have more visibility into the status of the IC. The monitor bits are real-time status indicators and are not internally debounced or otherwise time qualified.

The state of the MONITOR register bits listed in High-Impedance Mode is valid only when V_{BUS} is valid.

Charge Mode Control Bits

The CE# (REG01h[2]) bit is set to "1' by default, therefore, charging is disabled.

Setting the RESET (REG04h[7]) bit clears all registers (except SAFETY). The CE# bit will only be cleared if RESET occurs with a valid VBUS and $V_{BAT} < V_{LOWV}$. If HZ_MODE or the WD_DIS bit was set when the RESET bit is set, this bit is also cleared. Refer to the Register Bit Definitions section for more details.

The HZ_MODE (REG01h[1]) and DIS pin will put the device in High-Impedance Mode. If HZ_MODE = "1" or DIS pin is HIGH, so as to prevent the system from crashing, Q4 and Q5 are enabled.

The functionality of the HZ_MODE (REG01h[1]) bit and DIS pin has a dependence upon V_{BAT} voltage level and the WD_DIS (REG13h[1]) bit state. Refer to Table 5 for details.

Table 6. DIS Pin, HZ_MODE and WD_DIS bits Operation

Conditions	Functionality
WD_DIS = 1 and $V_{BAT} > V_{LOWV}$	Setting either the HZ_MODE bit through I^2C or the DIS pin to HIGH will disable the charger and put the IC into High-Impedance Mode. Resetting the HZ_MODE bit or the DIS pin to LOW will allow charging to resume. While in High-Impedance mode, if V_{BAT} drops below V_{LOWV}, all registers (except SAFETY), including HZ_MODE and CE# are reset. Note that charge parameters will need to be reprogrammed in order to completely charge the battery.
WD_DIS = 1 and $V_{BAT} < V_{LOWV}$	Setting either the HZ_MODE bit through I^2C or the DIS pin to HIGH will reset all registers (except SAFETY), including HZ_MODE and CE#.
WD_DIS = 0 and $V_{BAT} > V_{LOWV}$	Setting either the HZ_MODE bit through I^2C or the DIS pin to HIGH will stop the t_{32S} timer from advancing (does not reset it), disable the charger, and put the IC into High-Impedance Mode. Resetting the HZ_MODE bit or the DIS pin to LOW will allow charging to resume.
WD_DIS = 0 and $V_{BAT} < V_{LOWV}$	Setting either the HZ_MODE bit through I^2C or the DIS pin to HIGH will disable the charger and put the IC into High-Impedance Mode. The T_{32S} timer will continue to run. If the T_{32S} timer is allowed to overflow, all registers (except SAFETY) are reset, including WD_DIS, HZ_MODE and CE#.

Flow Charts

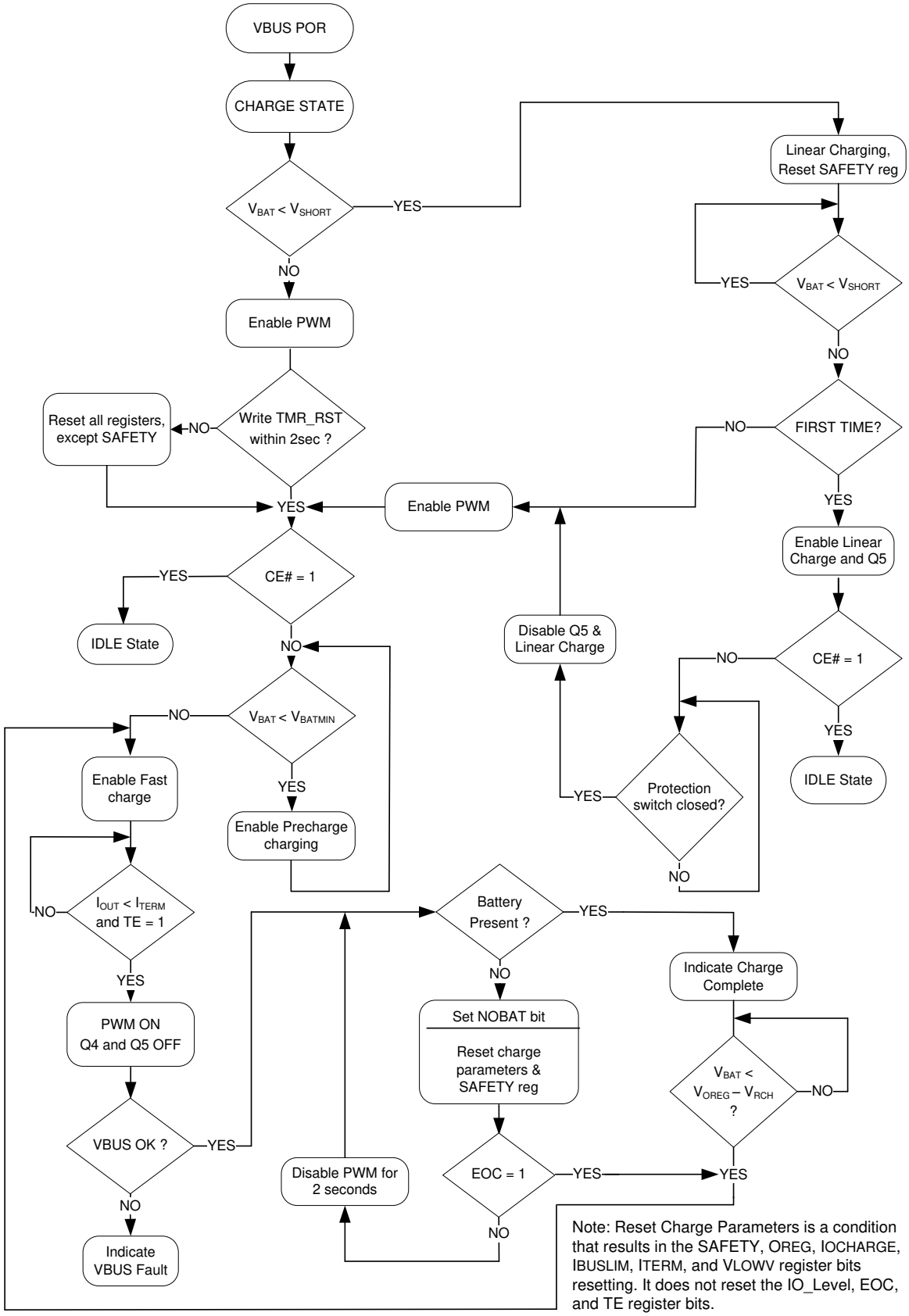


Figure 35. Charge State Flow Chart

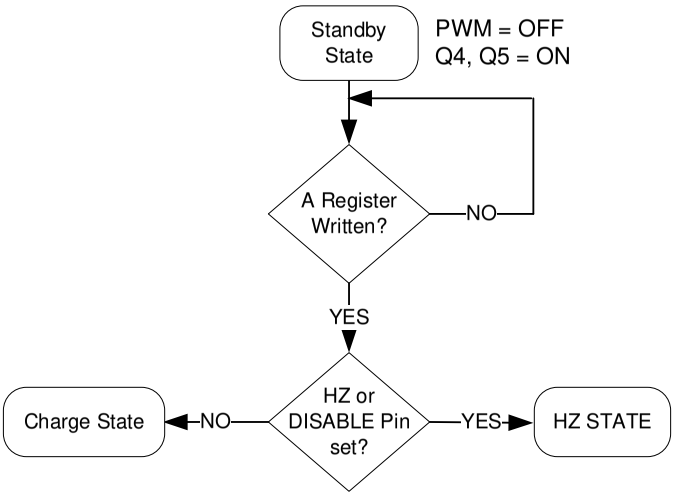


Figure 36. Standby State