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August 2013

FAN54300 — USB-Compliant, Dual-Power Input, Single-Cell, Li-Ion Switching Charger with USB-OTG Boost Regulator

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Accepts USB or Dedicated Power Input Source
- 5 V, 300 mA Boost Mode for USB OTG from 2.5 to 4.5 V Battery Input
- Charge Voltage Accuracy: ±0.5% at T_A=25°C
±1% from T_A=0 to 125°C
- ±5% USB Input Current Regulation Accuracy
- ±5% Charge Current Regulation Accuracy
- 20 V Absolute Maximum Input Voltage
- 9.5 V Maximum Input Operating Voltage on VIN Pin, 6.5 V Maximum on VBUS Pin
- Up to 1.5 A Maximum Charge Rate
- Programmable Charge and Mode through High-Speed I^2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Input Current
  - Fast-Charge / Termination Current
  - Charger Voltage
  - Safety Timer
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint, 1 µH, External Inductors
- Safety Timer with Reset Control
- Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum V_{BUS} Voltage
- Low Reverse Leakage from Battery Drain to VBUS or VIN
- Programmable LED Drive for Charge Indication
- Register and Slave Addresses Compatible with FAN540X and FAN542X Families

Description

The FAN54300 combines two highly integrated switch-mode chargers and a boost regulator to minimize single-cell Li-Ion charging time from a USB and/or auxiliary power source.

Charging parameters and operating modes are programmable through an I^2C Bus® interface that operates up to 3.4 Mbps. The charger and boost regulator circuits switch at 3 MHz to minimize the size of the external passive components.

The FAN54300 provides battery charging in three phases: conditioning, constant current, and constant voltage.

To ensure USB compliance and minimize charging time, the USB input current is limited to the value set through the I^2C host. Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I^2C host.

The IC automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode, with leakage from the battery to the input prevented. Charge status is reported back to the host through the I^2C port. Charge current is reduced when the die temperature reaches 120°C.

The FAN54300 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The FAN54300 is available in a 30-bump, 0.4 mm pitch, wafer-level, chip-scale package (WLCSP).

Applications

- Cell Phones, Smart Phones, PDAs
- Digital Cameras
- Portable Media Players

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN54300UCX	-40 to 85°C	30-Ball, WLCSP, 5x6 Array, 0.4mm Pitch, 586 µm Package Height	Tape and Reel

Table 1. Feature Summary

Part Number	Automatic Charge	Battery Absent Charge
FAN54300	Yes	No

Typical Application

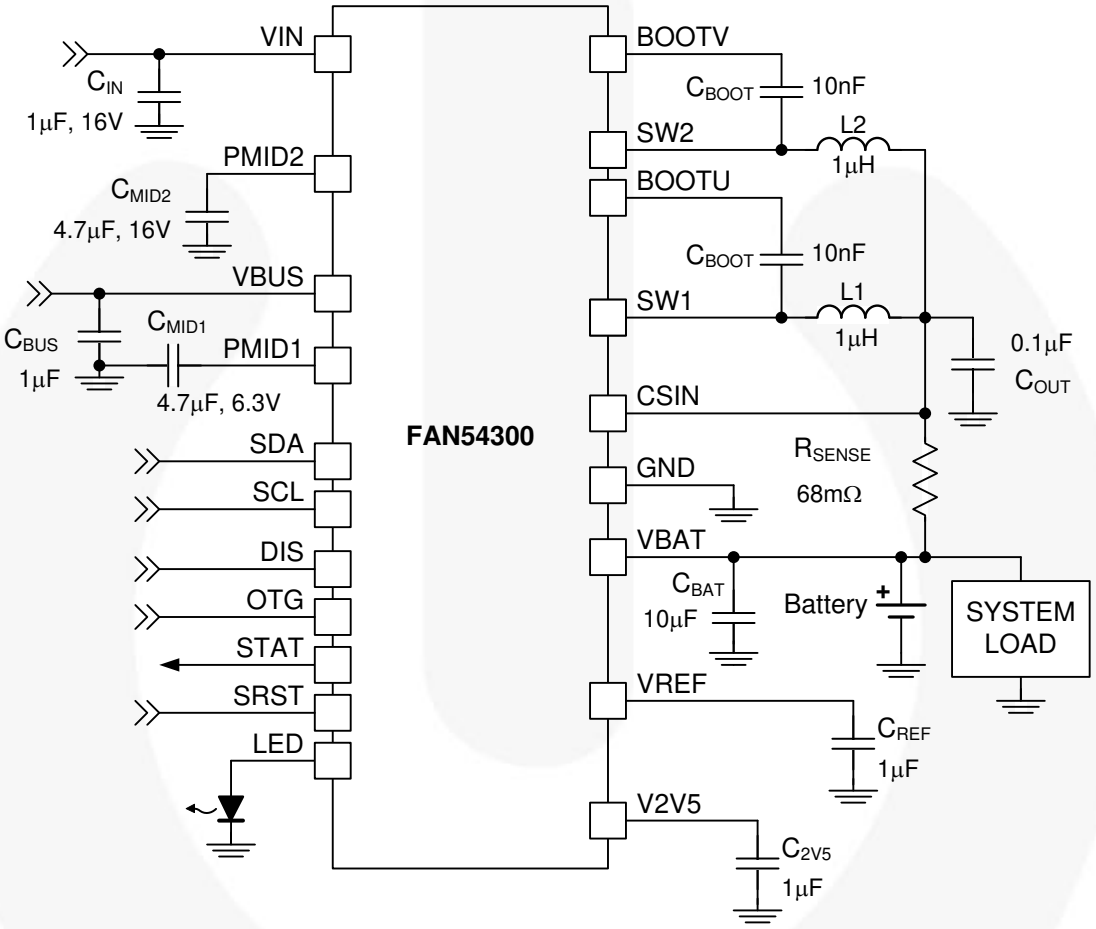


Figure 1. Typical Application

Block Diagrams

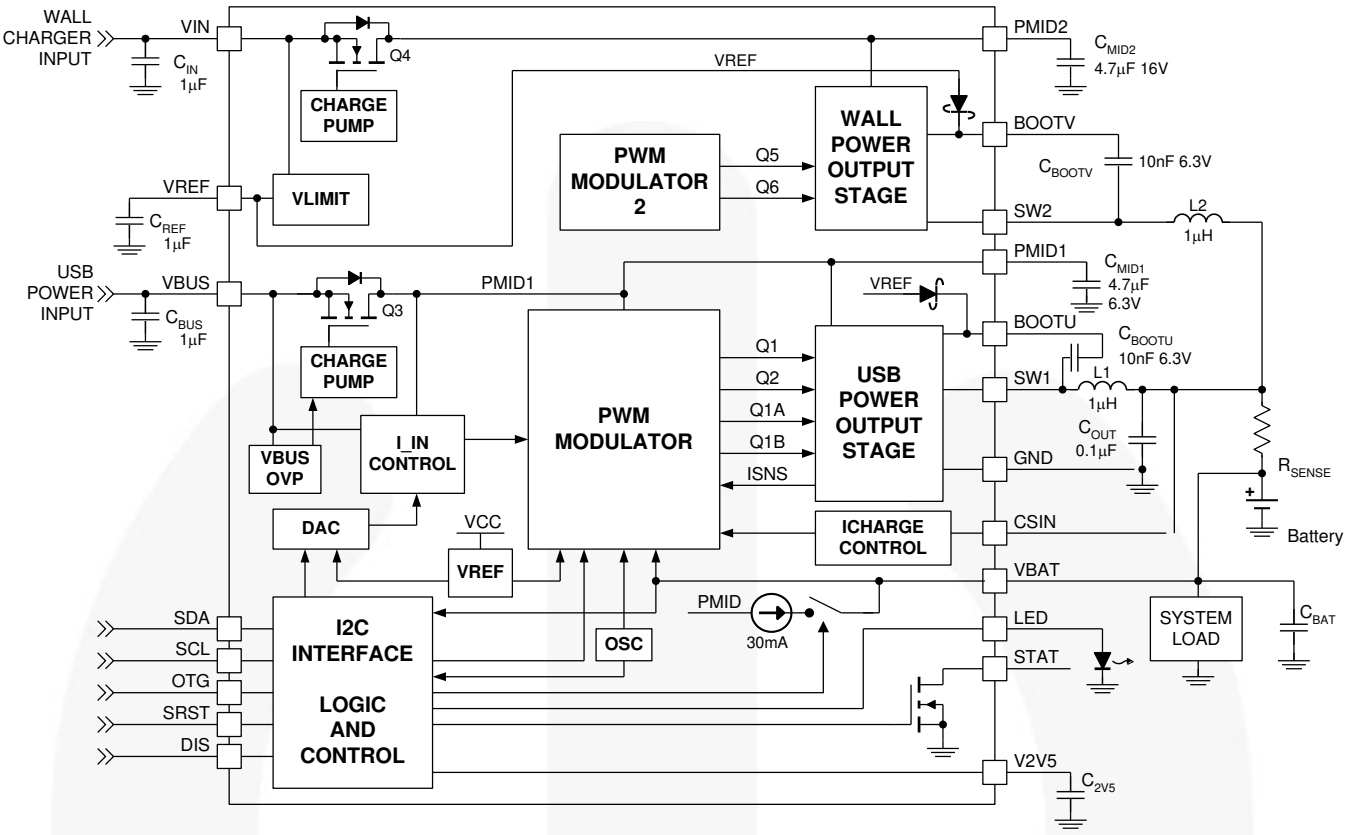


Figure 2. IC and System Block Diagram

Table 2. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Units
L1, L2:	Charge Currents to 1 A: 1 µH, 20%, 1.3 A, 2016	Murata: LQM2MPN1R0M	L	1.0	µH
			DCR	85	mΩ
	Charge Currents Above 1 A: 1 µH, 20%, 1.6 A, 2520	Murata: LQM2HPN1R0M	L	1.0	µH
			DCR	55	mΩ
C_{BAT}	10 µF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M	C	10	µF
$C_{MID1,2}$	4.7 µF, 10%, 16 V, X5R, 0805	Murata: GRM21BR61C475K	C	4.7	µF
C_{IN}, C_{BUS}	1.0 µF, 10%, 16 V, X5R, 0603	Murata GRM188R61E105K	C	1.0	µF
C_{BOOT}	10 nF, 10%, 6.3 V, X5R, 0201	Murata GRM033R70J103K	C	10	nF
C_{OUT}	0.1 µF, 10%, 6.3 V, X5R, 0201	Murata GRM033R60J104K	C	0.1	µF
C_{2V5}, C_{REF}	1µF, 10%, 6.3 V, X5R, 0402	Murata GRM155R60J105M	C	1.0	µF

Block Diagrams (Continued)

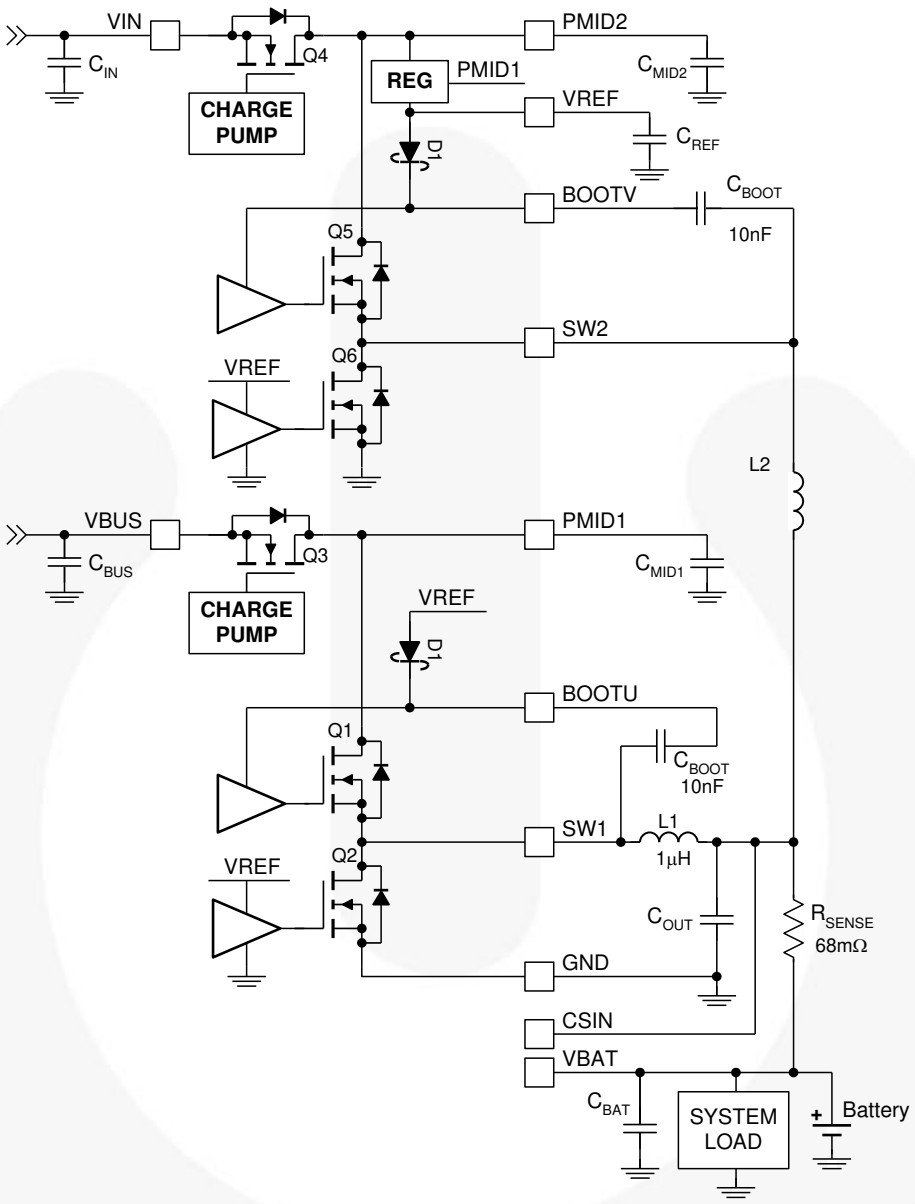


Figure 3. Power Output

Pin Configuration

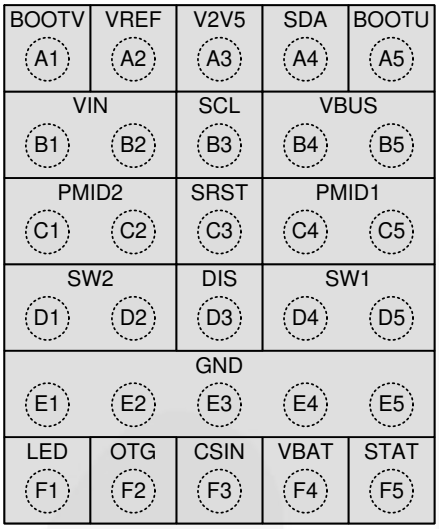


Figure 4. Pin Assignments (Top View)

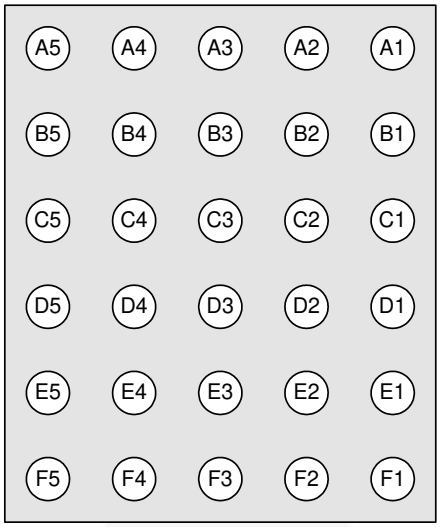


Figure 5. Pin Assignments (Bottom View)

Pin Definitions

Pin #	Name	Description
A1	BOOTV	**BOOT**. High-side NMOS driver supply. Connect a 10nF capacitor from SW2 to this pin.
A2	VREF	**Bias Regulator Output**. Connect to a 1 μF capacitor to PGND. This pin supplies the internal gate drive and power supply to the IC while charging. Up to 5 mA of current can be provided from this pin to drive external circuits. This pin is active when either V_{IN} or V_{BUS} are above V_{BAT}.
A3	V2V5	**2.5 V Regulator**. Connect to a 1 μF capacitor to PGND. Up to 5 mA can be provided from this pin to drive external circuits. This regulator is powered only when VIN is connected.
A4	SDA	**I^2C Interface Serial Data**. This pin should not be left floating.
A5	BOOTU	**BOOT**. High-side NMOS driver supply. Connect a 10 nF capacitor from SW1 to this pin.
B1, B2	VIN	**Charger Input Voltage**. Bypass with a minimum of 1 μF, 16 V capacitor to GND.
B3	SCL	**I^2C Interface Serial Clock**. This pin should not be left floating.
B4, B5	VBUS	**USB Input Voltage**. Bypass with a 1 μF, 16 V capacitor to GND.
C1, C2	PMID2	**Power Input Voltage for VIN Power Source**. Power input to the charger regulator, bypass point for the VIN input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 μF, 16 V capacitor to PGND.
C3	SRST	**Safety Reset**. When LOW, both safety registers are reset to their default values. When HIGH, the safety registers reset when V_{BAT} drops below V_{SHORT}.
C4, C5	PMID1	**Power Input Voltage for VBUS Power Source**. Power input to the VBUS switching charger regulator, bypass point for the VBUS input current sense, and high-voltage input switch. Bypass with a minimum of 4.7 μF, 6.3 V capacitor to PGND.
D1, D2	SW2	**Switching Node for VIN Charger**. Connect to the output inductor.
D3	DIS	**Charge Disable**. When this pin is HIGH, charging is disabled and no timers are reset. When LOW, charging is controlled by the I^2C registers. This pin does not affect the 32-second timer.
D4, D5	SW1	**Switching Node for VBUS Charger and OTG Boost**. Connect to the output inductor.
E1–E5	GND	**Ground**. Power return for gate drive and power transistors as well as IC signal ground. The connection from this pin to the bottoms of the C_{PMID} capacitors should be as short as possible.
F1	LED	**Light Emitting Diode Output**. Up to 5 mA current source drive from the active PMID indicates the battery is charging.

Pin #	Name	Description
F2	OTG	**On The Go**. When unattended charging is indicated, the level on this pin sets the I_{BUS} current limit. This pin is also used to put the IC into Boost Mode.
F3	CSIN	**Current-Sense Input**. Connect to sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 μF capacitor to PGND.
F4	VBAT	**Battery Voltage**. Connect to the positive (+) terminal of the battery pack. Bypass with a 10 μF capacitor to PGND.
F5	STAT	**Status**. Open-drain output indicating charge status. The IC pulls this pin LOW when charging is in process.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}	VBUS Voltage	Continuous	–1.4	20.0	V
		Pulsed, 100 ms Maximum Non-Repetitive	–2.0		
V_{IN}	VIN Voltage		–2.0	20.0	V
V_{BOOTU}	BOOTU Voltage		-0.7	20.0	V
V_{BOOTV}	BOOTV Voltage		-0.7	20.0	V
V_{PMID1}	PMID1 Voltage		–1.0	20.0	V
V_{SW1}	SW1 Voltage		–0.7	6.5	V
V_{PMID2}	PMID2 Voltage		–1.0	20.0	V
V_{SW2}	SW2 Voltage		–0.7	12.0	V
V_O	Other Pins		–0.3	6.5[1]	V
$\frac{dV_{BUS}}{dt}$	Maximum Rate of V_{BUS} Increase Above 5.5 V when IC Enabled			4	V/µs
$\frac{dV_{IN}}{dt}$	Maximum Rate of V_{IN} Increase Above 9.5 V when IC Enabled			4	V/µs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2.0		kV
		Charged Device Model per JESD22-C101	1.5		kV
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:

1. Lesser of 6.5 V or V_{REF} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{BUS}	VBUS Supply Voltage	4	6	V
V_{IN}	VIN Supply Voltage	4.0	9.5	V
T_A	Ambient Temperature	–30	+85	°C
T_J	Junction Temperature	0	+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	60	°C/W
θ_{JB}	Junction-to-PCB Thermal Resistance	20	°C/W

Electrical Specifications

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{BUS} or V_{IN} = 5.0 V, HZ1, HZ2, OPA_MODE = 0, (Charger Mode). SCL, SDA, OTG = 0 or 1.8 V. Typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
I_{VBUS}	VBUS Current	PWM Switching, Open Battery, TE=0		33		mA
		PWM Not Switching ($V_{BAT} > V_{OREG}$)		3.6		mA
		0°C < T_J < 85°C, HZ1 = 1, $V_{BAT} > V_{LOWV}$		350	500	µA
		0°C < T_J < 85°C, HZ1 = 1, $V_{BAT} < V_{LOWV}$, 32S Mode		350	500	µA
I_{VIN}	VIN Current	PWM Switching, Open Battery, TE=0		33		mA
		PWM Not Switching ($V_{BAT} > V_{OREG}$)		2.6		mA
		0°C < T_J < 85°C, HZ2 = 1, $V_{IN} > V_{LOWV}$		350	500	µA
		0°C < T_J < 85°C, HZ2 = 1, $V_{IN} < V_{LOWV}$, 32S Mode		350	500	µA
I_{BAT}	Battery Discharge Current in High-Z Mode	0°C < T_J < 85°C, HZ1=HZ2 = 1 or DIS=1, V_{BAT} = 4.2 V			20	µA
		0°C < T_J < 85°C, V_{BAT} = 4.2 V, V_{IN} = V_{BUS} = Open or GND, HZ1=HZ2=1, SDA = SCL = 1.8 V, No I^2C Traffic			30	µA
Charger Voltage Regulation						
V_{OREG}	Charge Voltage Range		3.5		4.4	V
	Charge Voltage Accuracy	T_A = 25°C	–0.5		+0.5	%
		T_J = 0 to 125°C	–1		+1	%
Charging Current Regulation						
I_{OCHRG}	Output Charge Current Range	$V_{LOWV} < V_{BAT} < V_{OREG}$, $V_{BUS} > V_{SLP}$, R_{SENSE} = 68 mΩ	550		1500	mA
	Charge Current Accuracy Across R_{SENSE}	20 mV ≤ V_{IREG} ≤ 40 mV	92	97	102	% of Setting
		V_{IREG} > 40 mV	94	97	100	
Weak-Battery Detection						
V_{LOWV}	Weak-Battery Threshold Accuracy	3.4 ≤ V_{LOWV} ≤ 3.7	-5		+5	%
	Weak Battery Deglitch Time	Rising Voltage, 2 mV Overdrive		30		ms
Logic Levels: DIS, SDA, SCL, OTG						
V_{IH}	HIGH-Level Input Voltage		1.05			V
V_{IL}	LOW-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{BAT}		0.01	1.00	µA
Charge Termination Detection						
$I_{(TERM)}$	Termination Current Range	$V_{BAT} > V_{OREG} – V_{RCH}$, $V_{BUS} > V_{SLP}$, R_{SENSE} = 68 mΩ	50		400	mA
	Termination Current Accuracy	[$V_{CSIN} – V_{BAT}$] from 3 mV to 20 mV	–25%		+25%	
		[$V_{CSIN} – V_{BAT}$] from 20 mV to 40 mV	–5%		+5%	
	Termination Current Deglitch Time	2 mV Overdrive		30		ms

Continued on the following page…

Electrical Specifications (Continued)

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{BUS} or V_{IN} = 5.0 V, HZ1, HZ2, OPA_MODE = 0, (Charger Mode). SCL, SDA, OTG = 0 or 1.8V. Typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VBUS Input Power Source Detection						
$V_{BUS(MIN)1}$	V_{BUS} Input Voltage Rising	To Start V_{BUS} Validation	4.20	4.30	4.40	V
$V_{BUS(MIN)2}$	Min. V_{BUS} to Pass Validation	During V_{BUS} Validation Period	4.00	4.08	4.15	V
$V_{BUS(MIN)3}$	Min. V_{BUS} During Charge	During Charging	3.64	3.71	3.78	V
t_{VBUS_VALID}	V_{BUS} Validation Time			30		ms
$VBUS_{LOAD}$	V_{BUS} Load	V_{BUS} = 5 V, Applied at V_{BUS} Validation		50		mA
VIN Input Power Source Detection						
$V_{IN(MIN)1}$	V_{IN} Input Voltage Rising	To Start V_{IN} Validation	4.20	4.30	4.40	V
$V_{IN(MIN)2}$	Min. V_{IN} to Pass Validation	During V_{IN} Validation Period	4.00	4.08	4.15	V
$V_{IN(MIN)3}$	Min. V_{IN} During Charge	During Charging	3.64	3.71	3.78	V
t_{VBUS_VALID}	V_{IN} Validation Time			30		ms
VIN_{LOAD}	V_{IN} Load	V_{IN} = 5 V, Applied at V_{IN} Validation		50		mA
Input Current Limit						
I_{BUSLIM}	VBUS Input Current-Limit Threshold	I_{BUS} set to 100 mA	88	93	98	mA
		I_{BUS} set to 500 mA	450	475	500	
V_{2V5} 2.5V Linear Regulator						
V_{2V5}	2.5 V Regulator Output	I_{2V5} from 0 to 5 mA, V_{IN} > 4.75 V	2.35	2.50	2.65	V
	Current Limit		6	8		mA
V_{REF} Bias Generator						
V_{REF}	Bias regulator voltage	$V_{IN} > V_{IN(MIN)}$	3.5		6.0	V
	current limit		10	15		mA
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below $V_{(OREG)}$	100	120	150	mV
	Deglitch Time	VBAT falling below V_{RCH} threshold		130		ms
STAT Output						
$V_{STAT(OL)}$	STAT Output LOW	I_{STAT} = 10 mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT} = 5 V			1	µA
LED Output						
$I_{LED(ON)}$	LED Output Current Accuracy	V_{LED} from 1.5 to 3.5 V, Max. (V_{REF},V_{BAT}) – V_{LED} > 100 mV	–30		+30	%
$I_{LED(OFF)}$	LED Off-State Leakage Current	V_{LED} = 0 V			1	µA
Battery Detection						
I_{DETECT}	Battery Detection Current Before Charge Complete (Sink Current)[2]	Begins After Termination Detected and $V_{BAT} \le V_{OREG} - V_{RCH}$		–0.45		mA
t_{DETECT}	Battery Detection time			262		ms

Continued on the following page…

Electrical Specifications (Continued)

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{BUS} or V_{IN} = 5.0 V, HZ1, HZ2, OPA_MODE = 0, (Charger Mode). SCL, SDA, OTG = 0 or 1.8 V. Typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Sleep Comparator						
V_{SLP}	Sleep Mode Entry Threshold, $V_{BUS} - V_{BAT}$ or $V_{IN} - V_{BAT}$	2.3 V ≤ V_{BAT} ≤ V_{OREG}, V_{PWRIN} Falling	0	90	160	mV
V_{SLP_EXIT}	Sleep Mode Exit Hysteresis	2.3 V ≤ V_{BAT} ≤ V_{OREG}		40		mV
	Deglitch Time for V_{BUS} Rising Above V_{SLP} + V_{SLP_EXIT}	Rising Voltage		30		ms
Power Switches *(see Figure 3)*						
$R_{DS(ON)}$	Q3 On Resistance (VBUS to PMID1)	$IBUS_{(LIMIT)}$ ≥ 500 mA		210	300	mΩ
	Q1 On Resistance (PMID1 to SW1)			110	225	
	Q2 On Resistance (SW1 to GND)			130	225	
	Q4 On Resistance (VIN to PMID2)			160	225	
	Q5 On Resistance (PMID2 to SW2)			110	225	
	Q6 On Resistance (SW2 to GND)			190	350	
Charger PWM Modulator						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				100	%
D_{MIN}	Minimum Duty Cycle			0		%
I_{SYNC}	Synchronous to Non-Synchronous Current Threshold(3)	Low-Side MOSFET Cycle-by-Cycle Current Limit		-120		mA
Boost Mode Operation (OPA_MODE = 1, HZ1 = 0)						
V_{BOOST}	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V, 0-200 mA Load	4.80	5.05	5.17	V
		2.7 V < V_{BAT} < 4.5 V, 0-300 mA Load	4.77	5.05	5.17	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	PFM Mode, V_{IN} = 3.6 V, I_{OUT} = 0		300	400	µA
$I_{LIMPK(BST)}$	Q2-Peak Current Limit		1160	1380	1550	mA
$V_{BAT(MAX)}$	Maximum Battery Input for Boost Operation	V_{BAT} Rising	4.7			V
	Hysteresis	V_{BAT} Falling		125		mV
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.42		V
		To Start Boost Regulator		2.58	2.70	
VBUS, VIN Load Resistance						
R_{VBUS}	VBUS to GND Resistance	Normal Operation	500	1000	1500	Ω
		V_{BUS} Validation	50	110	175	Ω
R_{VIN}	VIN to GND Resistance	Normal Operation	500	1000	1500	Ω
		V_{IN} Validation	50	110	175	Ω

Continued on the following page…

Electrical Specifications (Continued)

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{BUS} or V_{IN} = 5.0 V, HZ1, HZ2, OPA_MODE = 0, (Charger Mode). SCL, SDA, OTG = 0 or 1.8 V. Typical values are for T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Protection and Timers						
$VBUS_{OVP}$	VBUS Over-Voltage Shutdown	V_{BUS} Rising	6.12	6.31	6.50	V
	Hysteresis	V_{BUS} Falling		100		mV
VIN_{OVP}	VIN Over-Voltage Shutdown	V_{IN} Rising	9.5	10.0	10.5	V
	Hysteresis	V_{IN} Falling		100		mV
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	2.00	2.05	2.10	V
	Hysteresis	V_{BAT} Falling		100		
I_{SHORT}	Short-Circuit Current	$V_{BAT} < V_{SHORT}$	30	40	50	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold[4]	T_J Rising		165		°C
	Hysteresis[4]	T_J Falling		10		
T_{CF}	Thermal Regulation Threshold[4]	Charge Current Reduction Begins		120		°C
t_{INT}	Detection Interval			2.1		s
t_{32SEC}	32-Second Timer[5]	32-Second Mode	21.0		31.5	s
t_{15MIN}	15-Minute Timer	15-Minute Mode	12.0	13.5	15.0	min
Δt_{LF}	Low Frequency Timer Accuracy	Charger Inactive	–25		25	%

Notes:

2. Refers to negative inductor current. At lower battery charging current, of about 20 mA, non-synchronous switching operation commences.
3. Q2 and Q6 always turn on for »60 ns and then turn off if the current is below I_{SYNC}.
4. Guaranteed by design.
5. This tolerance applies to all timers on the IC, including soft-start and deglitching timers.

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, $C_B \leq 100$ pF			3400	
		High-Speed Mode, $C_B \leq 400$ pF			1700	
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		High-Speed Mode, $C_B \leq 100$ pF		160		ns
		High-Speed Mode, $C_B \leq 400$ pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \leq 100$ pF		60		ns
		High-Speed Mode, $C_B \leq 400$ pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \leq 100$ pF	0		70	ns
		High-Speed Mode, $C_B \leq 400$ pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	40	
		High-Speed Mode, $C_B \leq 400$ pF		20	80	
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	

Continued on the following page…

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{FDA}	SDA Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		High-Speed Mode, $C_B \leq 100$ pF		10	80	
		High-Speed Mode, $C_B \leq 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA, SCL				400	pF

Timing Diagrams

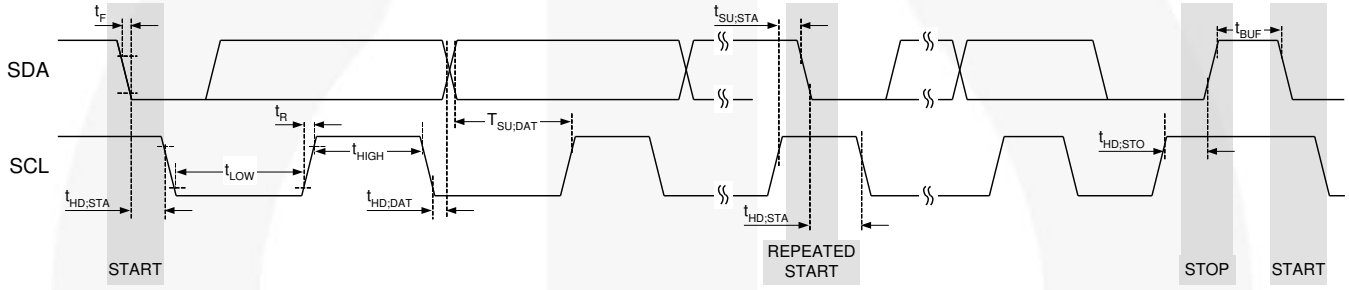
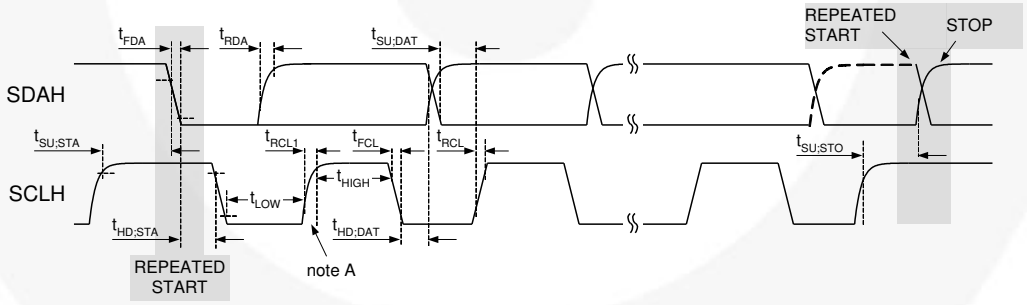


Figure 6. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 7. I²C Interface Timing for High-Speed Mode

VBUS Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

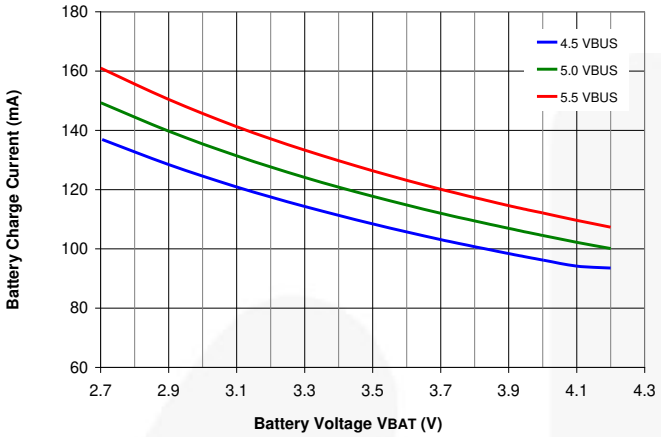


Figure 8. Battery Charge Current vs. V_{BUS} with I_{INLIM}=100 mA

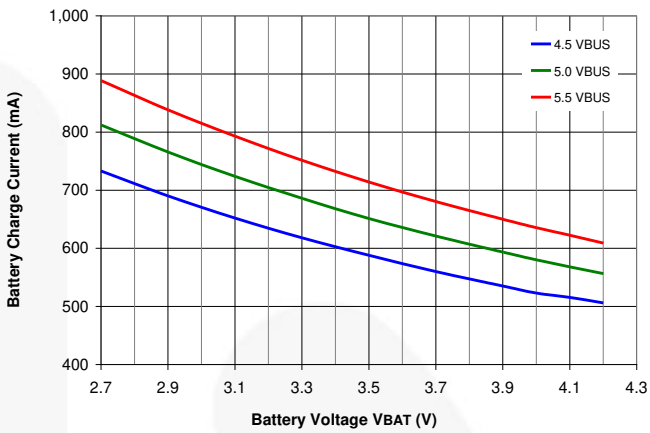


Figure 9. Battery Charge Current vs. V_{BUS} with I_{INLIM}=500 mA

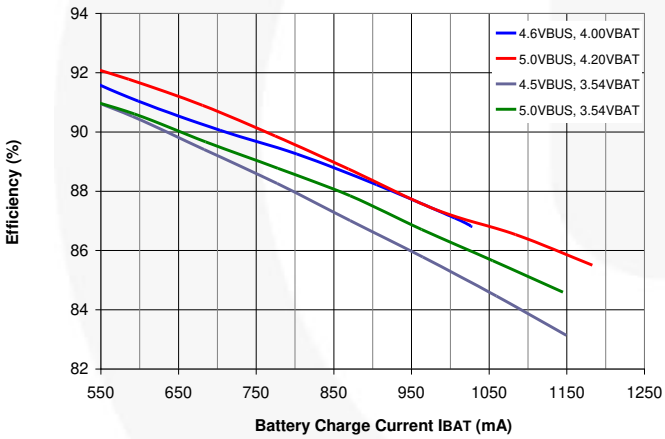


Figure 10. Charger Efficiency, No I_{INLIM}, $I_{OCHARGE}$=1250 mA

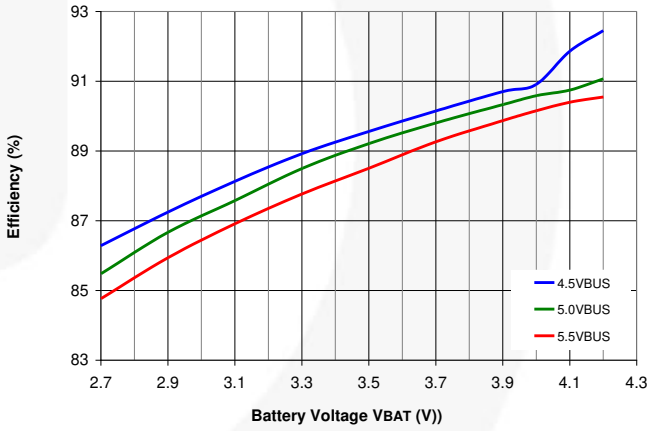


Figure 11. Charger Efficiency vs. V_{BUS}, I_{INLIM}=500 mA

VBUS Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

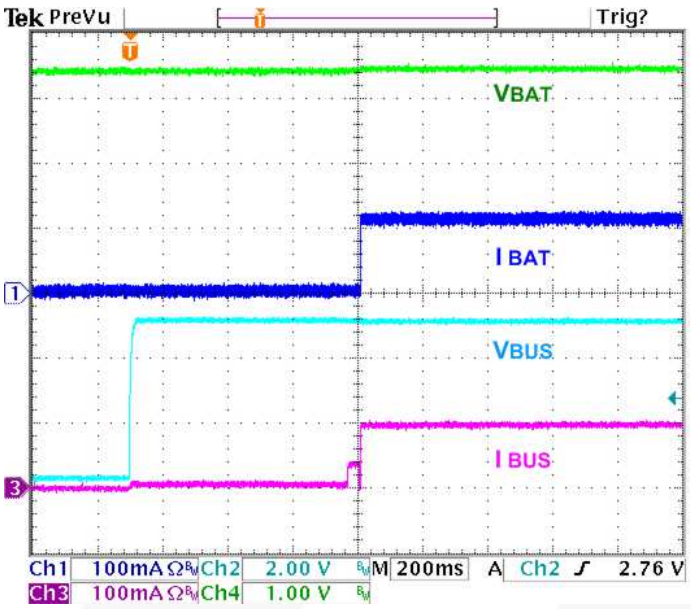


Figure 12. Auto-Charge Startup at V_{BUS} Plug-in, I_{INLIM}=100 mA, OTG=1, V_{BAT}=3.4 V

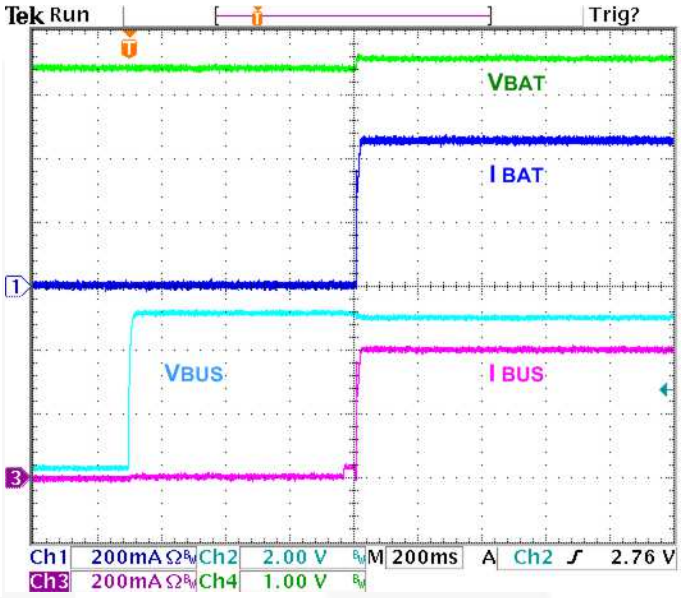


Figure 13. Auto-Charge Startup at V_{BUS} Plug-in, I_{INLIM}=500 mA, OTG=1, V_{BAT}=3.4 V

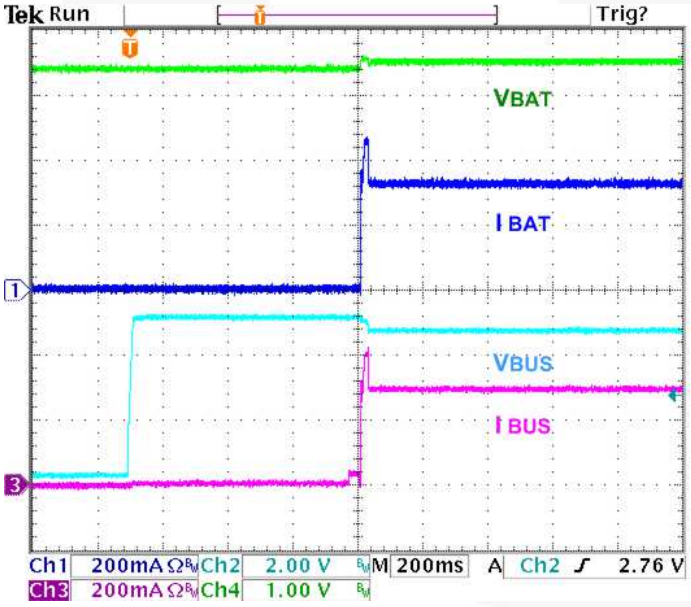


Figure 14. AutoCharge Startup with 300 mA Limited Charger / Adaptor, I_{INLIM}=500 mA, OTG=1, V_{BAT}=3.4 V

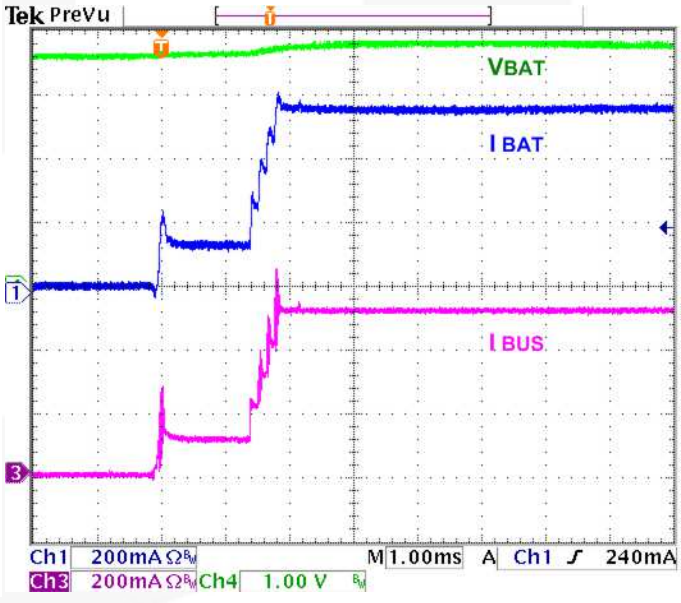


Figure 15. Charger Startup with HZ_MODE Bit Reset, I_{INLIM}=500 mA, $I_{OCHARGE}$=950 mA, V_{OREG}=4.2 V, V_{BAT}=3.6 V

VBUS Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.2 V, V_{BUS}=5.0 V, and T_A=25°C.

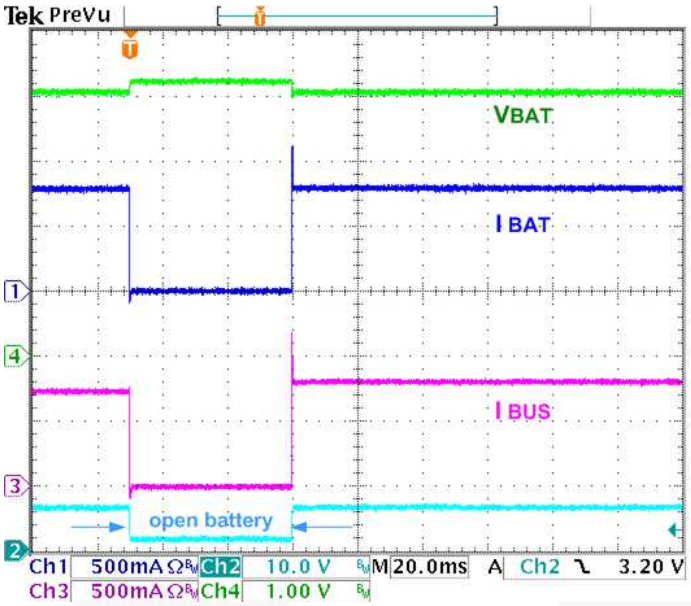


Figure 16. Battery Removal / Insertion during Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=950 mA, No I_{INLIM}, TE=0

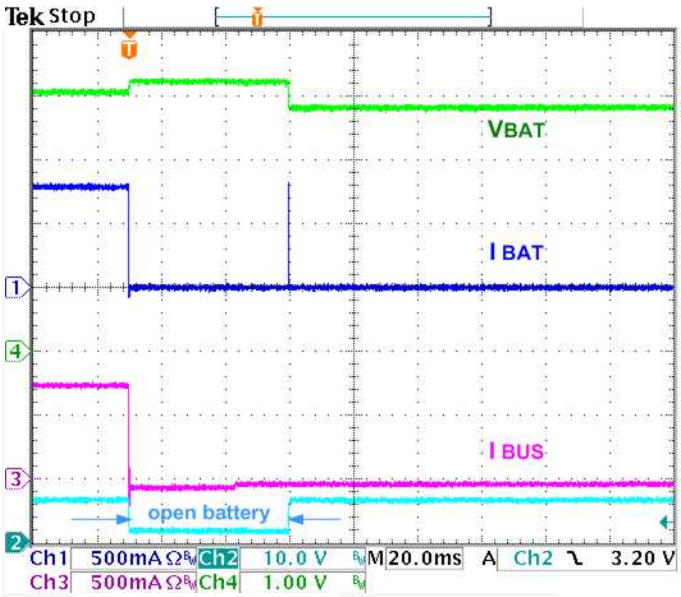


Figure 17. Battery Removal / Insertion during Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=950 mA, No I_{INLIM}, TE=1

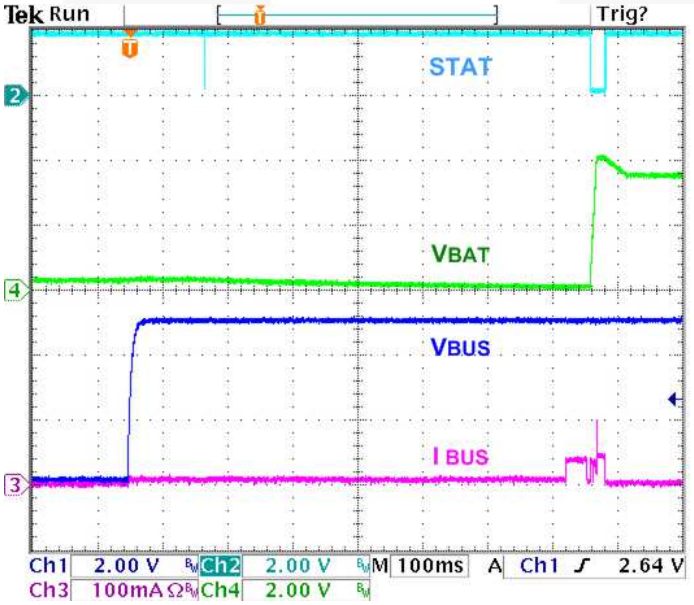


Figure 18. No Battery at V_{BUS} Power-up

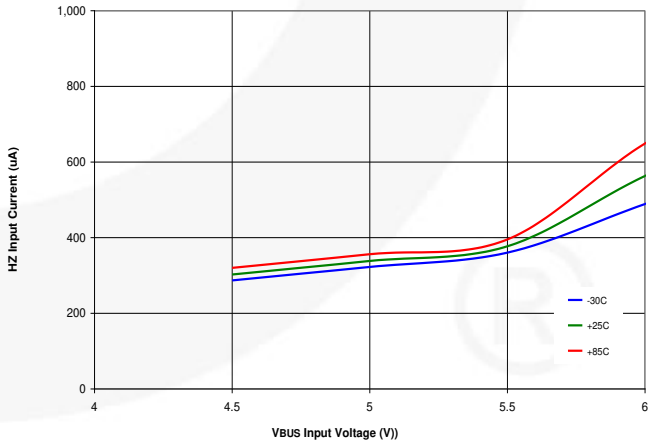


Figure 19. VBUS Current in High-Impedance Mode with Battery Open

VIN Charger Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.2 V, V_{IN} = 5.0 V, and T_A=25°C.

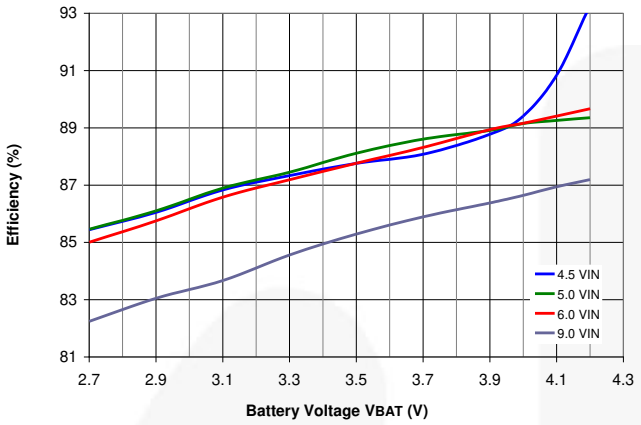


Figure 20. Charger Efficiency, $I_{OCHARGE}$=950 mA

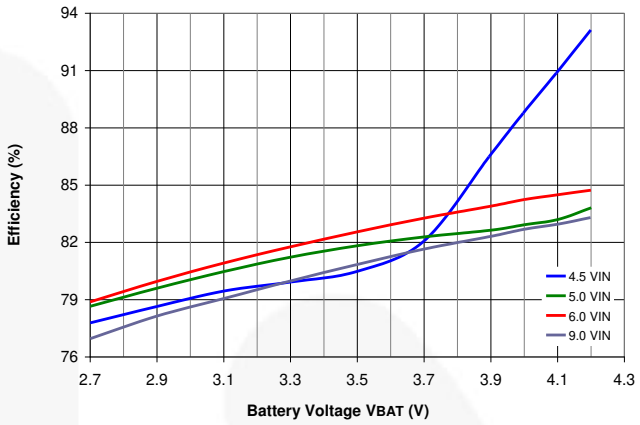


Figure 21. Charger Efficiency, $I_{OCHARGE}$=1550 mA

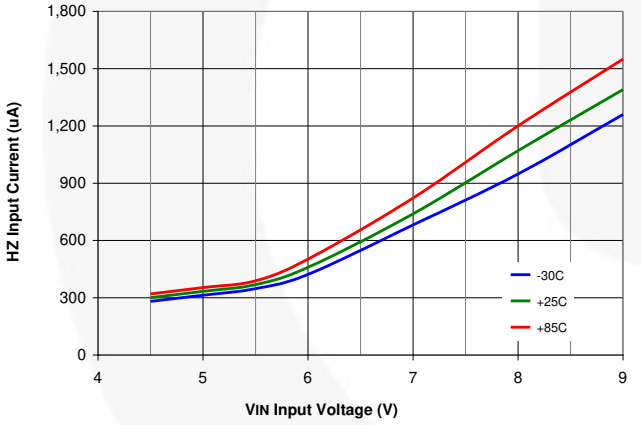


Figure 22. V_{IN} Current in High-Impedance Mode, V_{BAT}=3.6 V

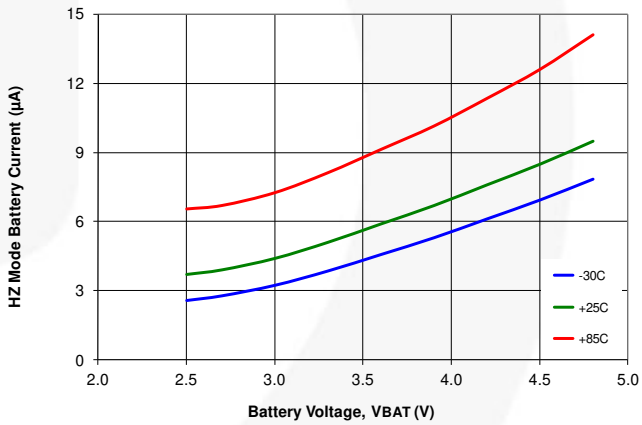


Figure 23. Battery Current in High-Impedance Mode, VBUS=Open, V_{IN}=Open

VIN Charger Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.2 V, V_{IN} = 5.0 V, and T_A=25°C.

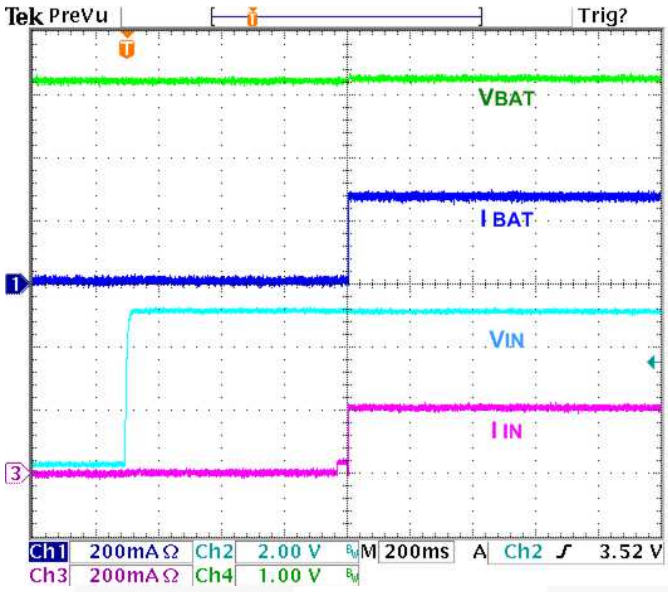


Figure 24. Auto-Charge Startup at V_{IN} Plug-in, V_{BAT}=3.2 V, IO_LEVELV = 1

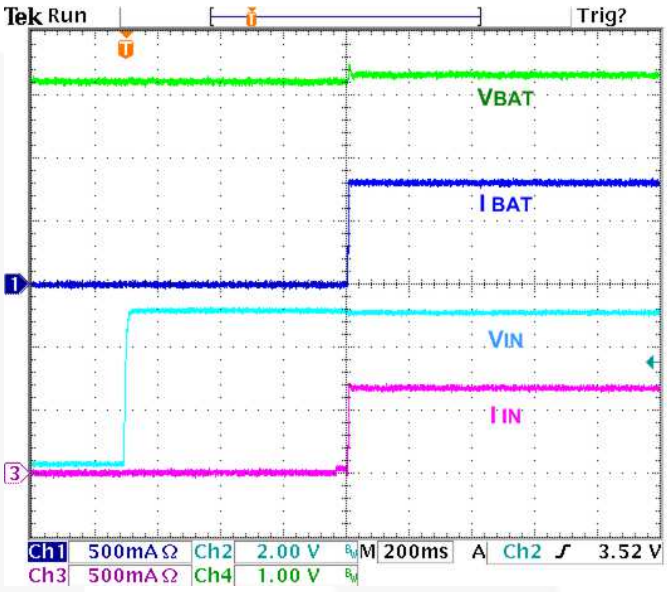


Figure 25. Auto-Charge Startup at V_{IN} Plug-in, V_{BAT}=3.2 V, $I_{OCHARGE}$=950 mA

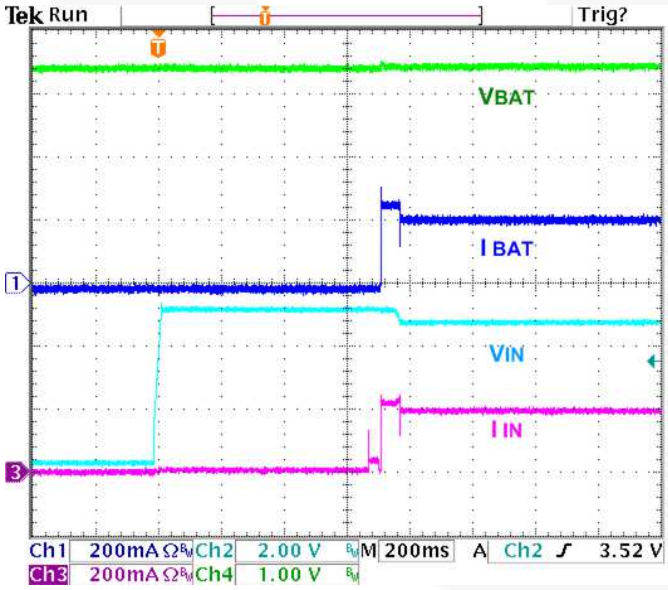


Figure 26. Auto-Charge Startup with 200 mA Limited Charger / Adaptor, V_{BAT}=3.4 V

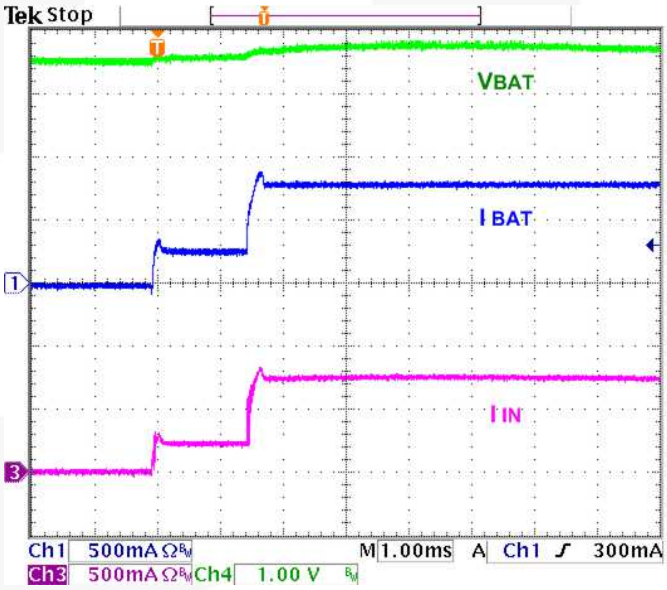


Figure 27. Charger Startup with HZ_MODE Bit Reset, $I_{OCHARGE}$=950 mA, V_{OREG}=4.2 V, V_{BAT}=3.6 V

VIN Charger Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.2 V, V_{IN} = 5.0 V, and T_A=25°C.

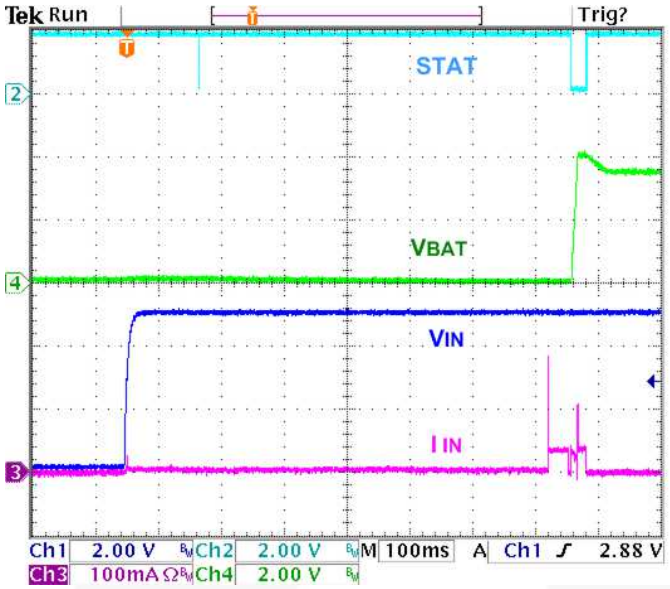


Figure 28. No Battery at V_{IN} Power-up

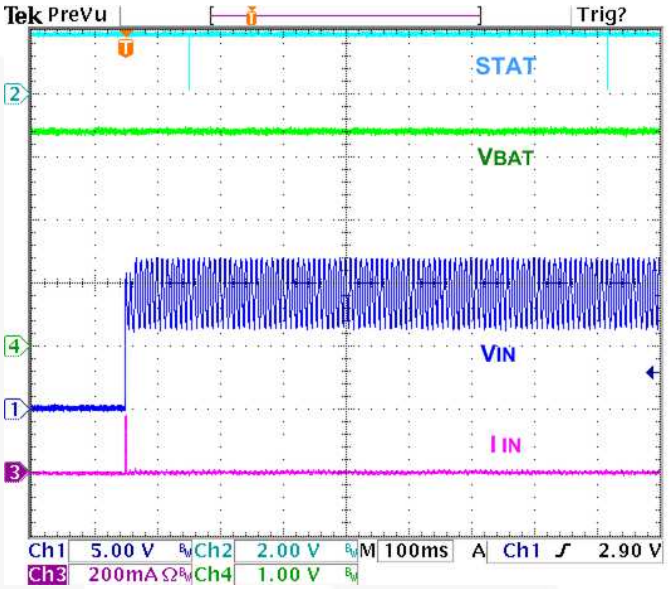


Figure 29. Non-Compliant Charger Rejection, V_{BAT}=3.4 V

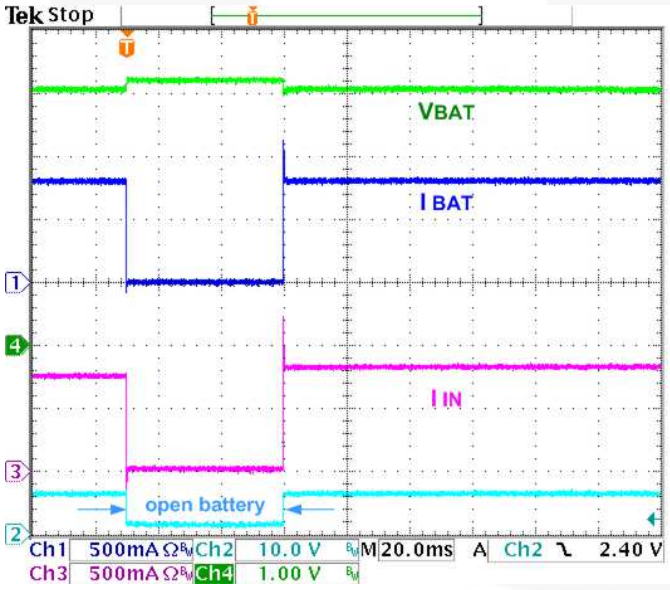


Figure 30. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=950 mA, TE=0

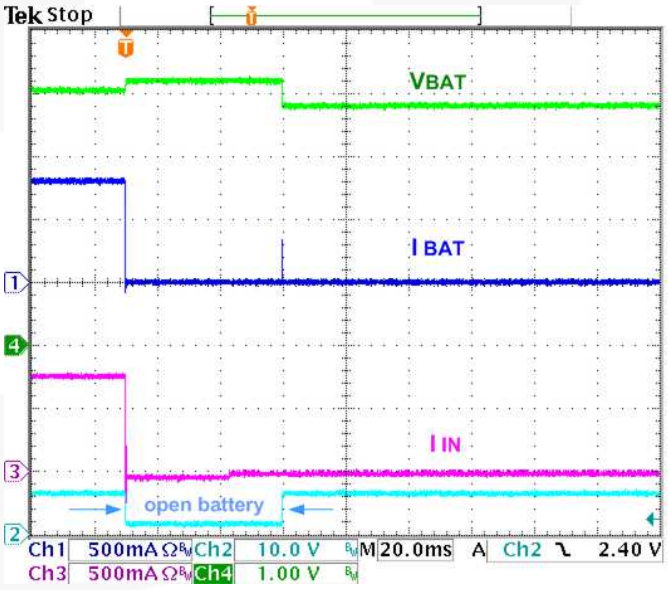


Figure 31. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=950 mA, TE=1

Boost Mode Typical Characteristics

Unless otherwise specified, using the circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

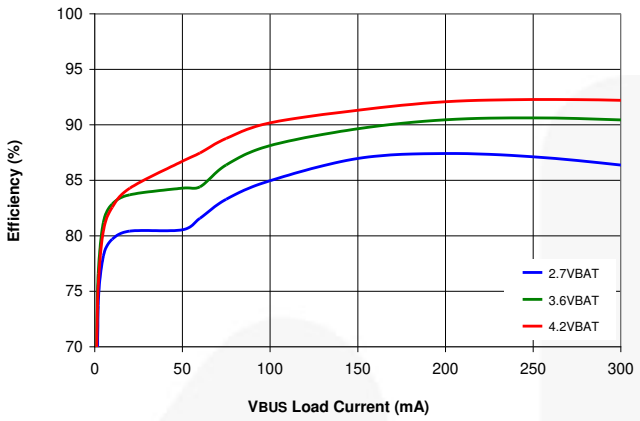


Figure 32. Efficiency vs. V_{BAT}

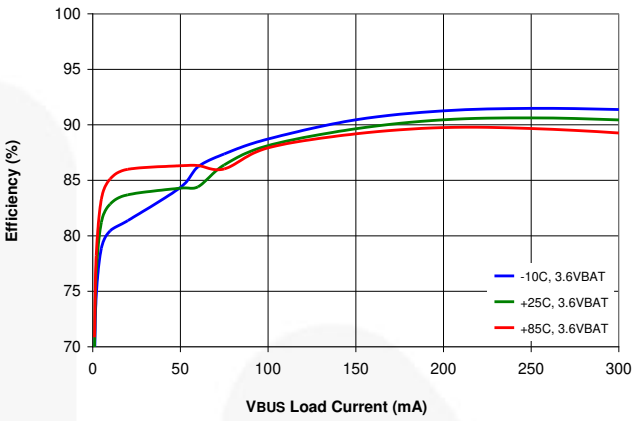


Figure 33. Efficiency Over Temperature

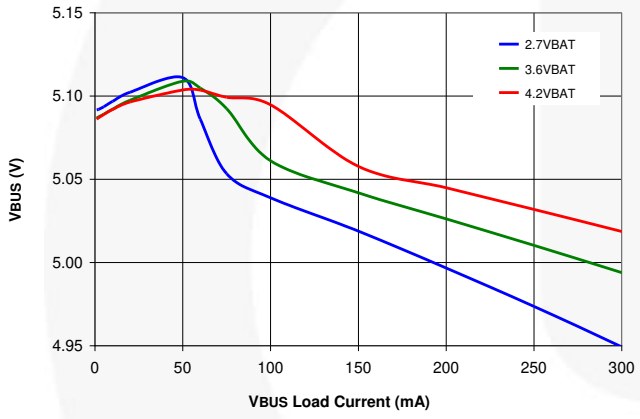


Figure 34. Output Regulation vs. V_{BAT}

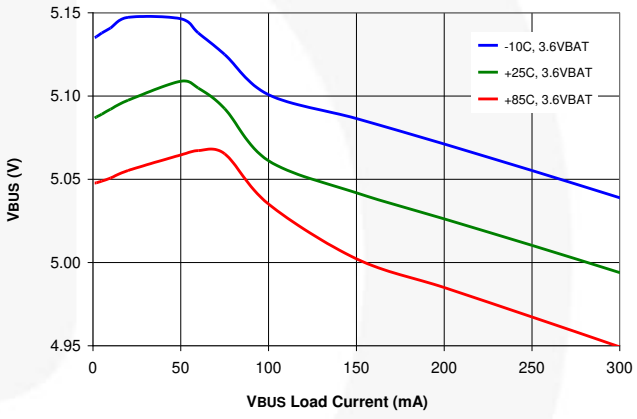


Figure 35. Output Regulation Over Temperature

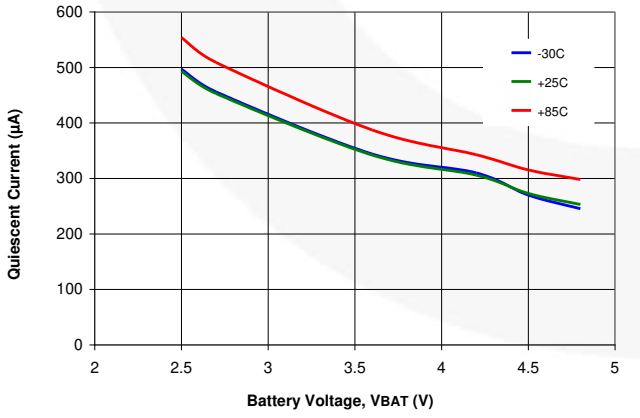


Figure 36. Quiescent Current

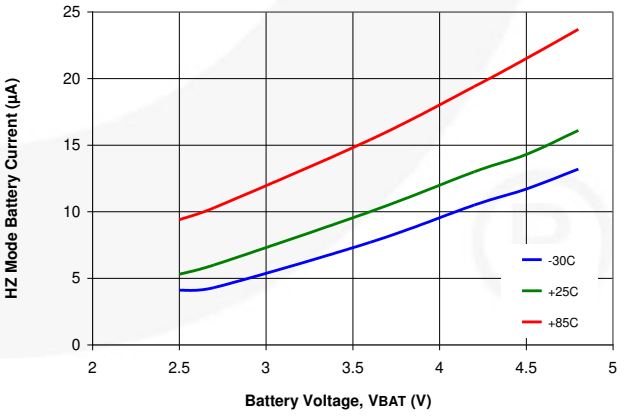


Figure 37. High-Impedance Mode Battery Current

Boost Mode Typical Characteristics

Unless otherwise specified, using the circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

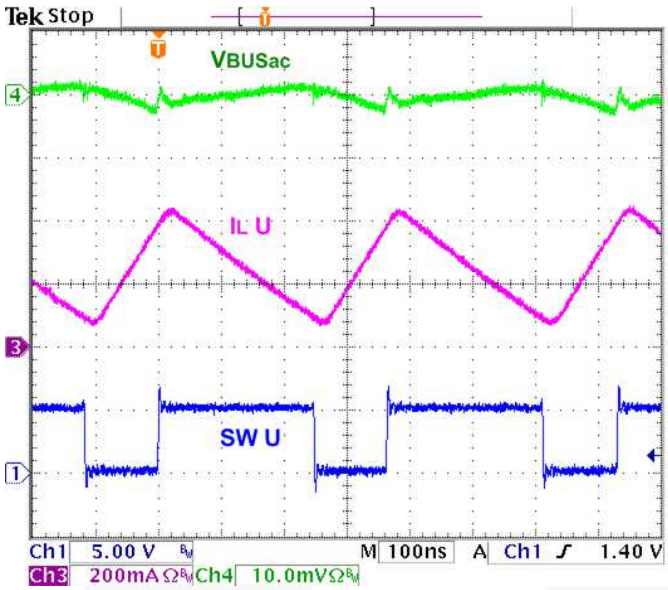


Figure 38. Boost PWM Waveform

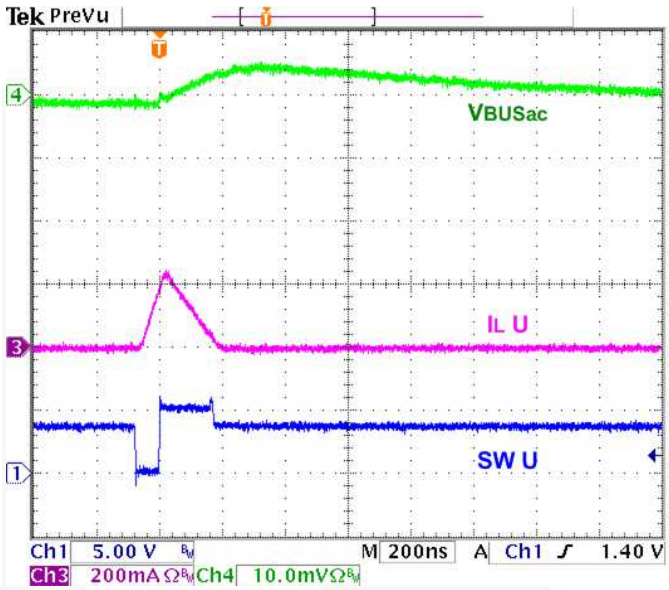


Figure 39. Boost PFM Waveform

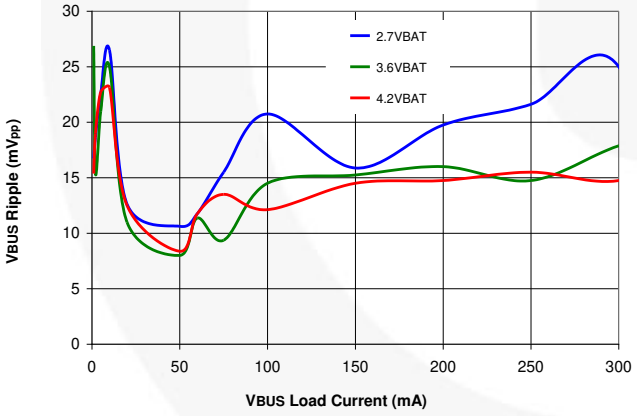


Figure 40. Output Ripple vs. V_{BAT}

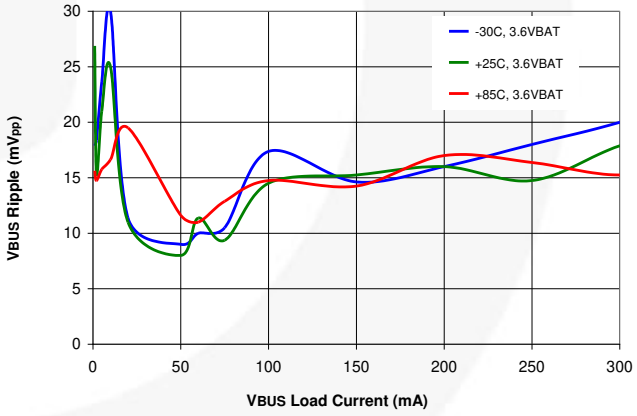


Figure 41. Output Ripple vs. Temperature

Boost Mode Typical Characteristics

Unless otherwise specified, using the circuit of Figure 1, V_{BAT}=3.6 V, T_A=25°C.

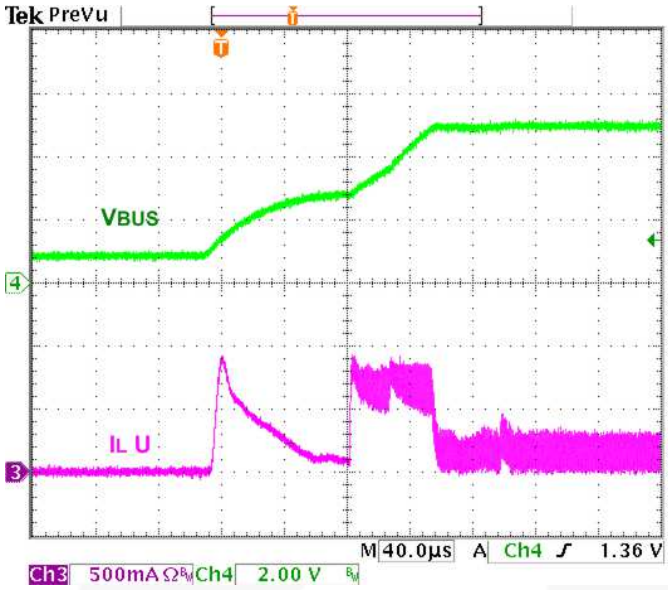


Figure 42. Startup, 3.6 V_{BAT}, 50 Ω Load, Additional 10 µF, X5R Across VBUS

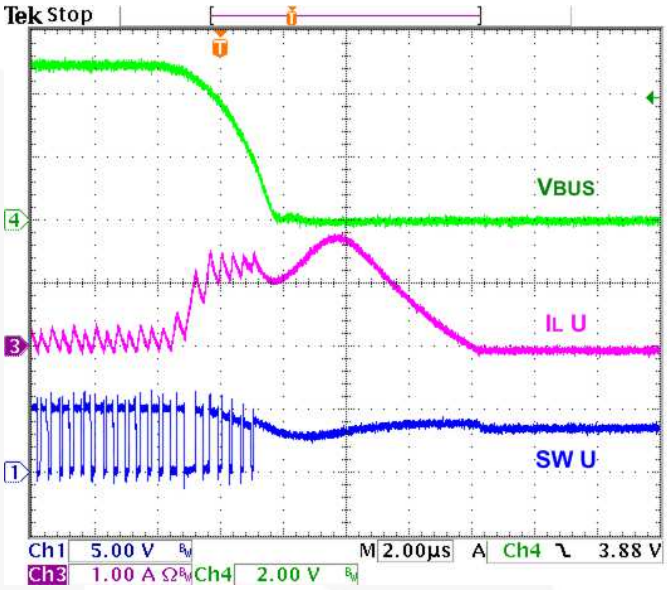


Figure 43. V_{BUS} Fault Response, 3.6 V_{BAT}

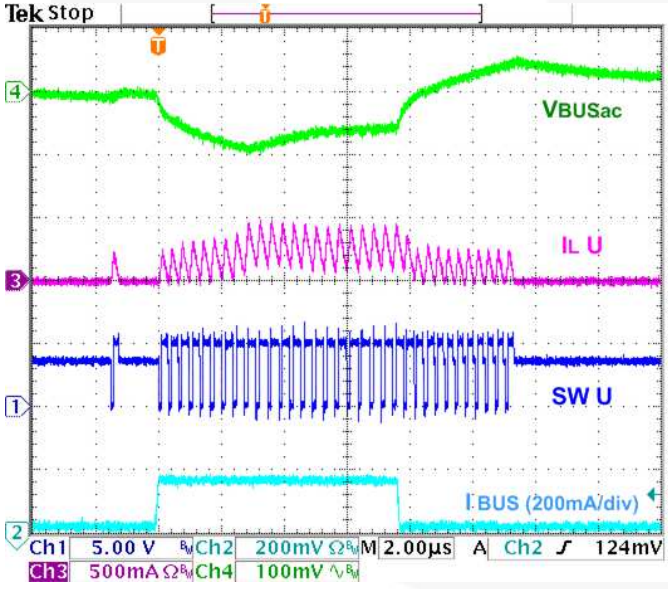


Figure 44. Load Transient, 5-155-5 mA, t_R=t_F=100 ns

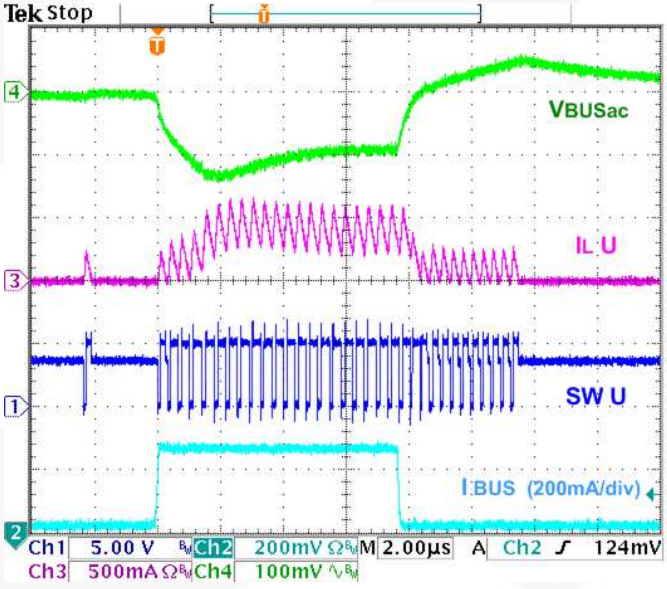


Figure 45. Load Transient, 5-255-5 mA, t_R=t_F=100 ns

Circuit Description / Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

The FAN54300 combines two highly integrated synchronous buck regulators for charging from two separate power sources. The IC also includes a synchronous boost regulator, which can supply 5 V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

In addition to its USB (VBUS) input, the FAN54300 allows a second power source (VIN) to be used for charging. This input source is typically a "wall wart" and can be up to 9.5 V input.

The FAN54300 has three operating modes:

- **Charge Mode**:
  Charges a single-cell Li-Ion or Li-polymer battery.
- **Boost Mode**:
  Provides 5 V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.
- **High-Impedance Mode**:
  Both the boost and charging circuits are off in this mode. Current flow from PWRIN (the charging power source) to the battery, or from the battery to PWRIN, are blocked in this mode. This mode consumes very little current from PWRIN or the battery.

When the IC is charging the battery from VIN, the boost regulator may be simultaneously enabled to supply 5 V for OTG peripherals.

Charge Mode

In Charge Mode, FAN54300 employs five regulation loops:

1. VBUS input current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface
2. Charging current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. Charge voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and R_{SENSE} works in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
4. Temperature: If the IC's junction temperature reaches 120°C, charge current is continuously reduced until the IC's temperature stabilizes at 120°C.
5. An additional loop limits the amount of drop on VBUS or VIN to a programmable voltage (V_{SP}) to accommodate current-limited wall chargers.

Input Source Selection

The FAN54300 selects the power source (PWRIN) for charging according to the following criteria.

Table 3. PWRIN: Charging Power Input Source Selection

V_{IN}	V_{BUS}	PWRIN
VALID	INVALID	V_{IN}
INVALID	VALID	V_{BUS}
VALID	VALID	V_{IN}

If charging is in progress with V_{BUS} and V_{IN} becomes valid, charging from VBUS stops and charging continues from V_{IN}. Charging stops if HZ_VIN is set when V_{IN} becomes valid while charging with V_{BUS}.

If VIN and VBUS are both connected and t_{15MIN} expires, both CE# bits are set. To reinitiate t_{15MIN} charging (autocharge) with a weak battery, both power sources must be unplugged, then a valid power source plugged in. If only one of the two connected sources are removed then connected with a weak battery, both CE# bits remain set.

Fault Reporting and Register Reset

All faults that occur during charging or boost are reported only in the STATUS register (R0) associated with the active charging source at the time of the fault. Any register reset that occurs due to t_{32SEC} overflow resets only the registers associated with the active charging source.

For example: Assume the IC is charging in 32-Second Mode with V_{IN} as a source. The processor stops setting TMR_RST, so t_{32SEC} expires. The IC then resets only the _V registers and goes into 15-Minute Mode charging with V_{IN}. A timer fault is enunciated, but reported in the CONTROL0_V register. CONTROL0_U is unaffected by this event. When the t_{15MIN} timer expires, the IC sets the CE#_V bit, but leaves the CE#_U bit unchanged.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source "pre-charges" the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuits are then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The FAN54300 is designed to work with a current-limited input source at PWRIN. During the current regulation phase of charging, PWRIN current limitations or the programmed charging current limit the amount of current available to charge the battery and power the system. The effect of input power limitations on I_{CHARGE} can be seen in Figure 47.

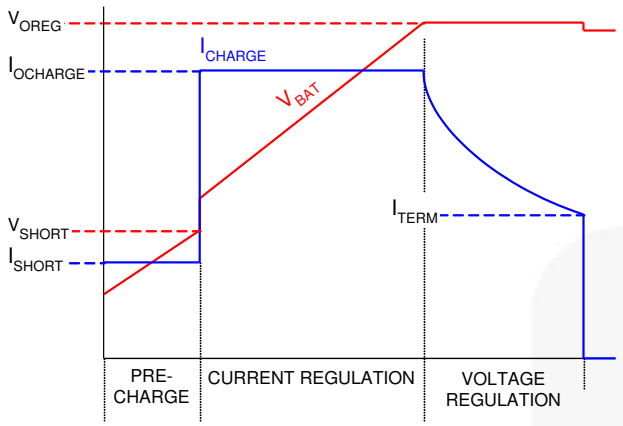


Figure 46. Charge Curve when PWRIN Limitations Don't Limit I_{CHARGE}

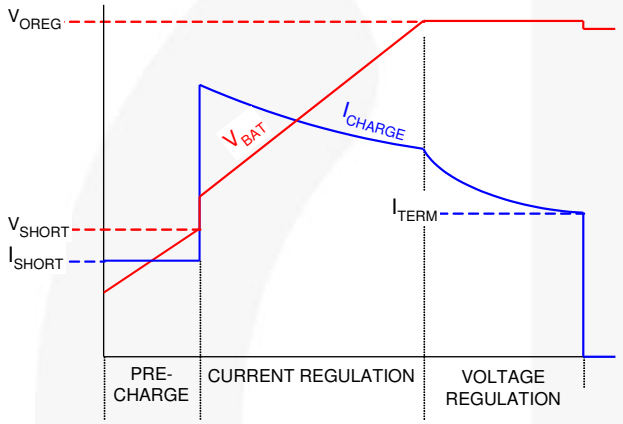


Figure 47. Charge Curve when PWRIN Limits I_{CHARGE}

PWRIN limitations are controlled either by:

- IBUSLIM: These bits set the maximum amount of current that the charger draws from VBUS; OR
- SP_CHARGER: For power-limited chargers, the FAN54300 limits current draw when the charging source drops to the voltage programmed by the SP_CHARGER bits. This allows "travel adapters" to be accommodated without host software overhead. The SP_CHARGER control loop applies to both VIN and VBUS.

Assuming V_{OREG} is programmed to the cell's fully charged "float" voltage, the current the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to VOREG declines and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit.

Charger Programmability

Throughout this document, any parameter that ends in "U" applies when charging from V_{BUS} and any parameter ending in "V" applies when charging from V_{IN}. Parameters set with slave address D6 are applied when charging from V_{BUS}. Parameters set with slave address D4 are applied when charging from V_{IN}.

The following charging and input power control parameters can be programmed by the host through I^2C.

Table 4. Programmable Charging Parameters

Parameter	Charging Source	Name	Register
Output Voltage Regulation	Either	OREG	REG2[7:2]
Battery Charging Current Limit	V_{BUS}	ICHGU	REG4[6:4]
	V_{IN}	ICHGV	REG4[6:3]
Input Current Limit	V_{BUS}	IBUSLIM	REG1[7:6]
Charge Termination Limit	Either	ITERM	REG4[2:0]
Special Charger Minimum Voltage	Either	VSP	REG5[2:0]

The charger output or "float" voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments.

Table 5. OREG Bits (REG2 [7:2]) vs. Charger V_{OUT} (V_{OREG}) Float Voltage

Decimal	Hex	VOREG	Decimal	Hex	VOREG
0	00	3.50	32	20	4.14
1	01	3.52	33	21	4.16
2	**02**	**3.54**	34	22	4.18
3	03	3.56	35	23	4.20
4	04	3.58	36	24	4.22
5	05	3.60	37	25	4.24
6	06	3.62	38	26	4.26
7	07	3.64	39	27	4.28
8	08	3.66	40	28	4.30
9	09	3.68	41	29	4.32
10	0A	3.70	42	2A	4.34
11	0B	3.72	43	2B	4.36
12	0C	3.74	44	2C	4.38
13	0D	3.76	45	2D	4.40
14	0E	3.78	46	2E	4.42
15	0F	3.80	47	2F	4.44
16	10	3.82	48	30	4.44
17	11	3.84	49	31	4.44
18	12	3.86	50	32	4.44
19	13	3.88	51	33	4.44
20	14	3.90	52	34	4.44
21	15	3.92	53	35	4.44
22	16	3.94	54	36	4.44
23	17	3.96	55	37	4.44
24	18	3.98	56	38	4.44
25	19	4.00	57	39	4.44
26	1A	4.02	58	3A	4.44
27	1B	4.04	59	3B	4.44
28	1C	4.06	60	3C	4.44
29	1D	4.08	61	3D	4.44
30	1E	4.10	62	3E	4.44
31	1F	4.12	63	3F	4.44

Note:

6. All register default settings are noted by **bold typeface**.