Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

June 2016

FAN602F
Offline Quasi-Resonant PWM Controller

Features

- High Efficiency Across Wide Input and Output Conditions in a Small Form Factor
- Quasi-Resonant Switching Operation with Two Step Maximum Blanking Frequency (140 kHz and 75 kHz)
- User Configurable Burst Mode Entry and Exit to Maximize Light-Load Efficiency and Minimize Audible Noise
- Adaptive Burst Mode Entry Level for Adaptive Charger Application
- mWSaver® Technology for Ultra Low Standby Power Consumption (<20 mW)
- Forced and Inherent Frequency Modulation of Valley Switching for Low EMI Emissions and Common Mode Noise
- Built-In and User Configurable Over-Voltage Protection (OVP), Under-Voltage Protection (UVP) and Over-Temperature Protection (OTP)
- Fully Programmable Brown-In and Brownout Protection
- Precise Constant Output Current Regulation with Programmable Line Compensation
- Built-In High-Voltage Startup to Reduce External Components
- 10 Lead SOIC JEDEC

Applications

- Battery Charges for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices or Battery Chargers that Require CV/CC Control

Description

The FAN602F is an advanced PWM controller aimed at achieving power density of ≥10W/in^3 in universal input range AC/DC flyback isolated power supplies. It incorporates Quasi-Resonant (QR) control with proprietary Valley Switching with a limited frequency variation. QR switching provides high efficiency by reducing switching losses while Valley Switching with a limited frequency variation bounds the frequency band to overcome the inherent limitation of QR switching.

FAN602F features mWSaver® burst mode operation with extremely low operating current (300 µA) and significantly reduces standby power consumption to meet the most stringent efficiency regulations such as Energy Star's 5-Star Level and CoC Tier II specifications.

FAN602F includes several user configurable features aimed at optimizing efficiency, EMI and protections. FAN602F has a programmable switching frequency range that provides flexibility in choosing noise rejection in targeted frequency zones. It incorporates user-configurable minimum peak current, which allows controlling the burst mode entry/exit power level, thereby enhancing light-load efficiency and eliminating audible noise. It also includes several rich programmable protection features such as Over-Voltage Protection (OVP), precise constant output current regulation (CC) and Over-Temperature Protection (OTP) through external thermistor.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN602FMX	-40°C to +125°C	10-Lead, Small Outline Package (SOIC), JEDEC MS-012, .150-Inch Narrow Body	Tape & Reel

Typical Application

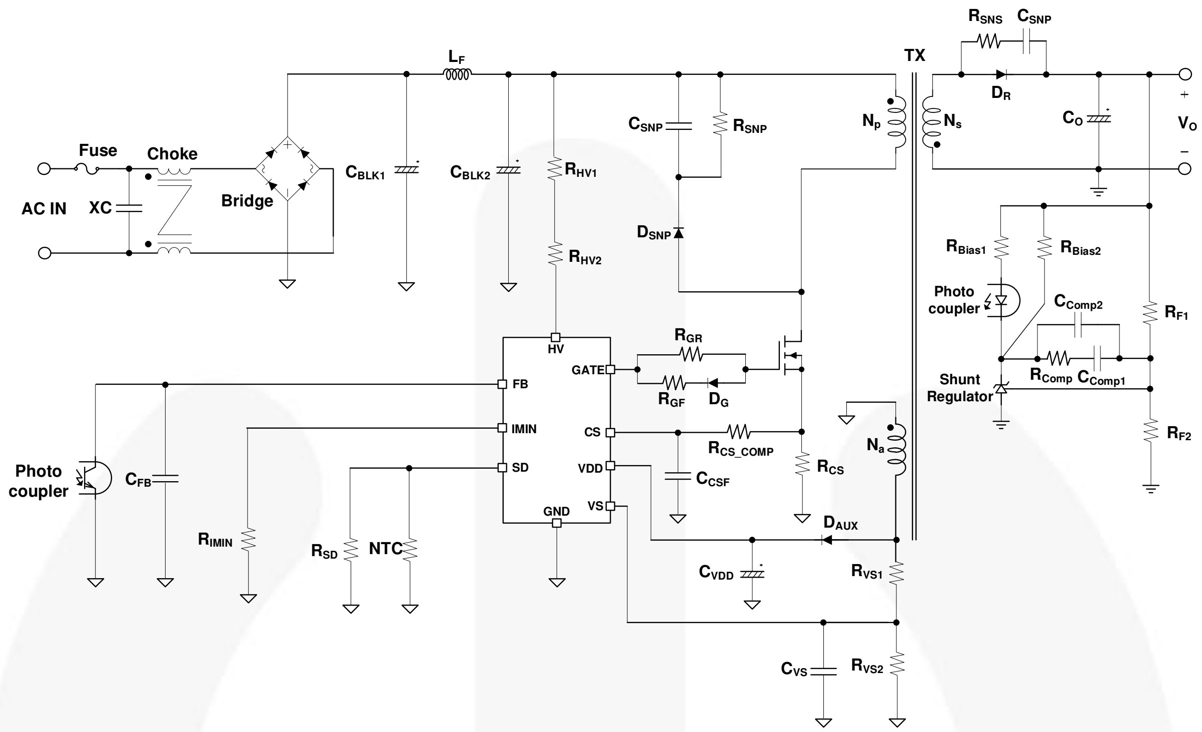


Figure 1. FAN602F Typical Application

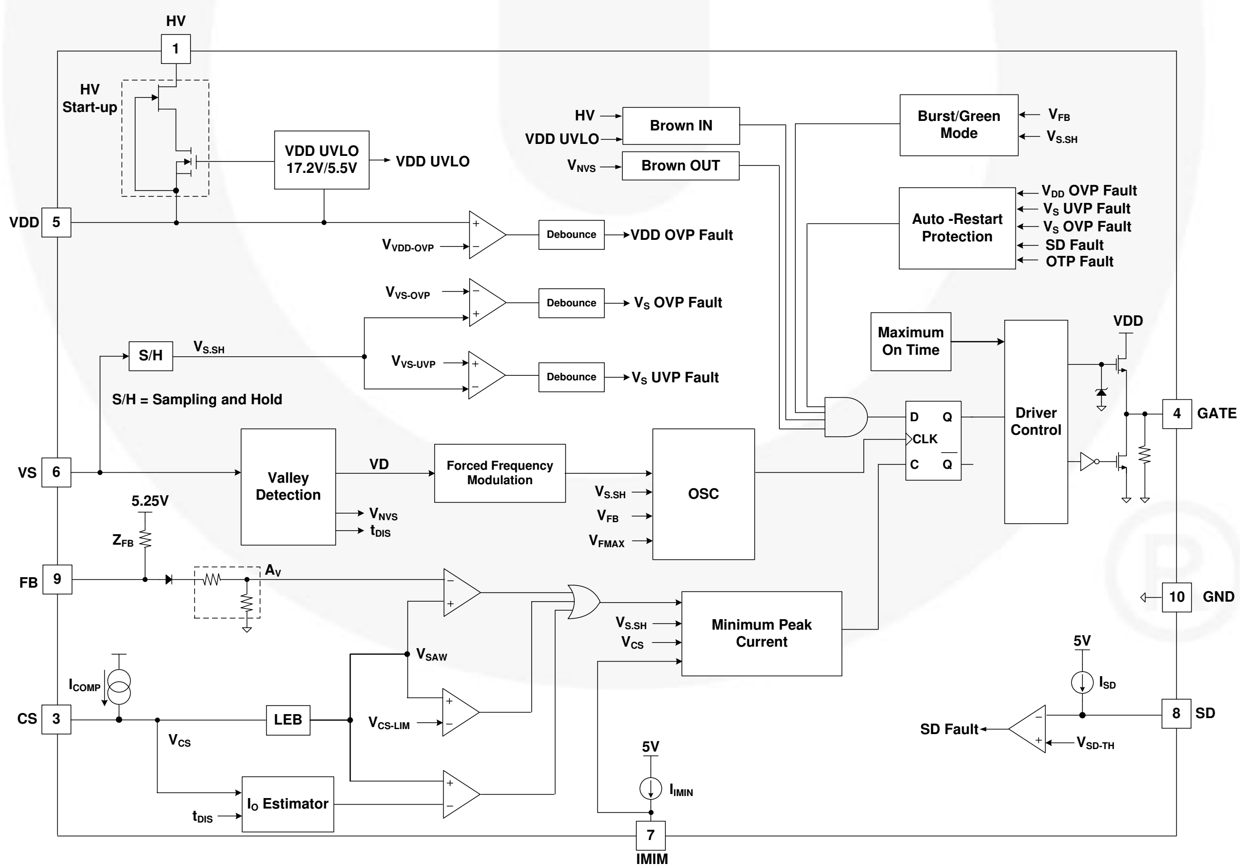


Figure 2. FAN602F Block Diagram

Marking Information

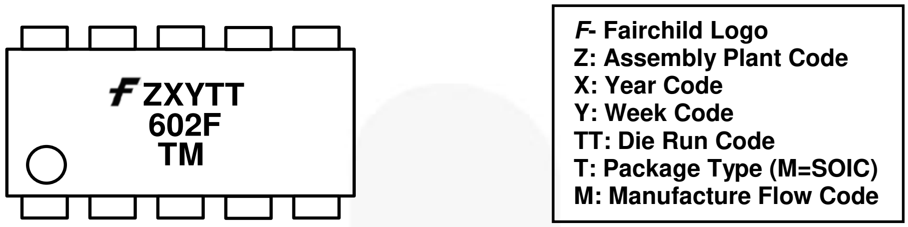


Figure 3. Top Mark

Pin Configuration

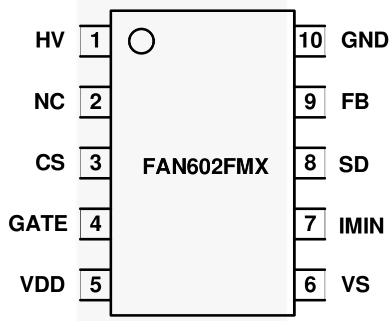


Figure 4. Pin Assignment

Pin Definitions

Pin #	Name	Description
1	HV	**High Voltage**. This pin connects to DC bus for high-voltage startup.
2	NC	**No Connect.**
3	CS	**Current Sense**. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation. The current sense information is also used to estimate the output current for CC regulation.
4	GATE	**PWM Signal Output**. This pin has an internal totem-pole output driver to drive the power MOSFET. The gate driving voltage is internally clamped at 7.5 V.
5	VDD	**Power Supply**. IC operating current and MOSFET driving current are supplied through this pin. This pin is typically connected to an external V_{DD} capacitor.
6	VS	**Voltage Sense**. The VS voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage. It also senses input voltage for Brownout protection.
7	IMIN	**Minimum V_{CS}.**This pin connects to external resistor to program minimum VCS Threshold level for burst mode operating optimization.
8	SD	**Shut Down.** This pin is implemented for external over-temperature-protect by connecting NTC thermistor.
9	FB	**Feedback**. Typically Opto-Coupler is connected to this pin to provide feedback information to the internal PWM comparator. This feedback is used to control the duty cycle in CV regulation.
10	GND	**Ground.**

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{HV}	HV Pin Input Voltage			500	V
V_{VDD}	DC Supply Voltage			30	V
V_{VS}	VS Pin Input Voltage		-0.3	6.0	V
V_{CS}	CS Pin Input Voltage		-0.3	6.0	V
V_{FB}	FB Pin Input Voltage		-0.3	6.0	V
V_{IMIN}	IMIN Pin Input Voltage		-0.3	6.0	V
V_{SD}	SD Pin Input Voltage		-0.3	6.0	V
P_D	Power Dissipation (T_A=25°C)			850	mW
θ_{JA}	Thermal Resistance (Junction-to-Ambient)			140	°C/W
Ψ_{JT}	Thermal Resistance (Junction-to-Top)			13	°C/W
T_J	Operating Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature Range		-40	+150	°C
T_L	Lead Temperature, (Wave soldering or IR, 10 Seconds)			+260	°C
ESD(3)	Electrostatic Discharge Capability	Human Body Model, JEDEC:JESD22_A114 (Except HV Pin)		3.0	kV
		Charged Device Model, JEDEC:JESD22_C101 (Except HV Pin)		2.0	

Notes:
1. All voltage values, except differential voltages, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. ESD ratings including HV pin: HBM=2.0 kV, CDM=2.0 kV.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{HV}	HV Pin Supply Voltage	50		400	V
V_{VDD}	VDD Pin Supply Voltage	6	15	25	V
V_{VS}	VS Pin Supply Voltage	0.65		2.90	V
V_{CS}	CS Pin Supply Voltage	0		0.9	V
V_{FB}	FB Pin Supply Voltage	0		5.25	V
V_{SD}	SD Pin Supply Voltage	0		5	V
V_{IMIN}	IMIN Pin Supply Voltage	0		2.5	V
T_A	Operating Temperature	-40		+85	°C

Electrical Characteristics

V_{DD}=15 V and T_J=-40~125°C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HV Section						
I_{HV}	Supply Current Drawn from HV Pin	V_{HV}=120 V, V_{DD}=0 V	1.2	2.0	10	mA
$I_{HV\text{-}LC}$	Leakage Current Drawn from HV Pin	V_{HV}=500 V, V_{DD}=$V_{DD\text{-}OFF}$+1 V	0	0.8	10	μA
$V_{Brown\text{-}IN}$	Brown-In Threshold Voltage.	R_{HV}=150 kΩ, V_{IN}=80 V_{rms}	100	110	120	V
V_{DD} Section						
$V_{DD\text{-}ON}$	Turn-On Threshold Voltage	V_{DD} Rising	15.3	17.2	18.7	V
$V_{DD\text{-}OFF}$	Turn-Off Threshold Voltage	V_{DD} Falling	5.0	5.5	5.7	V
$V_{DD\text{-}HV\text{-}ON}$	Threshold Voltage for HV Startup	T_J=25°C	4.1	4.7	5.4	V
$I_{DD\text{-}ST}$	Startup Current	V_{DD}=$V_{DD\text{-}ON}$-0.16 V, T_J=25°C		300	400	μA
$I_{DD\text{-}OP}$	Operating Supply Current	V_{CS}=5.0 V, V_S=3 V, V_{FB}=3 V, V_{DD}=15 V, C_{GATE}=1 nF		2	3	mA
$I_{DD\text{-}Burst}$	Burst-Mode Operating Supply Current	V_{CS}=0.3 V, V_S=0 V, V_{FB}=0 V; V_{DD}=$V_{DD\text{-}ON}$→$V_{DD\text{-}OVP}$→10 V, C_{GATE}=1 nF		300	600	μA
$V_{VDD\text{-}OVP}$	V_{DD} Over-Voltage-Protection Level	T_J=25°C	27.5	29.0	29.5	V
$t_{D\text{-}VDDOVP}$	VDD Over-Voltage-Protection Debounce Time			70	105	μs
Oscillator Section						
$f_{BNK\text{-}MAX}$	Maximum Blanking Frequency	V_{FB} > $V_{FB\text{-}BNK\text{-}H}$	130	140	150	kHz
$f_{BNK\text{-}MIN}$	Minimum Blanking Frequency	V_{FB} < $V_{FB\text{-}BNK\text{-}L}$, T_J=25°C	70	75	80	kHz
$f_{OSC\text{-}MIN\text{-}DCM}$	Minimum Frequency for DCM	V_{VS}=0 V	40	50	60	kHz
$f_{OSC\text{-}MIN\text{-}CrM}$	Minimum Frequency for CrM	V_{VS}=1 V, T_J=25°C	11	20	29	kHz
$\Delta t_{FM\text{-}Range}$	Forced Frequency Modulation Range	V_{FB}> $V_{FB\text{-}Burst\text{--}H}$	225	265	305	ns
$\Delta t_{FM\text{-}Period}$	Forced Frequency Modulation Period		2.1	2.5	2.9	ms
$V_{FB\text{-}BNK\text{-}H\text{-}H}$	Frequency Jumping point V_{FB}	V_{S_SH} > 2.1 V	2.0	2.1	2.2	V
$V_{FB\text{-}BNK\text{-}L\text{-}H}$	Frequency Jumping point V_{FB}		1.8	1.9	2.0	V
$V_{FB\text{-}BNK\text{-}H\text{-}L}$	Frequency Jumping point V_{FB}	V_{S_SH} < 2.0 V	1.55	1.65	1.75	V
$V_{FB\text{-}BNK\text{-}L\text{-}L}$	Frequency Jumping point V_{FB}		1.35	1.45	1.55	V
Feedback Input Section						
Z_{FB}	FB Pin Input Impedance		39	42	45	kΩ
$A_{V\text{-}H}$	Internal Voltage Attenuator of FB Pin(4)	V_{FB} > $V_{FB\text{-}BNK\text{-}H}$	1/3	1/3.5	1/4	V/V
$A_{V\text{-}L}$	Internal Voltage Attenuator of FB Pin(4)	V_{FB} < $V_{FB\text{-}BNK\text{-}L}$	1/2.1	1/2.6	1/3.1	V/V
$V_{FB\text{-}Open}$	FB Pin Pull-Up Voltage	FB Pin Open	4.75	5.25	5.90	V
$V_{FB\text{-}Burst\text{-}H}$	FB Threshold to Enable/Disable Gate Drive in Burst Mode	V_{FB} Rising	0.85	0.95	1.05	V
$V_{FB\text{-}Burst\text{-}L}$		V_{FB} Falling	0.8	0.9	1.0	V

Continued on the following page…

Electrical Characteristics

V_{DD}=15 V and T_J=-40~125 °C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Voltage-Sense Section						
$I_{VS\text{-}MAX}$	Maximum V_S Source Current Capability				3	mA
$t_{VS\text{-}BNK1}$	V_S Sampling Blanking Time 1 after GATE Pin Pull-Low	$V_{FB} < V_{FB\text{-}BNK\text{-}L}$	0.9	1.1	1.37	µs
$t_{VS\text{-}BNK2}$	V_S Sampling Blanking Time 2 after GATE Pin Pull-Low	$V_{FB} > V_{FB\text{-}BNK\text{-}H}$, T_J=25°C	1.6	1.8	2.1	µs
$t_{ZCD\text{-}to\ PWM}$	Delay from VS Voltage Zero Crossing to PWM ON(4)	V_{VS}=0 V, C_{GATE}=1 nF		175		ns
$I_{VS\text{-}Brownout}$	V_S Source Current Threshold to Enable Brownout	Set I_{VS}=2.4 mA at 264 V_{rms}, Brownout=55 V_{rms}	370	450	520	µA
$t_{D\text{-}Brownout}$	Brownout Debounce Time		12.5	16.5	21	ms
$V_{VS\text{-}OVP}$	Output Over-Voltage-Protection with Vs Sampling Voltage		2.8	2.9	3.0	V
$N_{VS\text{-}OVP}$	Output Over-Voltage-Protection Debounce Cycle Counts			2		Cycle
$V_{VS\text{-}UVP\text{-}H}$	Output Under-Voltage-Protection with Vs Sampling Voltage	T_J=25°C	0.76	0.80	0.84	V
$V_{VS\text{-}UVP\text{-}L}$	Output Under-Voltage-Protection with Vs Sampling Voltage	T_J=25°C	0.625	0.650	0.675	V
$N_{VS\text{-}UVP}$	Output Over-Voltage-Protection Debounce Cycle Counts			2		Cycle
$t_{VS\text{-}UVP\text{-}BLANK}$	Output Under-Voltage Protection Blanking Time at start-up		25	40	55	ms
$N_{VDD\text{-}Hiccup}$	Auto-Restart 2 Cycles Mode Counts	$V_{S\_SH} < V_{VS\text{-}UVP}$		2		Cycle
Over-Temperature Protection Section						
T_{OTP}	Threshold Temperature for Over-Temperature-Protection(4)			140		°C
Current-Sense Section						
$V_{CS\text{-}LIM}$	Current Limit Threshold Voltage	FB Pin Open	0.85	0.9	0.95	V
I_{IMIN}	IMIN Pin Current		9	10	11	µA
$V_{CS\text{-}IMIN\text{-}MIN}$	Minimum Current Sense Voltage	V_{S_SH}=2.5 V,R_{IMIN}=250 kΩ	0.050	0.100	0.150	V
$V_{CS\text{-}IMIN\text{-}MAX}$	Maximum Current Sense Voltage	V_{S_SH}=2.5 V,R_{IMIN}=0 Ω	0.185	0.225	0.255	V
t_{PD}	GATE Output Turn-Off Delay			100	200	ns
t_{LEB}	Leading-Edge Blanking Time			150	200	ns

Continued on the following page…

Electrical Characteristics

V_{DD}=15 V and T_J=-40~125 °C unless noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Shut-Down Function Section						
I_{SD}	SD Pin Source Current		90	103	110	μA
V_{SD-TH}	Threshold Voltage for Shut-Down Function Enable		0.95	1.00	1.05	V
t_{D-SD}	Debounce Time for Shut-Down Function		200	400	600	μs
$V_{SD-TH-ST}$	Hysteresis of Threshold Voltage for Shut-Down Function Enable		1.30	1.35	1.40	V
t_{SD-ST}	Duration of $V_{SD-TH-ST}$ at startup		0.8	1.3	1.8	ms
Constant Current Correction Section						
I_{COMP-H}	High Line Compensation Current	V_{IN}=264 V_{rms}	90	100	110	μA
I_{COMP-L}	Low Line Compensation Current	V_{IN}=90 V_{rms}	32	36	40	μA
Constant Current Estimator						
V_{REF_CC}	Constant Current Control Reference Voltage[(4)]			1.2		V
A_{PK}	Peak Value Amplifying Gain[(4)]			3.6		V/V
$V_{FB-CC-Open}$	FB CC Pull-Up Voltage[(4)]			4.0		V
A_{V-CC}	Internal Voltage Attenuator of FB CC[(4)]			0.444		V/V
GATE Section						
V_{GATE-L}	Gate Output Voltage Low		0		1.5	V
$V_{DD-PMOS-ON}$	Internal Gate PMOS Driver ON		7.0	7.5	8.0	V
$V_{DD-PMOS-OFF}$	Internal Gate PMOS Driver OFF		9.0	9.5	10.0	V
t_r	Rising Time	V_{CS}=0 V, V_S=0 V, C_{GATE}=1 nF	100	135	180	ns
t_f	Falling Time	V_{CS}=0 V, V_S=0 V, C_{GATE}=1 nF	30	50	70	ns
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=25 V	6.8	7.5	8.2	V
t_{ON-MAX}	Maximum On Time	V_{FB}=3 V, V_{CS}=0.3 V	18	20	23	μs

Note:
4. Guaranteed by design.

Typical Performance Characteristics

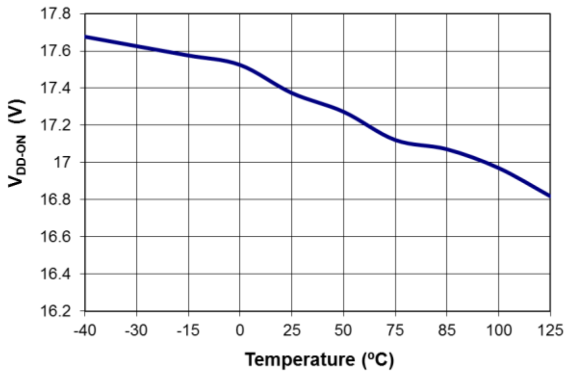


Figure 5. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

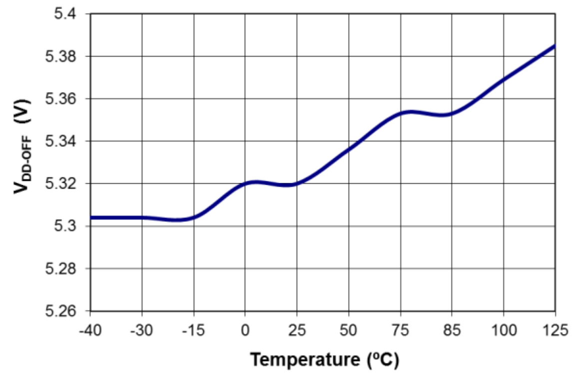


Figure 6. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

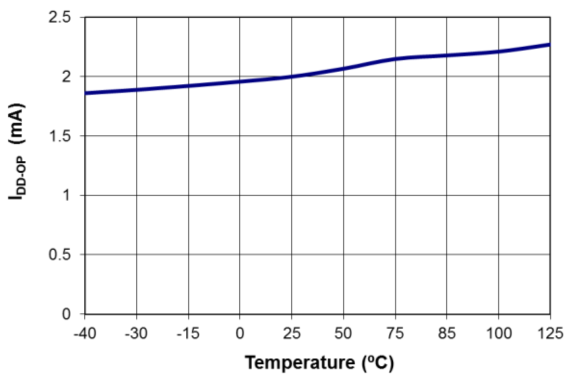


Figure 7. Operating Supply Current (I_{DD-OP}) vs. Temperature

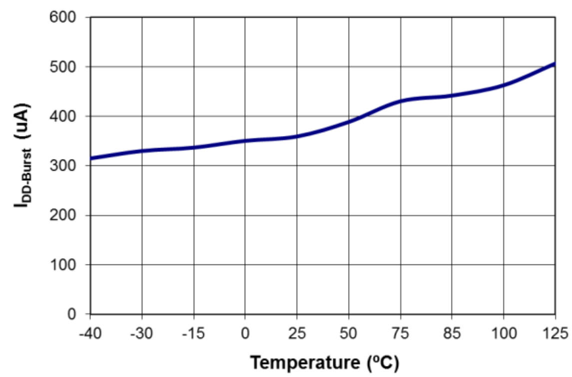


Figure 8. Burst-Mode Operating Supply Current ($I_{DD-Burst}$) vs. Temperature

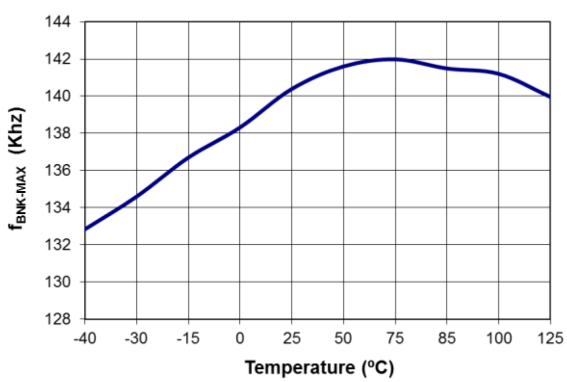


Figure 9. Maximum Blanking Frequency ($f_{BNK-MAX}$) vs. Temperature

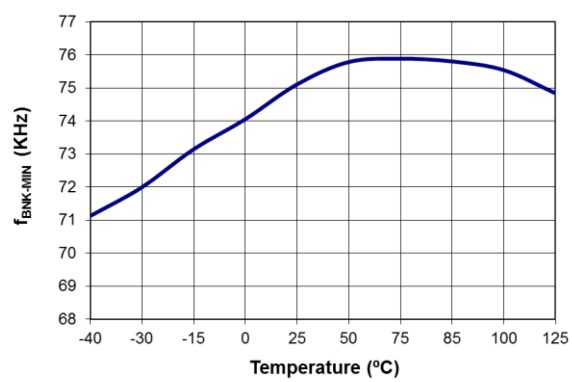


Figure 10. Minimum Blanking Frequency ($f_{BNK-MIN}$) vs. Temperature

Typical Performance Characteristics (Continued)

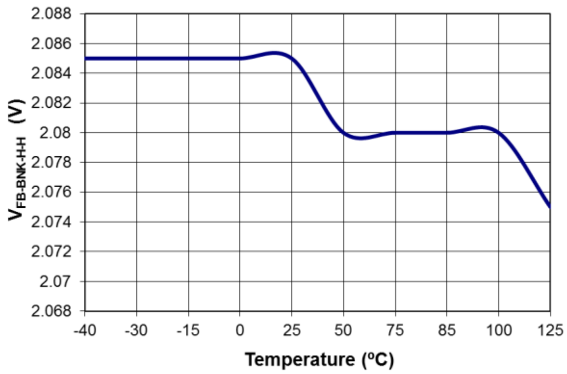


Figure 11. Frequency Jumping point ($V_{FB-BNK-H-H}$) vs. Temperature

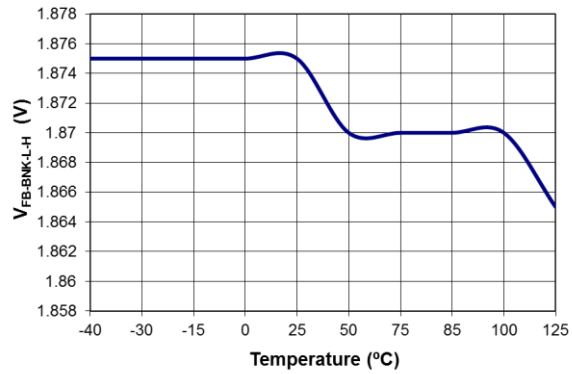


Figure 12. Frequency Jumping point ($V_{FB-BNK-L-H}$) vs. Temperature

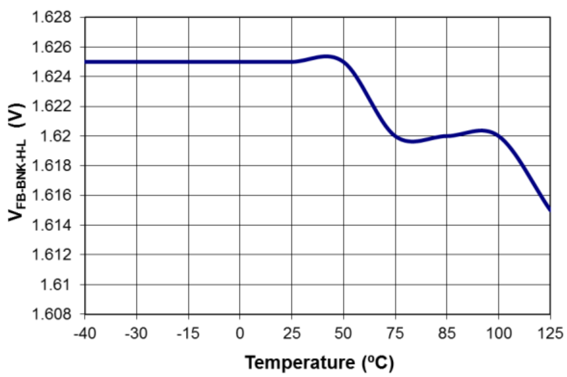


Figure 13. Frequency Jumping point ($V_{FB-BNK-H-L}$) vs. Temperature

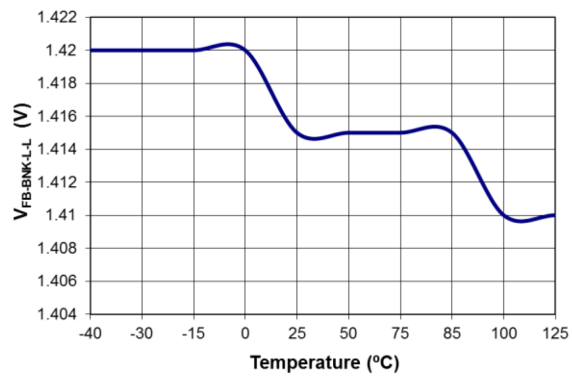


Figure 14. Frequency Jumping point ($V_{FB-BNK-L-L}$) vs. Temperature

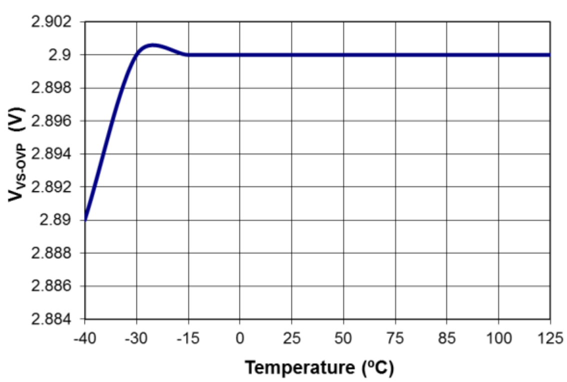


Figure 15. Output Over-Voltage-Protection V_{VS-OVP}) vs. Temperature

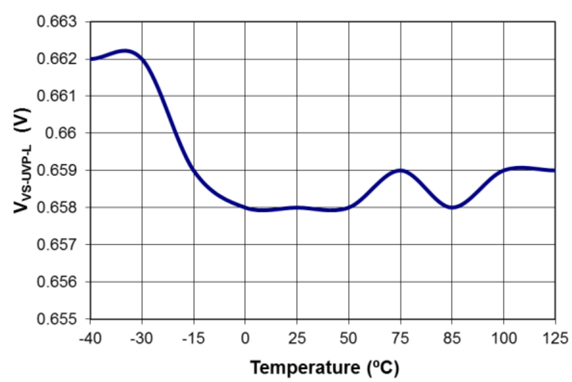


Figure 16. Output Under-Voltage Protection ($V_{VS-UVP-L}$) vs. Temperature

Typical Performance Characteristics (Continued)

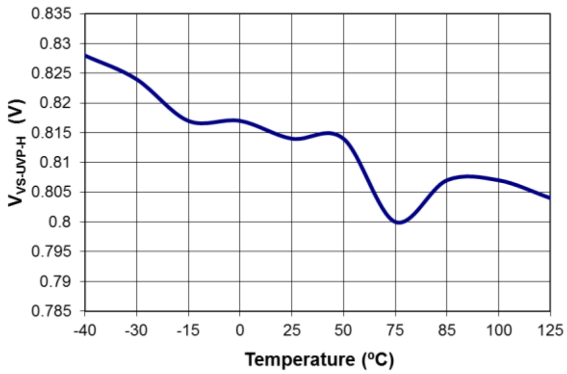


Figure 17. Output Under-Voltage Protection ($V_{VS-UVP-H}$) vs. Temperature

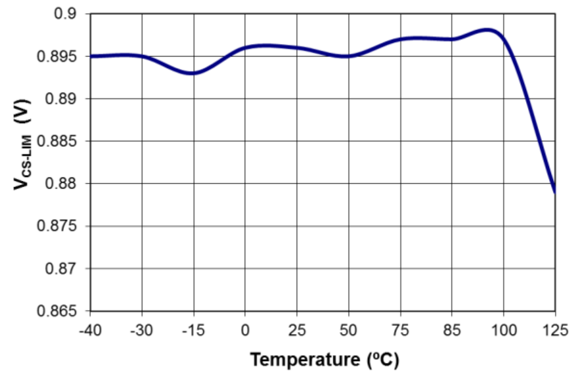


Figure 18. Current Limit Threshold Voltage (V_{CS-LIM}) vs. Temperature

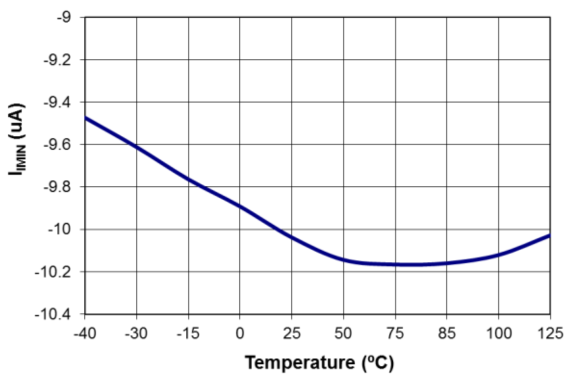


Figure 19. IMIN Pin Current (I_{IMIN}) vs. Temperature

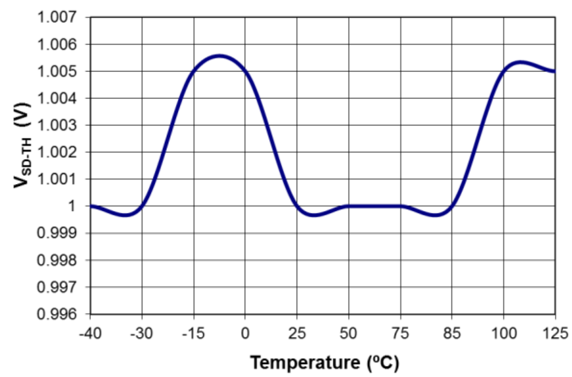


Figure 20. Threshold Voltage for Shutdown Function Enable (V_{SD-TH}) vs. Temperature

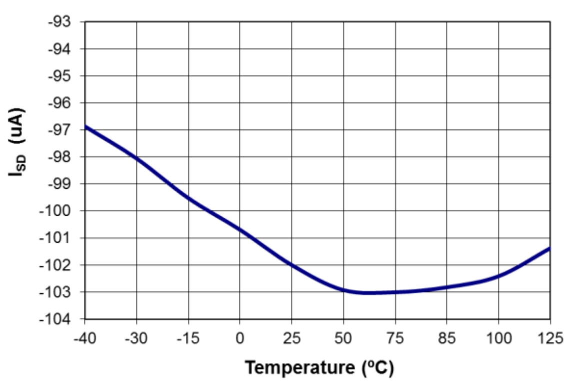


Figure 21. SD Pin Source Current (I_{SD}) vs. Temperature

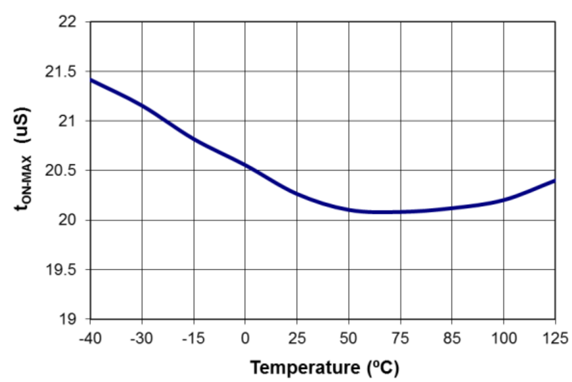


Figure 22. Maximum On Time (t_{ON-MAX}) vs. Temperature

Functional Description

FAN602F is an offline PWM controller which operates in a quasi-resonant (QR) mode and significantly enhances system efficiency and power density. Its control method is based on the load condition (valley switching with the maximum blanking time at heavy load and valley switching with the minimum blanking time at medium load) to maximize the efficiency. It offers constant output voltage (CV) regulation through opto-coupler feedback circuitry.

Line voltage compensation gain can be programmed by using an external resistor to minimize the effect of line voltage variation on output current regulation due to turn-off delay of the gate drive circuit. FAN602F incorporates HV startup and accurate brown-in through HV pin. The brown-in voltage is programmed by using an external HV pin resistor. The minimum peak current ($V_{CS\text{-}IMIN}$), which controls the burst mode entry/exit and improves light-load efficiency, is programmable via an external resistor connected to the IMIN pin.

Basic Operation Principle

Quasi-resonant switching is a method to reduce primary MOSFET switching losses especially in high line. In order to perform QR turn-on of the primary MOSFET, the valley of the resonance occurring between transformer magnetizing inductance (L_m) and MOSFET effective output capacitance ($C_{oss\text{-}eff}$) must be detected.

$$C_{OSS-eff} = C_{OSS-MOSFET} + C_{trans} + C_{parasitic} \quad (1)$$

$$t_{resonance} = 2\pi \cdot \sqrt{L_m \cdot C_{OSS-eff}} \quad (2)$$

For heavy load condition (55%~100% of full load), the blanking time for the valley detection is fixed such that the switching time is between t_{BNK} and $t_{BNK}+t_{resonance}$. For the medium load condition (10%~55% of full load), the blanking time is changed by V_{FB} and output voltage such that the upper limit of the blanking frequency varies from $f_{BNK\text{-}MAX}$ to $f_{BNK\text{-}MIN}$.

For adaptive output application, the blanking frequency jumping point will be changed by threshold voltage of $V_{S\text{-}SH}$. At high output voltage, $V_{FB\text{-}BNK\text{-}L}$= $V_{FB\text{-}BNK\text{-}L\text{-}H}$(1.9 V) and $V_{FB\text{-}BNK\text{-}H}$= $V_{FB\text{-}BNK\text{-}H\text{-}H}$ (2.1 V) when $V_{S\text{-}SH}$ > 2.1 V. At low output voltage, $V_{FB\text{-}BNK\text{-}L}$= $V_{FB\text{-}BNK\text{-}L\text{-}L}$(1.45 V) and $V_{FB\text{-}BNK\text{-}H}$= $V_{FB\text{-}BNK\text{-}H\text{-}L}$(1.65 V) when $V_{S\text{-}SH}$ < 2.0 V as shown in Figure 24.

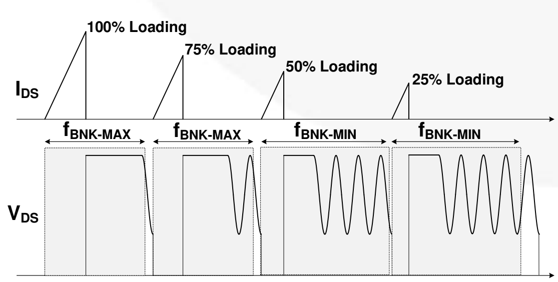


Figure 23. Two Step Blanking Frequency

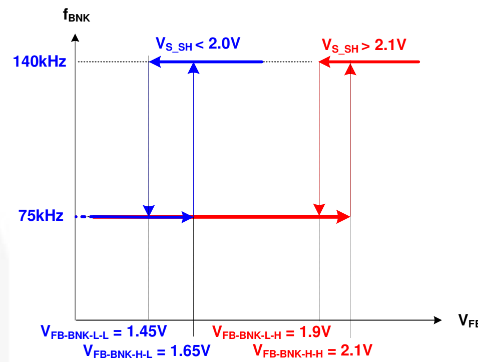


Figure 24. The Blanking Frequency Jumping Point with Variation of $V_{S\text{-}SH}$

Valley Detection

There will be a logic propagation delay from VS Zero-Crossing Detection ($V_{S\text{-}ZCD}$) to IC GATE turn on and a MOSFET gate drives propagation delay from GATE pin to MOSFET turn on. We can assume the sum of these propagation delays to be $t_{ZCD\text{-}to\text{-}PWM}$, as shown in Figure 26. However, if 1/2 t_F is larger than $t_{ZCD\text{-}to\text{-}PWM}$, the switching occurs away from the valley causing higher losses. The time period of resonant ringing is dependent on L_m and $C_{oss\text{-}eff.}$ Typically, the time period of resonance ringing is around 1~1.5 µs depending on the system parameters. Hence, the switching may occur at a point different from the valley depending on the system. When PCB layout is poor, it may cause noise on the VS pin. The VS pin needs to be in parallel with the capacitor (C_{VS}) less than 10 pF to filter the noise.

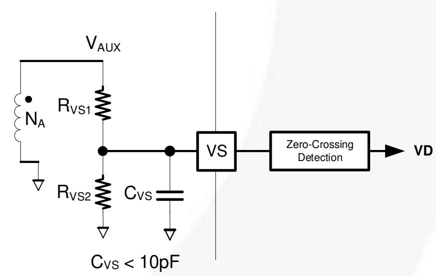


Figure 25. The Valley Detection Circuit

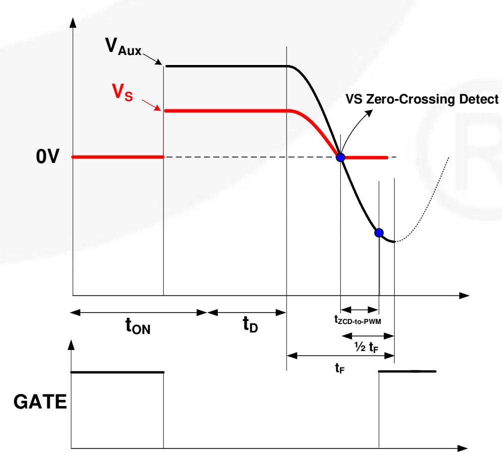


Figure 26. Valley Detection Behavior

Inherent and Forced Frequency Modulation

Typically, the bulk capacitor of flyback converter has a longer charging time in low line than in high line. Thus, the voltage ripple (ΔV_{DC}) in low line is higher as shown in Figure 27. This large ripple results in 4~6% variation of the switching frequency in low line for a valley switched converter. Hence, the EMI performance in low line is satisfied. However, in high line, the ripple is very small and consequent. The EMI performance for high line may suffer. In order to maintain good EMI performance for high line, forced frequency modulation is provided. FAN602F varies the valley switching point from 0 to $\Delta t_{FM-Range}$ (265 ns) in every $\Delta t_{FM-Period}$ (2.5 ms) as shown in Figure 28. Since the drain voltage at which the switching occurs does not change much with this variation, there is minimum impact on the efficiency.

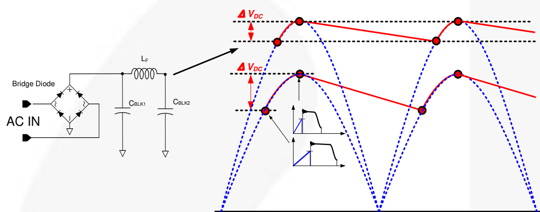


Figure 27. Inherent Frequency Modulation

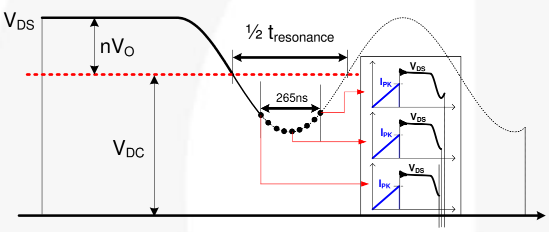


Figure 28. Forced Frequency Modulation

Output Voltage Detection

Figure 29 shows the VS voltage is sampled (V_{S-SH}) after t_{VS-BNK} of GATE turn-off so that the ringing does not introduce any error in the sampling. FAN602F dynamically varies t_{VS-BNK} with load. At heavy load, $t_{VS-BNK}=t_{VS-BNK1}$ (1.8 µs) when $V_{FB} > V_{FB-BNK-H}$. At light-load, $t_{VS-BNK}=t_{VS-BNK2}$ (1.1 µs) when $V_{FB} < V_{FB-BNK-L}$. This dynamic variation ensures that VS sampling occurs after ringing due to leakage inductance has stopped and before secondary current goes to zero.

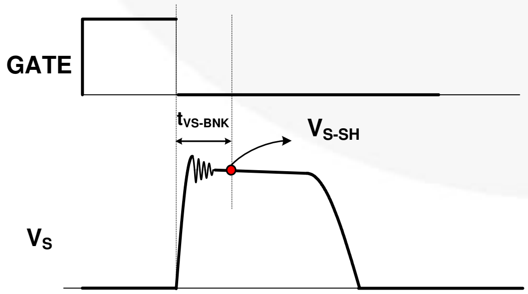


Figure 29. Output Voltage Detection

$$V_{S-SH} = V_O \cdot \frac{N_A}{N_S} \cdot \frac{R_{VS2}}{(R_{VS1} + R_{VS2})} \tag{3}$$

Burst Mode Operation

FAN602F features burst mode operation with a programmable burst mode entry load condition by using minimum peak current ($V_{CS-IMIN}$) control which enables light-load efficiency to be optimized for a given application. The IMIN pin can be programmed with external resistor R_{IMIN} to select the minimum V_{CS} threshold level for burst mode entry. Figure 30 shows the implementation of IMIN in FAN602F.

Figure 31 shows when V_{FB} drops below $V_{FB-Burst-L}$, the PWM output shuts off and the output voltage drops at a rate which is depended on the load current level. This causes the feedback voltage to rise. Once V_{FB} exceeds $V_{FB-Burst-H}$, FAN602F resumes switching. As shown in Figure 32, when the FB voltage drops below the corresponding $V_{CS-IMIN}$, the peak currents in switching cycles are fixed to $V_{CS-IMIN}$ regardless of FB voltage. Thus, more power is delivered to the load than required and once FB voltage is pulled low below $V_{FB-Burst-L}$, switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the MOSFET to reduce the switching losses.

For adaptive output application, the minimum peak current is modulated in accordance with the V_{S-SH} such that the minimum peak current is proportional to the square root of output voltage. For easy circuit implementation, curve fitting is used as shown in Figure 33.

$$V_{CS-IMIN} = \frac{(V_{S-SH} - I_{MIN} \times R_{IMIN})}{20} + 0.1 \tag{4}$$

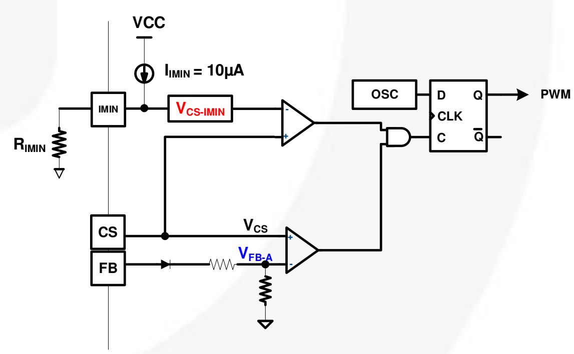


Figure 30. IMIN Function Circuit

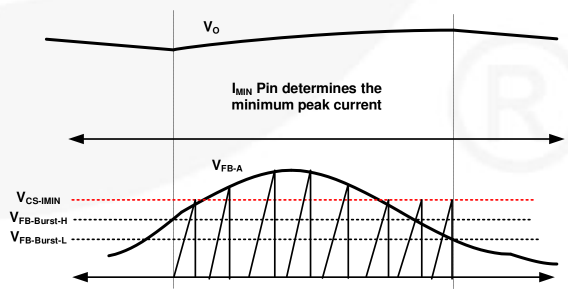


Figure 31. Burst-Mode Operation with IMIN

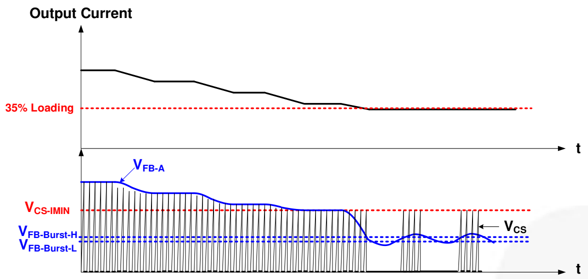


Figure 32. System enter Burst-Mode Behavior

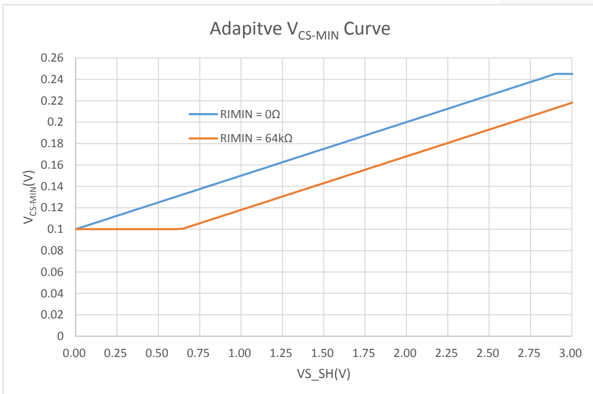


Figure 33. $V_{CS\text{-}IMIN}$ as a Function of R_{IMIN} with Variation of $V_{S\text{-}SH}$

Deep Burst Mode

FAN602F enters deep burst mode if FB voltage stays lower than $V_{FB\text{-}Burst\text{-}L}$ for more than $t_{Deep\text{-}Burst\text{-}Entry}$ (640 µs). Once FAN602F enters deep burst mode, the operating current is reduced to $I_{DD\text{-}Burst}$ (300 µA) to minimize power consumption. Once feedback voltage is more than $V_{FB\text{-}Burst\text{-}H}$, power-on-reset occurs within a time period of $t_{Deep\text{-}Burst\text{-}Exit}$ (25 µs) and IC resumes switching with normal operating current, $I_{DD\text{-}OP}$.

Line Voltage Detection

The FAN602F indirectly senses the line voltage through the VS pin while the MOSFET is turned on, as illustrated in Figure 34 and Figure 35. During MOSFET turn-on period, the auxiliary winding voltage, V_{AUX}, is proportional to the input bulk capacitor voltage, V_{BLK}, due to the transformer coupling between the primary and auxiliary windings. During the MOSFET conduction time, the line voltage detector clamps the VS pin voltage to $V_{S\text{-}Clamp}$ (0 V), and then the current I_{VS} flowing out of VS pin is expressed as:

$$I_{VS} = \frac{V_{BLK}}{R_{VS1}} \cdot \frac{N_A}{N_S} \qquad (5)$$

The I_{VS} current, reflecting the line voltage information, is used for brownout protection and CC control correction weighting.

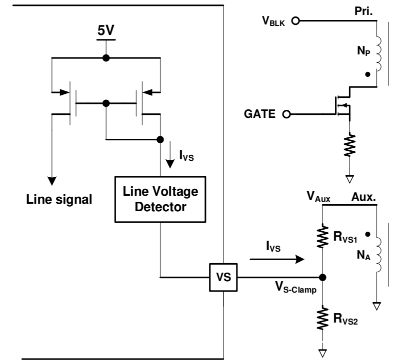


Figure 34. Line Voltage Detection Circuit

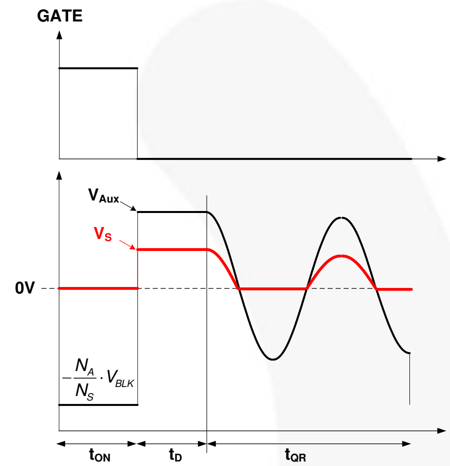


Figure 35. Waveforms for Line Voltage Detection

CV / CC PWM Operation Principle

Figure 36 shows a simplified CV / CC PWM control circuit of the FAN602F. The Constant Voltage (CV) regulation is implemented in the same manner as the conventional isolated power supply, where the output voltage is sensed using a voltage divider and compared with the internal reference of the shunt regulator to generate a compensation signal. The compensation signal is transferred to the primary side through an opto-coupler and scaled down by attenuator A_V to generate a COMV signal. This COMV signal is applied to the PWM comparator to determine the duty cycle.

The Constant Current (CC) regulation is implemented internally with primary-side control. The output current estimator calculates the output current using the transformer primary-side current and diode current discharge time. By comparing the estimated output current with internal reference signal, a COMI signal is generated to determine the duty cycle.

These two control signals, COMV and COMI, are compared with an internal sawtooth waveform (V_{SAW}) by two PWM comparators to determine the duty cycle. Figure 37 illustrates the outputs of two comparators, combined with an OR gate, to determine the MOSFET turn-off instant. Either of COMV or COMI, the lower signal determines the duty cycle. As shown in Figure 37, during CV regulation, COMV determines the duty cycle while COMI is saturated to HIGH level. During CC regulation, COMI determines the duty cycle while COMV is saturated to HIGH level.

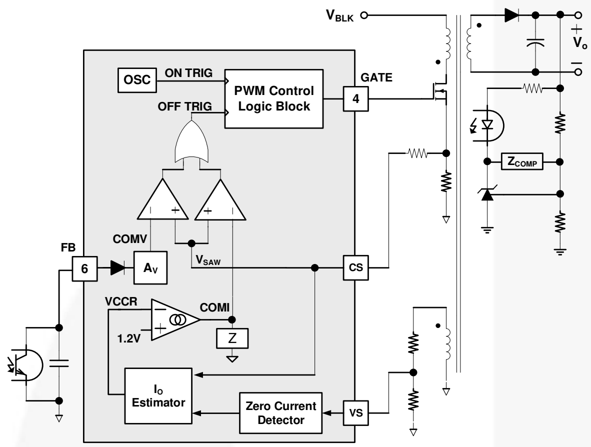


Figure 36. Simplified PWM Control Circuit

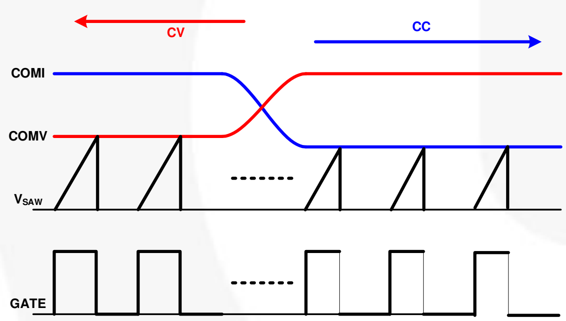


Figure 37. PWM Operation for CV/CC Regulation

Primary-Side Constant Current Operation

Figure 38 shows the key waveforms of a flyback converter operating in DCM. The output current is estimated by calculating the average of output diode current in the one switching cycle:

$$I_O = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{CS-PK}\cdot T_{dis}}{T_S}\frac{N_P}{N_S}\eta = \frac{1}{2}\frac{1}{R_{CS}}\frac{V_{REF\_CC}}{A_{PK}}\frac{N_P}{N_S}\eta \qquad (6)$$

When the diode current reaches zero, the transformer winding voltage begins to drop sharply and VS pin voltage drops as well. When VS pin voltage drops below the V_{S-SH} by more than 500 mV, zero current detection (ZCD) of diode current is obtained.

The output current can be programmed by setting the current sensing resistor as:

$$R_{CS} = \frac{1}{2}\cdot\frac{1}{I_O}\cdot\frac{V_{REF\_CC}}{A_{PK}}\cdot\frac{N_P}{N_S}\cdot\eta \qquad (7)$$

Where V_{REF_CC} is the internal voltage for CC control and A_{PK} is the IC design parameter, 3.6 for FAN602F.

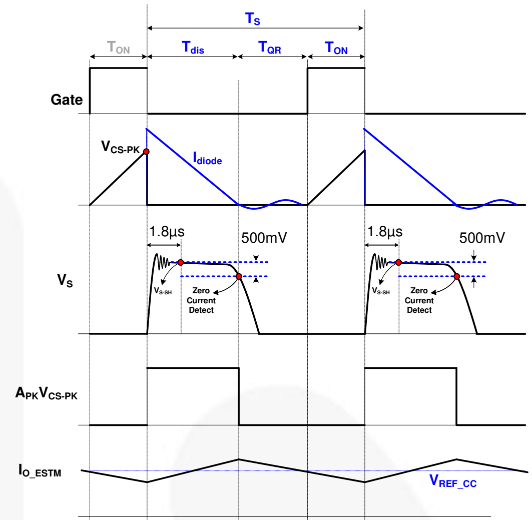


Figure 38. Waveforms for Estimate Output Current

Line Voltage Compensation

The output current estimation is also affected by the turn-off delay of the MOSFET as illustrated in Figure 39. The actual MOSFET's turn-off time is delayed due to the MOSFET gate charge and gate driver's capability, resulting in peak current detection error as

$$\Delta I_{DS}{}^{PK} = \frac{V_{BLK}}{L_m}\cdot t_{OFF.DLY} \qquad (8)$$

Where L_m is the transformer's primary side magnetizing inductance. Since the output current error is proportional to the line voltage, the FAN602F incorporates line voltage compensation to improve output current estimation accuracy. Line information is obtained through the line voltage detector as shown in Figure 34. I_{COMP} is an internal current source, which is proportional to line voltage. The line compensation gain is programmed by using CS pin series resistor, R_{CS_COMP}, depending on the MOSFET turn-off delay, $t_{OFF.DLY}$. I_{COMP} creates a voltage drop, V_{OFFSET}, across R_{CS_COMP}. This line compensation offset is proportional to the DC link capacitor voltage, V_{BLK}, and turn-off delay, $t_{OFF.DLY}$. Figure 40 demonstrates the effect of the line compensation.

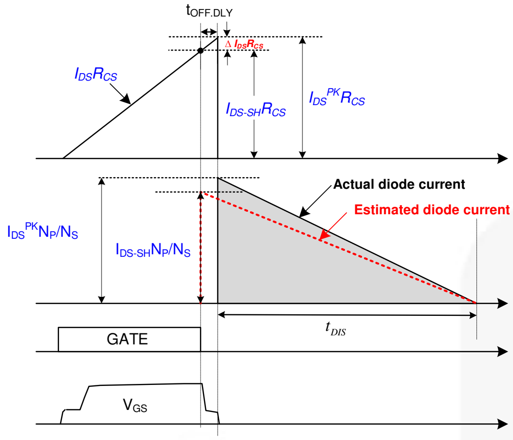


Figure 39. Effect of MOSFET Turn-off Delay

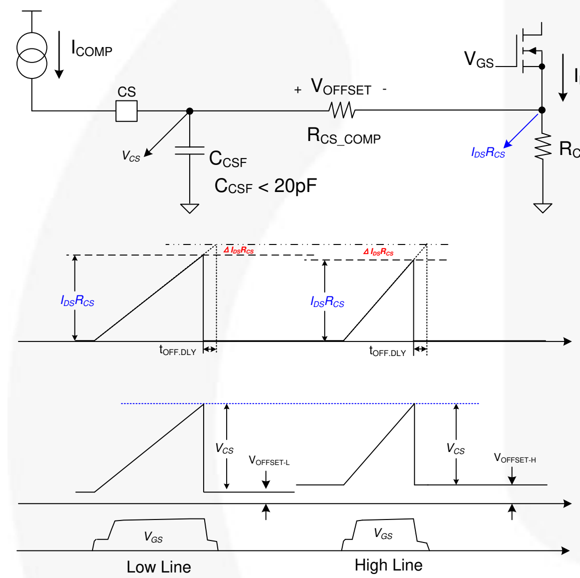


Figure 40. Line Voltage Compensation

CCM Prevention

When input or output voltage drops, the secondary side current does not reduce to zero within $t_{OSC\text{-}MIN\text{-}DCM}$ (time period for $f_{OSC\text{-}MIN\text{-}DCM}$). FAN602F does not initiate turn-on. FAN602F turns on the primary MOSFET after VS-ZCD and ensures boundary conduction mode switching. Thus FAN602F does not allow the converter to enter CCM. During CCM prevention, FAN602F can reduce the frequency down to $f_{OSC\text{-}MIN\text{-}CrM}$ (20 kHz). This phenomenon is explained in Figure 41.

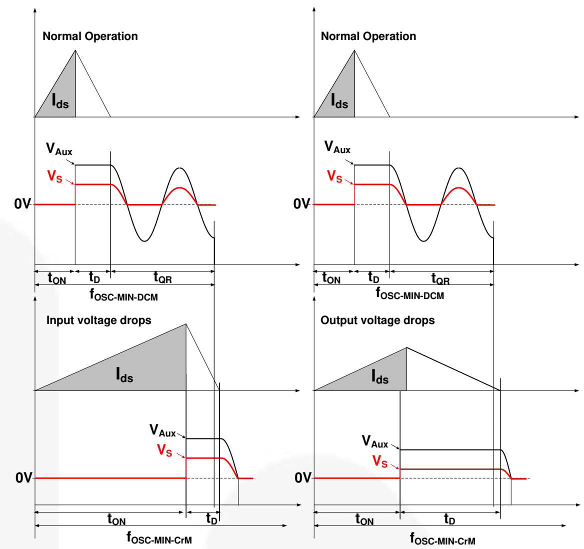


Figure 41. CCM Prevention Behavior

HV Startup and Brown-In

Figure 42 shows the high-voltage (HV) startup circuit. An Internal JFET provides a high voltage current source, whose characteristics are shown in Figure 43. To improve reliability and surge immunity, it is typical to use a R_{HV} resistor between the HV pin and the bulk capacitor voltage. The actual current flowing into the HV pin at a given bulk capacitor voltage and startup resistor value is determined by the intersection point of characteristics I-V line and the load line as shown in Figure 43.

During startup, the internal startup circuit is enabled and the bulk capacitor voltage supplies the current, I_{HV}, to charge the hold-up capacitor, C_{VDD}, through R_{HV}. When the V_{DD} voltage reaches $V_{DD\text{-}ON}$, the sampling circuit shown in Figure 42 is turned on for $t_{HV\text{-}det}$ (100 µs) to sample the bulk capacitor voltage. Voltage across R_{LS} is compared with reference which generates a signal to start switching. If brown-in condition is not detected within this time, switching does not start. Equation (9) can be used to program the brown-in of the system. If line voltage is lower than the programmed brown-in voltage, FAN602F goes in auto-restart mode.

$$V_{IN} = \frac{R_{LS} + R_{JEFT} + R_{HV}}{R_{LS}} \times V_{REF} \qquad (9)$$

Once switching starts, the internal HV startup circuit is disabled. During normal switching, the line voltage information is obtained from the I_{VS} signal. Once the HV startup circuit is disabled, the energy stored in C_{VDD} supplies the IC operating current until the transformer auxiliary winding voltage reaches the nominal value. Therefore, C_{VDD} should be properly designed to prevent V_{DD} from dropping below $V_{DD\text{-}OFF}$ threshold (typically 5.5 V) before the auxiliary winding builds up enough voltage to supply V_{DD}. During startup, the IC current is limited to $I_{DD\text{-}ST}$ (300 µA).

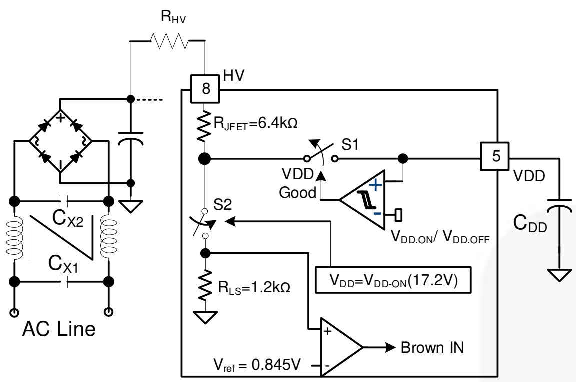


Figure 42. HV Startup Circuit

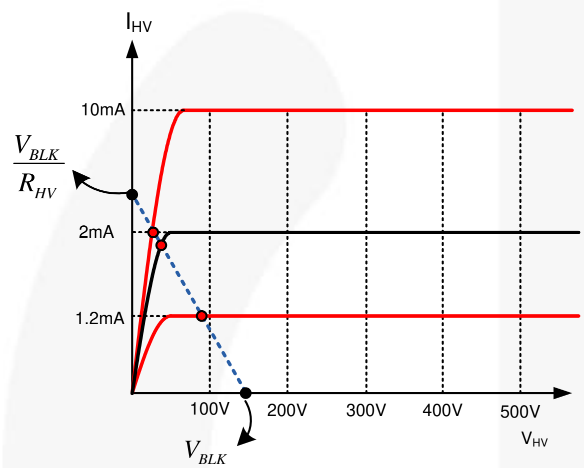


Figure 43. Characteristics of HV pin

Protections

The FAN602F protection functions include VDD Over-Voltage Protection (VDD-OVP), brownout protection, VS Over-Voltage Protection (VS-OVP), VS Under-Voltage Protection (VS-UVP), and IC internal Over-Temperature Protection (OTP). The VDD-OVP, brownout protection VS-OVP and OTP are implemented with Auto-Restart mode. The VS-UVP is implemented with Extend Auto-Restart mode.

When the Auto-Restart Mode protection is triggered, switching is terminated and the MOSFET remains off, causing VDD to drop because of IC operating current $I_{DD\text{-}OP}$ (2 mA). When VDD drops to the VDD turn-off voltage of $V_{DD\text{-}OFF}$ (5.5 V), operation current reduces to $I_{DD\text{-}Deep\text{-}Burst}$ (300 μA). When the VDD voltage drops further to $V_{DD\text{-}HV\text{-}ON}$, the protection is reset and the supply current drawn from HV pin begins to charge the VDD hold-up capacitor. When VDD reaches the turn-on voltage of $V_{DD\text{-}ON}$ (17.2 V), the FAN602F resumes normal operation. In this manner, the Auto-Restart mode alternately enables and disables the switching of the MOSFET until the abnormal condition is eliminated as shown in Figure 44.

When the Extend Auto-Restart Mode protection is triggered via VS under-voltage protection (VS-UVP), switching is terminated and the MOSFET remains off, causing VDD to drop. While V_{DD} drops to $V_{DD\text{-}HV\text{-}ON}$ for HV startup circuit enable, then IC enters Extend Auto-Restart period with two cycles as shown Figure 45. During Extend Auto-Restart period, VDD voltage swings between $V_{DD\text{-}ON}$ and $V_{DD\text{-}HVON}$ without gate switching, and IC operation current is reduced to $I_{DD\text{-}Burst}$ of 300 μA for slowing down the VDD capacitor discharging slope. As Extend Auto-Restart period ends, normal operation resumes.

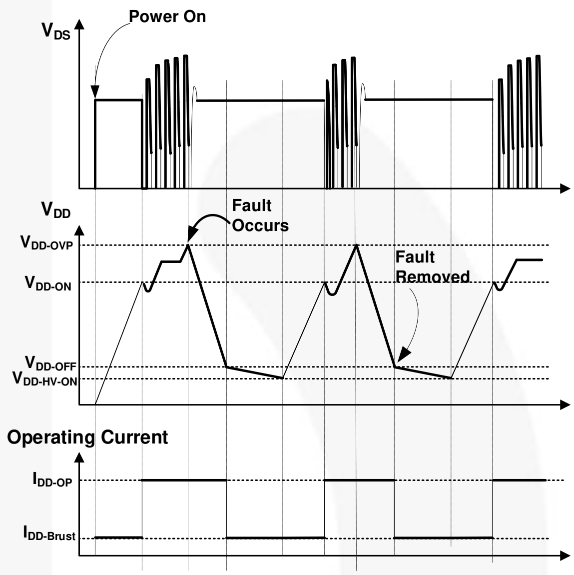


Figure 44. Auto-Restart Mode Operation

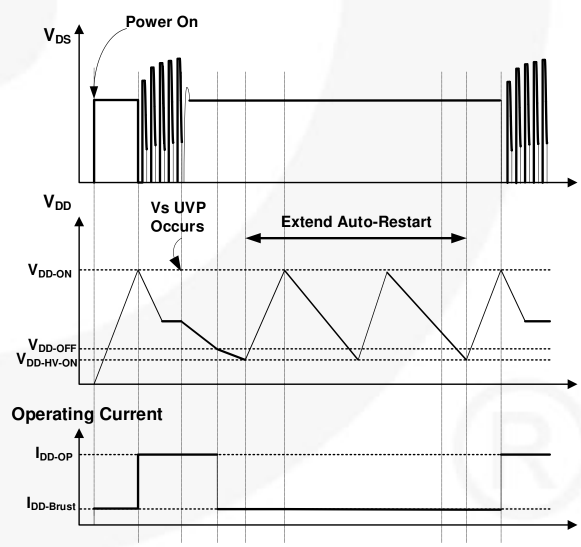


Figure 45. Extend Auto-Restart Mode Operation

VDD Over-Voltage-Protection (VDD-OVP)

VDD over-voltage protection prevents IC damage from over-voltage stress. It is operated in Auto-Restart mode. When the VDD voltage exceeds $V_{DD\text{-}OVP}$ (29.0 V) for the de-bounce time, $t_{D\text{-}VDDOVP}$ (70 µs), due to abnormal condition, the protection is triggered. This protection is typically caused by an open circuit of secondary side feedback network.

Brownout Protection

Line voltage information is also used for brownout protection. When the I_{VS} current out of the VS pin during the MOSFET conduction time is less than 450 µA for longer than 16.5 ms, the brownout protection is triggered. The input bulk capacitor voltage to trigger brownout protection is given as

$$V_{BLK.BO} = 450\mu \cdot \frac{R_{VS1}}{N_A/N_P} \tag{10}$$

IC Internal Over-Temperature-Protection (OTP)

The internal temperature-sensing circuit disables the PWM output if the junction temperature exceeds 140°C (T_{OTP}) and the FAN602F enters Auto-Restart Mode protection.

VS Over-Voltage-Protection (VS-OVP)

VS over-voltage protection prevents damage caused by output over-voltage condition. It is operated in Auto-Restart mode. Figure 46 shows the internal circuit of VS-OVP protection. When abnormal system conditions occur, which cause VS sampling voltage to exceed $V_{VS\text{-}OVP}$ (2.9V) for more than 2 consecutive switching cycles ($N_{VS\text{-}OVP}$), PWM pulses are disabled and FAN602F enters Auto-Restart protection. VS over-voltage conditions are usually caused by open circuit of the secondary side feedback network or a fault condition in the VS pin voltage divider resistors. For VS pin voltage divider design, R_{VS1} is obtained from Equation (10), and R_{VS2} is determined by the desired VS-OVP protection function as

$$R_{VS2} = R_{VS1} \cdot \frac{1}{\frac{V_{O-OVP}}{V_{VS-OVP}} \cdot \frac{N_A}{N_S} - 1} \tag{11}$$

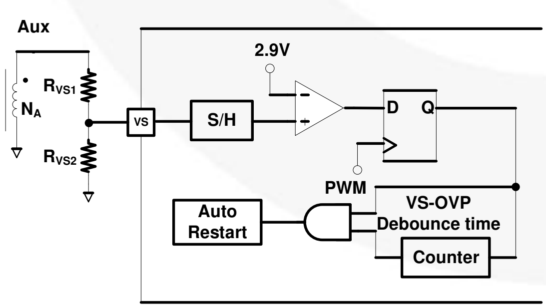


Figure 46. VS-OVP Protection Circuit

VS Under-Voltage-Protection (VS-UVP)

In the event of an output short, output voltage will drop and the primary peak current will increase. To prevent operation for a long time in this condition, FAN602F incorporates under-voltage protection through VS pin. Figure 47 shows the internal circuit for VS-UVP. By sampling the auxiliary winding voltage on the VS pin at the end of diode conduction time, the output voltage is indirectly sensed. When V_S sampling voltage is less than $V_{VS\text{-}UVP}$ (0.65 V) and longer than de-bounce cycles $N_{VS\text{-}UVP}$, VS-UVP is triggered and the FAN602F enters Extend Auto-Restart Mode.

To avoid VS-UVP triggering during the startup sequence, a startup blanking time, $t_{VS\text{-}UVP\text{-}BLANK}$ (45 ms), is included for system power on. For VS pin voltage divider design, R_{VS1} is obtained from Equation (10) and R_{VS2} is determined by Equation (11). $V_{O\text{-}UVP}$ can be determined by Equation (12).

$$V_{O-UVP} = \frac{N_S}{N_A} \cdot \left(1 + \frac{R_{VS1}}{R_{VS2}}\right) \cdot V_{VS-UVP} \tag{12}$$

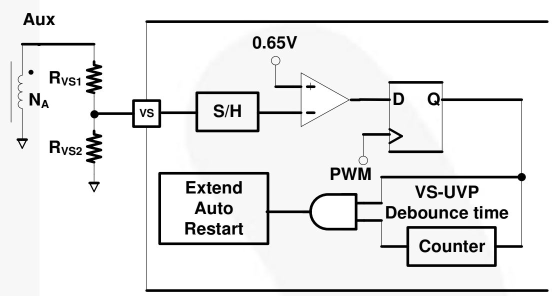


Figure 47. VS-UVP Protection Circuit

Externally Triggered Shutdown (SD)

By pulling down SD pin voltage below a threshold voltage $V_{SD\text{-}TH}$ (1.0 V), shutdown can be externally triggered and the FAN602F will enter into Auto-Restart mode protection. It can be also used for external Over-Temperature-Protection by connecting a NTC thermistor between the shutdown (SD) programming pin and ground. An internal constant current source I_{SD} (103 µA) creates a voltage drop across the thermistor. The resistance of the NTC thermistor becomes smaller as the ambient temperature increases, which reduces the voltage drop across the thermistor.

SD pin voltage is sampled every gate cycle when $V_{FB} > V_{FB\text{-}Burst\text{-}H}$ and sampled continuously when $V_{FB} < V_{FB\text{-}Burst\text{-}L}$. When the voltage at SD pin is sampled to be below the threshold voltage, $V_{SD\text{-}TH}$ (1.0 V), for a de-bounce time of $t_{D\text{-}SD}$ (400 µs), Auto-Restart protection is triggered. A capacitor may also be placed in parallel with the NTC thermistor to further improve the noise immunity. The capacitor should be designed such that SD pin voltage is more than $V_{SD\text{-}TH}$ within the time period of $t_{D\text{-}SD}$.

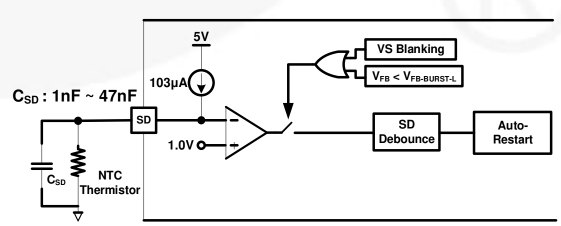


Figure 48. External OTP using SD Pin

Pulse-by-Pulse Current Limit

During startup or overload condition, the feedback loop is saturated to high and is unable to control the primary peak current. To limit the current during such conditions, FAN602F has pulse-by-pulse current limit protection which forces the GATE to turn off when the CS pin voltage reaches the current limit threshold, $V_{CS\text{-}LIM}$ (0.9 V).

Secondary-Side Diode Shot Protection

When the secondary-side diode is damaged, the slope of the primary-side peak current will be sharp within leading-edge blanking time. To limit the current during such conditions, FAN602F has secondary-side diode short protection which forces the GATE to turn off when the CS pin voltage reaches 1.6 V. After one switching cycle, it will operate in Auto-Restart mode as shown in Figure 49.

Current Sense Short Protection

Current sense short protection prevents damage caused by CS pin open or short to ground. After two switching cycle, it will operate in Auto-Restart mode. Figure 49 shows the internal circuit of current sense short protection. When abnormal system conditions occur, which cause CS pin voltage lower than 0.2 V after debounce time ($t_{CS\text{-}short}$) for more than 2 consecutive switching cycles, PWM pulses are disabled and FAN602F enters Auto-Restart protection. The $I_{CS\text{-}Short}$ is an internal current source, which is proportional to line voltage. The debounce time ($t_{CS\text{-}short}$) is created by $I_{CS\text{-}short}$, capacitor (2 pF) and threshold voltage (2.4 V). This debounce time ($t_{CS\text{-}short}$) is inversely proportional to the DC link capacitor voltage, V_{BLK}.

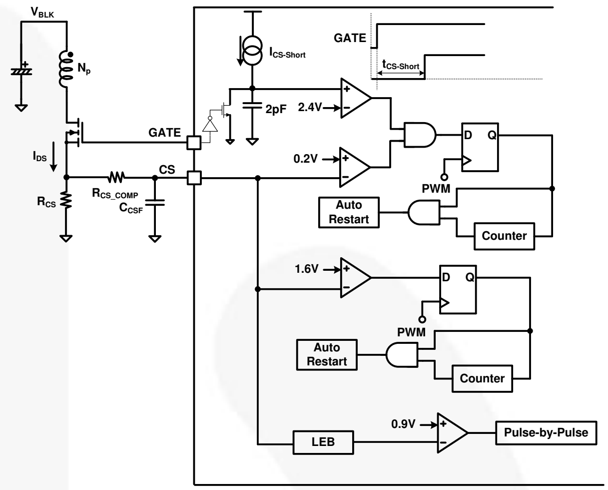
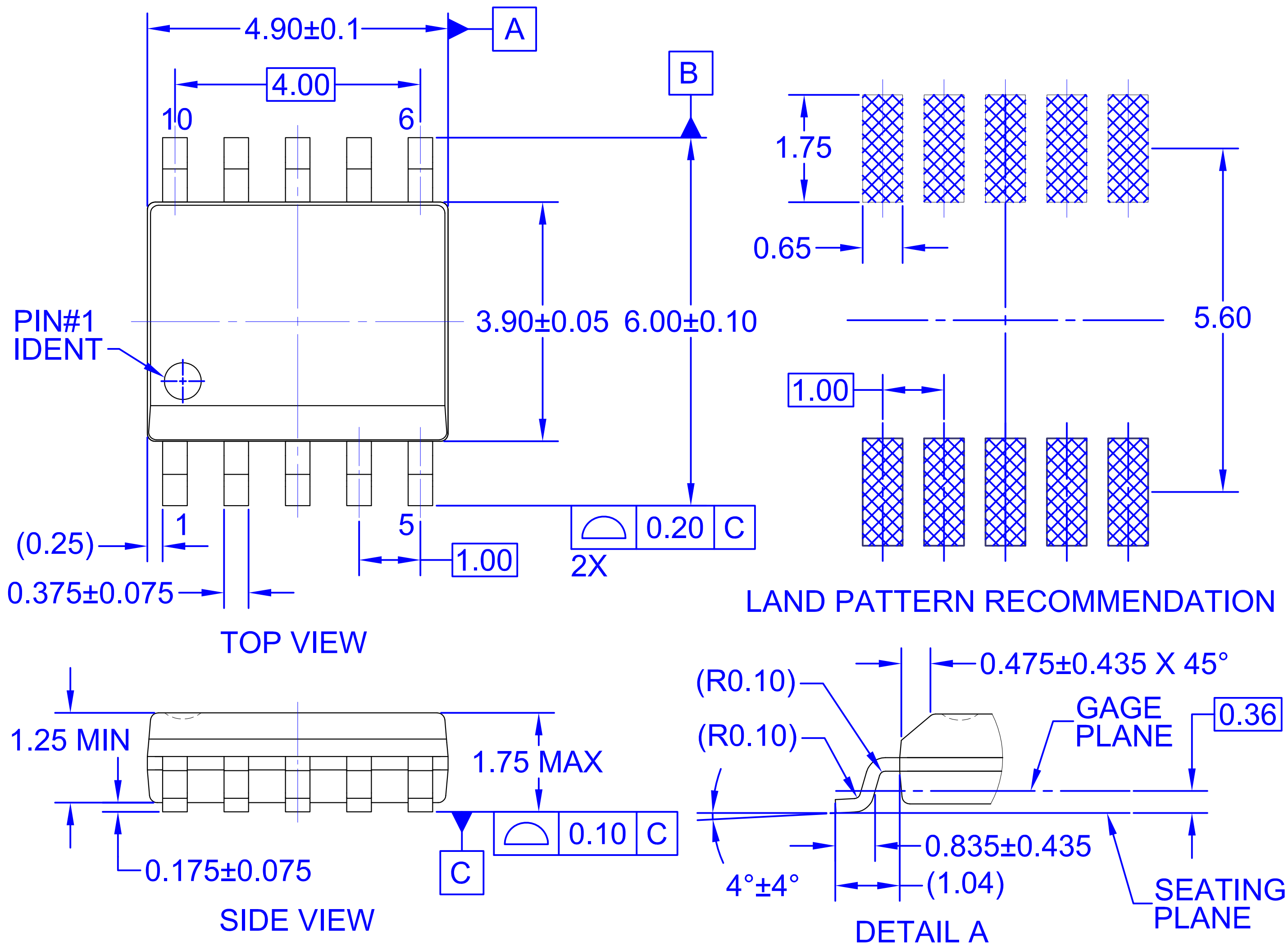
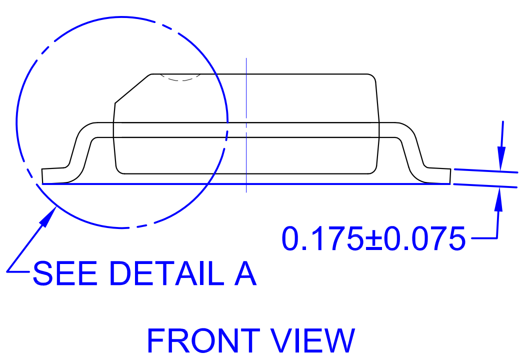


Figure 49. Current Sense Protection Circuit





NOTES:

A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MS-012.

B. ALL DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

D. LAND PATTERN STANDARD: SOIC127P600X175.10M

E. DRAWING FILENAME: MKT-M10ArevB

ON Semiconductor

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative