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FAN7085_GF085 High Side Gate Driver with Recharge FET

Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation fully operational up to 300V.
- Tolerance to negative transient voltage on VS pin
- dv/dt immune.
- Gate drive supply range from 4.5V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down and pull-up
- High side output out of phase with input (Inverted input)
- Reset input
- Internal recharge FET for bootstrap refresh

Typical Applications

- Diesel and gasoline injectors/valves
- MOSFET-and IGBT high side driver applications



For Fairchild's definition of "green" Eco Status, please visit:
http://www.fairchildsemi.com/company/green/rohs_green.html

Description

The FAN7085_GF085 is a high-side gate drive IC with reset input and built-in recharge FET. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 300V. Fairchild's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dV/dt noise circumstances. Logic input is compatible with standard CMOS outputs. The UVLO circuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 250mA and 250mA. Built-in recharge FET to refresh bootstrap circuit is very useful for circuit topology requiring switches on low and high side of load.

SOIC-8

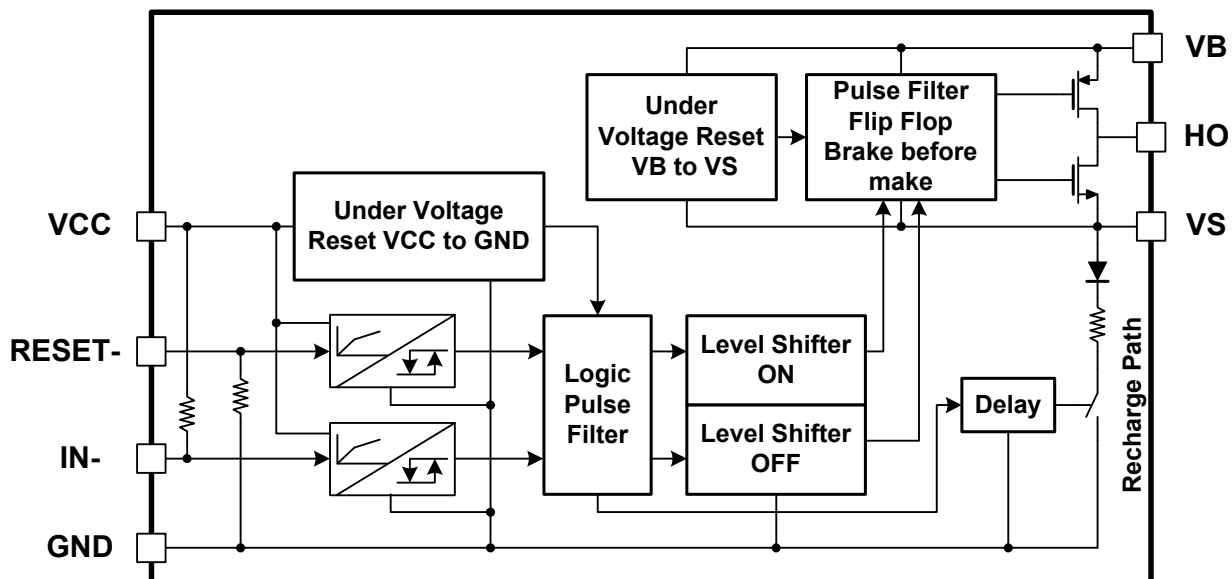


Ordering Information

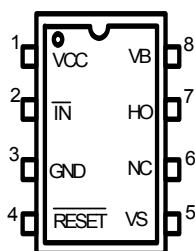
| Device | Package | Operating Temp. |
|-----------------|---------|-----------------|
| FAN7085M_GF085 | SOIC-8 | -40 °C ~ 125 °C |
| FAN7085MX_GF085 | SOIC-8 | -40 °C ~ 125 °C |

X : Tape & Reel type

Block Diagrams



Pin Assignments



Pin Definitions

| Pin Number | Pin Name | I/O | Pin Function Description |
|------------|----------|-----|--|
| 1 | VCC | P | Driver supply voltage, typically 5V |
| 2 | IN- | I | Driver control signal input (Negative Logic) |
| 3 | GND | P | Ground |
| 4 | RESET- | I | Driver enable input signal (Negative Logic) |
| 5 | VS | P | High side floating offset for MOSFET Source connection |
| 6 | NC | - | No connection (No Bond wire) |
| 7 | HO | A | High side drive output for MOSFET Gate connection |
| 8 | VB | P | Driver output stage supply |

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND.

| Parameter | Symbol | Min. | Max. | Unit |
|--|------------------|--------|---------|------|
| High side floating supply voltage | VBS | -0.3 | 25 | V |
| High side driver output stage voltage Neg. transient: 0.5 ms, external MOSFET off | VB | -5 | 325 | V |
| High side floating supply offset voltage Neg. transient 0.2 us | Vs | -25 | 300 | V |
| High side floating output voltage | VHO | VS-0.3 | VB+0.3 | V |
| Supply voltage | VCC | -0.3 | 25 | V |
| Input voltage for IN- | VIN | -0.3 | Vcc+0.3 | V |
| Input voltage for RESET- | VRES | -0.3 | Vcc+0.3 | V |
| Power Dissipation ¹⁾ | Pd | | 0.625 | W |
| Thermal resistance, junction to ambient ¹⁾ | Rthja | | 200 | °C/W |
| Electrostatic discharge voltage (Human Body Model) | V _{ESD} | 1.5K | | V |
| Charge device model | V _{CDM} | 500 | | V |
| Junction Temperature | T _J | | 150 | °C |
| Storage Temperature | T _S | -55 | 150 | °C |

Note: 1) The thermal resistance and power dissipation rating are measured below conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural condition(StillAir)

JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. -40°C ≤ Ta ≤ 125°C

| Parameter | Symbol | Min. | Max. | Unit |
|---|-----------------------|--------|-------|------|
| High side floating supply voltage(DC) Transient:-10V@ 0.2 us | VB | VS+4.5 | VS+20 | V |
| High side floating supply offset voltage(DC) @VBS=7V | VS | -3 | 300 | V |
| High side floating supply offset voltage(Transient) 0.2us @VBS<25V | VS | -25 | 300 | V |
| High side floating output voltage | VHO | Vs | VB | V |
| Allowable offset voltage Slew Rate ¹⁾ | dv/dt | - | 50 | V/ns |
| Supply voltage for logic part | VCC | 4.5 | 20 | V |
| Input voltage for IN- | VIN | 0 | Vcc | V |
| Input voltage for RESET- | VRESET | 0 | Vcc | V |
| Switching frequency ²⁾ | Fs | | 200K | Hz |
| Minimum low input width ³⁾ | tIN(low,min) | 560 | - | ns |
| Minimum high input width ³⁾ | tIN(high,min) | 60 | - | ns |
| Minimum operating voltage of VB related to GND | VB(MIN) ⁴⁾ | 4 | - | V |
| Ambient temperature | Ta | -40 | 125 | °C |

Note: 1) Guaranteed by design.

2) Duty = 0.5, VBS ≥ 7V

3) Guaranteed by design. Pulse widths below the specified values, may be ignored. Output will either follow the input signal or will ignore it.

No false output state is guaranteed when minimum input width is smaller than tin

4) Guaranteed by design

Statics Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, $V_{BS} = 7\text{V}$, $V_S = 0\text{V}$, $V_{RESET} = 5\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|------------------|--|------------|------|----------|------------|
| VCC and VBS Supply Characteristics | | | | | | |
| VCC and VBS supply under voltage positive going threshold | VCCUV+ VBSUV+ | VCC and VBS rising from 0V | - | 3.7 | 4.3 | V |
| VCC and VBS supply under voltage negative going threshold | VCCUV- VBSUV- | VCC and VBS dropping from 5V | 2.8 | 3.4 | - | V |
| VCC and VBS under voltage hysteresis | VCCUVH VBSUVH | - | 0.02 | 0.3 | - | V |
| Under voltage lockout response time | tduvcc tduvbs | VCC: 6.5V->2.4V or 2.4V->6.5V VBS: 6.5V->2.4V or 2.4V->6.5V | 0.5 0.5 | | 20 20 | us us |
| Offset supply leakage current | ILK | VB=VS=300V | - | - | 200 | uA |
| Quiescent Vcc supply current | IQCC | VCC=20V | - | - | 500 | uA |
| Quiescent VBS supply current | IQBS1 | Static mode, VBS=7V, VIN=0 or 5V | | | 100 | uA |
| Quiescent VBS supply current | IQBS2 | Static mode, VBS=16V, VIN=0 or 5V | | | 200 | uA |
| VBS drop due to output turn-on (Design guaranty) | ΔV_{BS} | VBS=7V, Cbs=1uF, tdiG-IN=3uS, tTEST=100uS | | | 210 | mV |
| Input Characteristics | | | | | | |
| High logic level input voltage for IN- | VIH | | 0.6VCC | - | - | V |
| Low logic level input voltage for IN- | VIL | | - | - | 0.28VCC | V |
| Low logic level input bias current for IN- | IIN- | VIN=0 | 5 | 25 | 60 | uA |
| High logic level input bias current for IN- | IIN+ | VIN=5V | - | - | 5 | uA |
| Full up resistance at IN | RIN | | 83 | 200 | 1000 | K Ω |
| High logic level input voltage for RESET- | VRH | | 0.6Vcc | - | - | V |
| Low logic level input voltage for RESET- | VRL | | | | 0.28Vcc | V |
| High logic level input current for RESET- | IRES+ | VRESET=5V | 5 | 25 | 60 | uA |
| Low logic level input bias current for RESET- | IRES- | VRESET=0 | | | 5 | uA |
| Full down resistance at RESET- | RRES | | 83 | 200 | 1000 | K Ω |
| Output characteristics | | | | | | |
| High level output voltage, VB - VHO | VOH | IO=0 | - | - | 0.1 | V |
| Low level output voltage, VHO-GND | VOL | IO=0 | - | - | 0.1 | V |
| Peak output source current | IO+ | VIN=5V | 250 | 450 | - | mA |
| Peak output sink current | IO- | VIN=0 | 250 | 450 | - | mA |
| Equivalent output resistance | ROP | | | 15.5 | 28 | Ω |
| | RON | | | 15.5 | 28 | Ω |
| Recharge Characteristics | | | | | | |
| Recharge TR turn-on propagation delay | Ton_rech | | 4 | 7.9 | 9.8 | us |
| Recharge TR turn-off propagation delay | Toff_rech | | | 0.2 | 0.4 | us |
| Recharge TR on-state voltage drop | VRECH | Is=1mA, VIN=5V @125°C | | | 1.2 | V |
| Dead Time Characteristics | | | | | | |
| High side turn-off to recharge gate turn-on | DTHOFF | VCC=5V, VS=7V | 4 | 7.8 | 9.8 | us |
| Recharge gate turn-off to high side turn-on | DTHON | VCC=5V, VS=7V | 0.1 | 0.4 | 0.7 | us |

Note: The input parameter are referenced to GND. The VO and IO parameters are referenced to GND.

Dynamic Electrical Characteristics

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, $V_{BS} = 7\text{V}$, $V_S = 0\text{V}$, $V_{RESET} = 5\text{V}$, $R_L = 50\Omega$, $C_L = 2.5\text{nF}$.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|----------------------|---|------|------|------|------|
| Input-to-output turn-on propagation delay | t _{plh} | 50% input level to 10% output level, V _S = 0V | | 0.56 | 1 | us |
| Input-to-output turn-off propagation delay | t _{phl} | 50% input level to 90% output level V _S = 0V | - | 0.15 | 0.5 | us |
| RESET-to-output turn-off propagation delay | t _{phl_res} | 50% input level to 90% output level | - | 0.17 | 0.5 | us |
| RESET-to-output turn-on propagation delay | t _{plh_res} | 50% input level to 10% output level | - | 0.56 | 1 | us |
| Output rising time | tr1 | T _j =25°C | - | 65 | 200 | ns |
| | tr2 | | | - | 400 | ns |
| | tr3 | T _j =25°C, V _{BS} =16V | | 65 | 200 | ns |
| | tr4 | V _{BS} =16V | | - | 400 | ns |
| Output falling time | tf1 | T _j =25°C | - | 25 | 200 | ns |
| | tf2 | | | - | 300 | ns |
| | tf3 | T _j =25°C, V _{BS} =16V | | 25 | 200 | ns |
| | tf4 | V _{BS} =16V | | - | 300 | ns |

Application Information

1. Logic Tables

| VCC | VBS | RESET- | IN- | Ho | RechFET |
|------------|------------|--------|------|-----|---------|
| < VCCUVLO- | X | X | X | OFF | ON |
| X | X | LOW | X | OFF | ON |
| X | X | X | HIGH | OFF | ON |
| > VCCUVLO+ | > VBSUVLO+ | HIGH | LOW | ON | OFF |
| > VCCUVLO+ | < VBSUVLO- | HIGH | LOW | OFF | OFF |

Notes:

X means independent from signal

IN=LOW indicates that the high side NMOS is ON

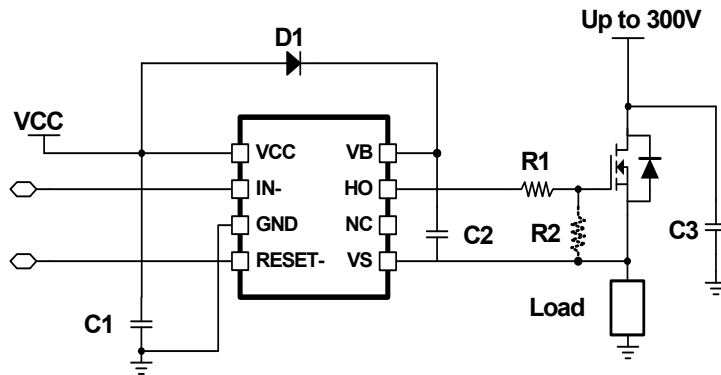
IN=HIGH indicates that the high side NMOS is OFF

RechFET =ON indicates that the recharge MOSFET is ON

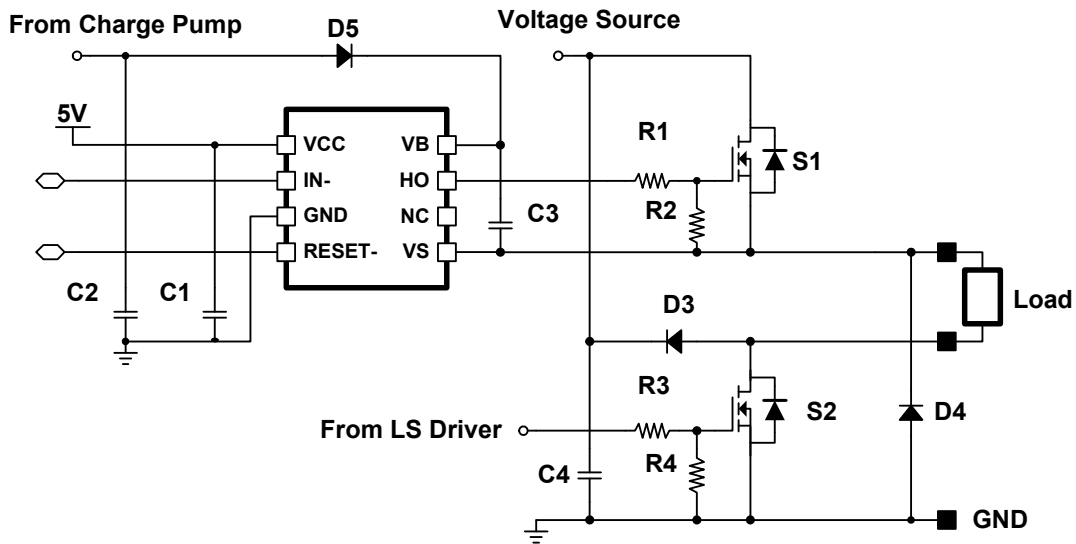
RechFET =OFF indicates that the recharge MOSFET is OFF

Typical Application Circuit

1. Typical Application Circuit



2. Application Example



Input-Output Waveforms

1. Input/Output Timing Diagrams

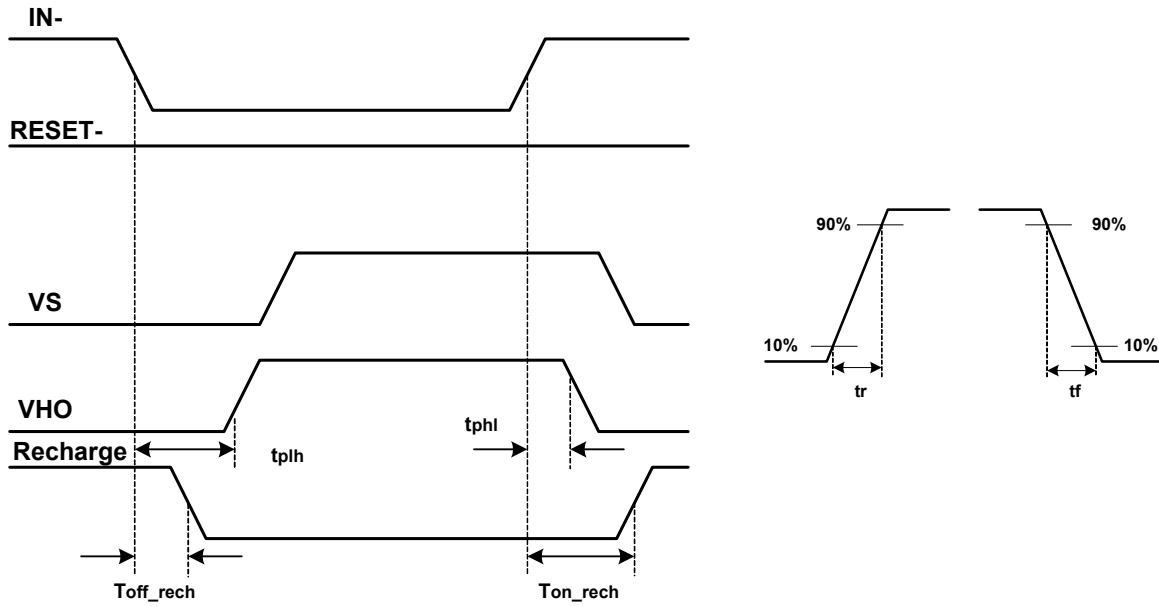


Figure.1 Input and Output Timing Diagram and Switching Time Waveform Definition

2. Reset Timing Diagrams

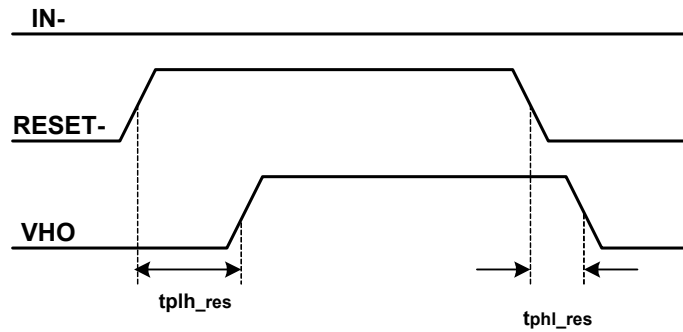


Figure.2 Reset and Output Timing Diagram

3.VB Drop Voltage Diagram

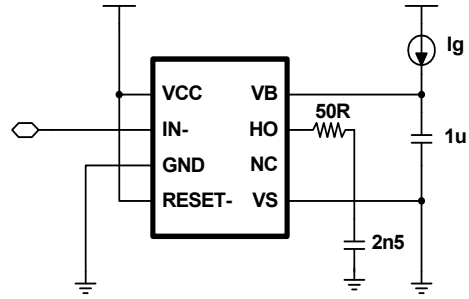
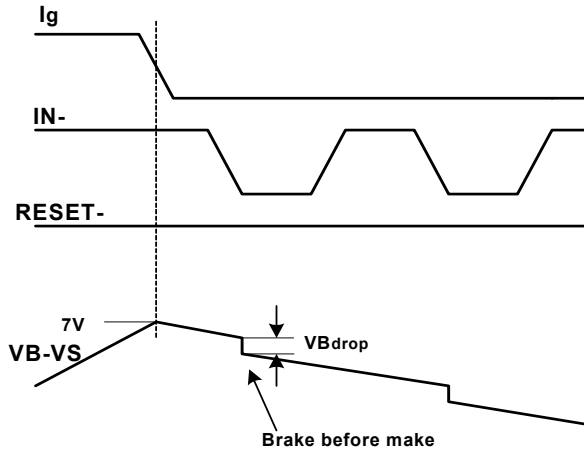


Figure3.b VB Drop Voltage Test Circuit

4.Recommendation Min. Short Pulse Width

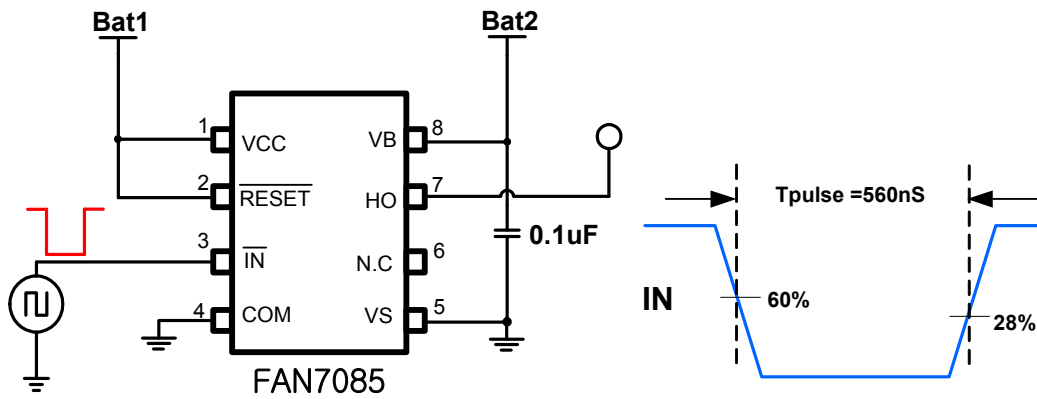


Figure 4a.Short Pulse Width Test Circuit and Pulse Width Waveform

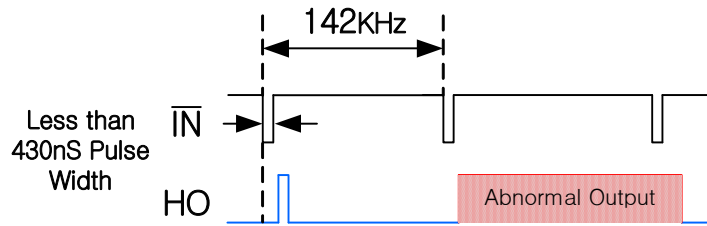


Figure 4b. Abnormal Output Waveform with short pulse width

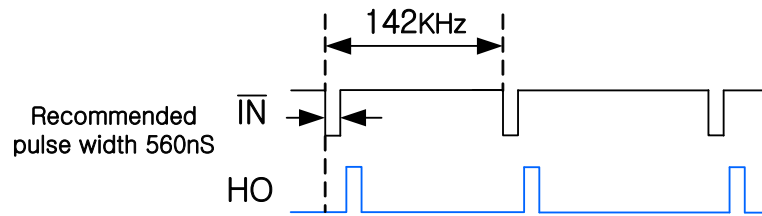


Figure 4c. Recommendation of pulse width Output Waveform

Performance Graphs

This performance graphs based on ambient temperature -40°C ~125°C

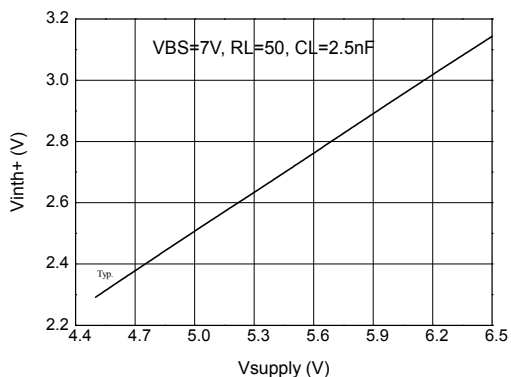


Figure 5a. Positive IN and RESET Threshold vs VCC Supply

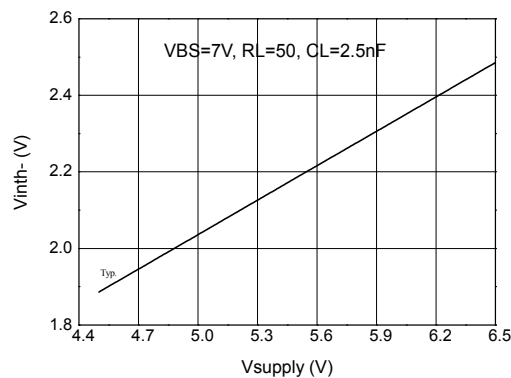


Figure 5b. Negative IN and RESET Threshold vs VCC Supply

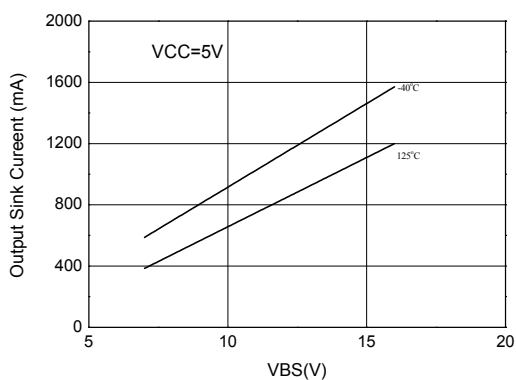


Figure6a. Output Sink Current vs VBS Supply

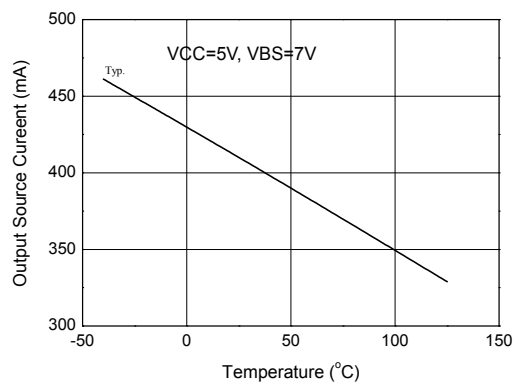


Figure6b. Output Source Current vs Temperature

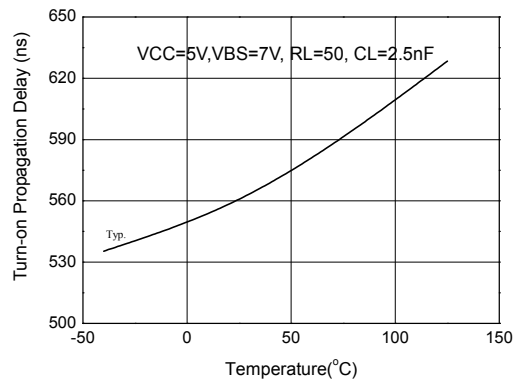


Figure 7a. Turn-On Propagation Delay Time vs Temperature

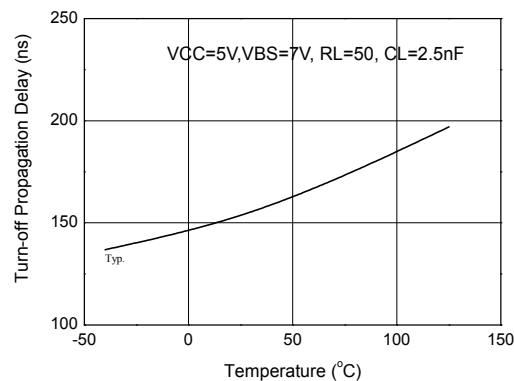


Figure 7b. Turn-Off Propagation Delay Time vs Temperature

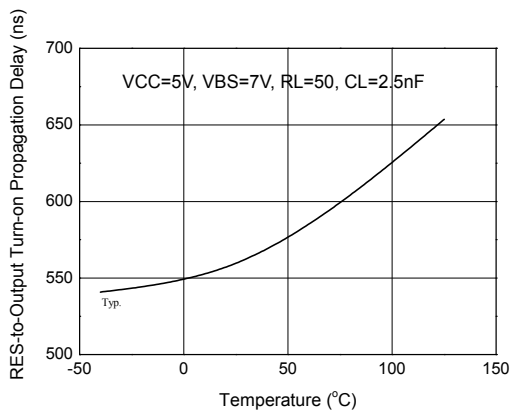


Figure 8a. RES to Output Turn-On Propagation Delay vs Temperature

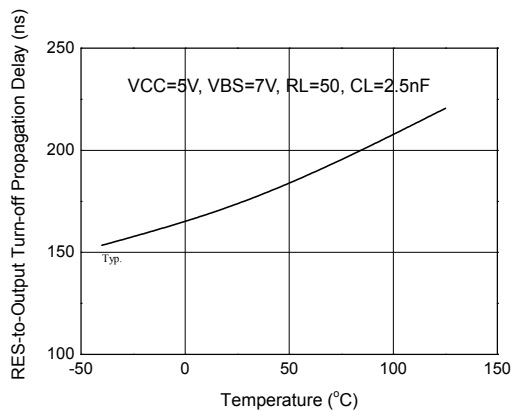


Figure 8b. RES to Output Turn-Off Propagation Delay vs Temperature

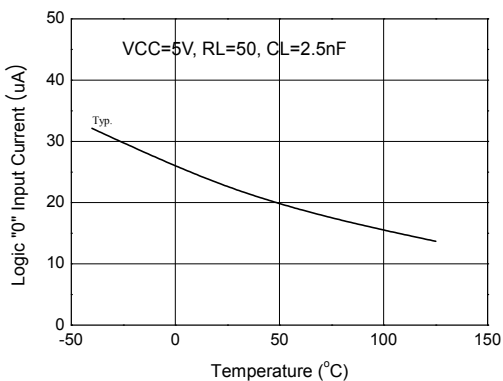


Figure 9. Logic "0" IN Input Current vs Temperature

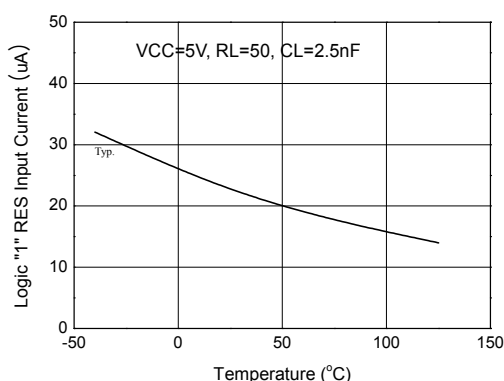


Figure 10. Logic "1" RESET Input Current vs Temperature

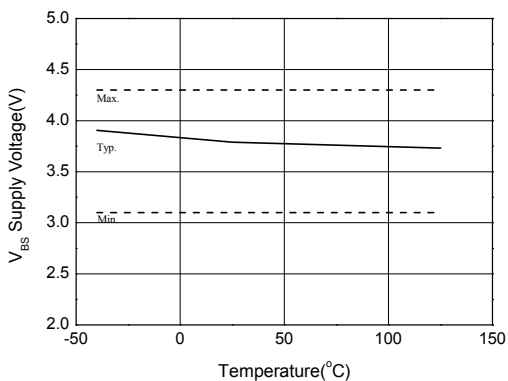


Figure 11a. VBS Under Voltage Threshold(+) vs Temperature

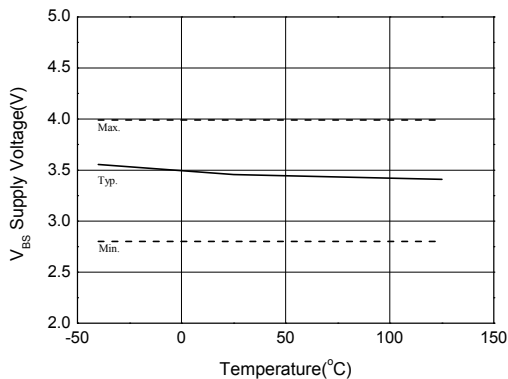


Figure 11b. VBS Under Voltage Threshold(-) vs Temperature

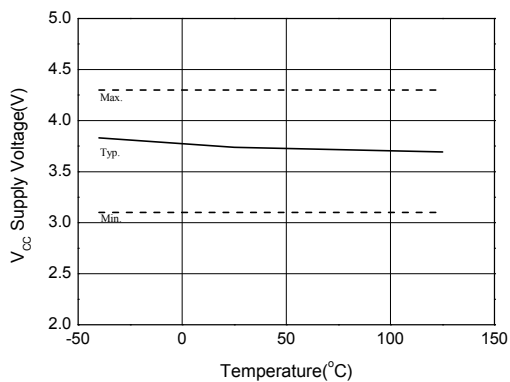


Figure 12a. VCC Under Voltage Threshold(+) vs Temperature

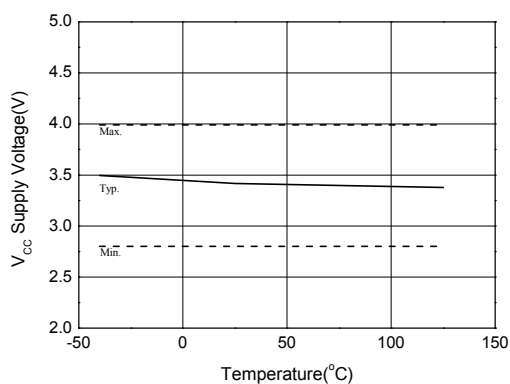


Figure 12b. VCC Under Voltage Threshold(-) vs Temperature

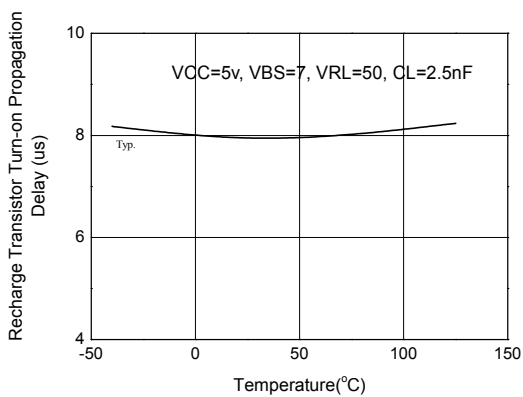


Figure 13. Recharge FET Turn-on Delay time

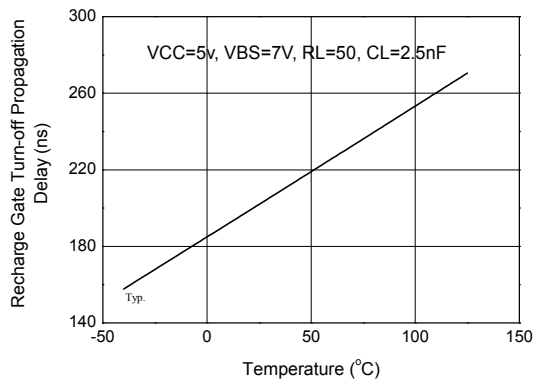


Figure 14. Recharge FET Turn-off Delay time

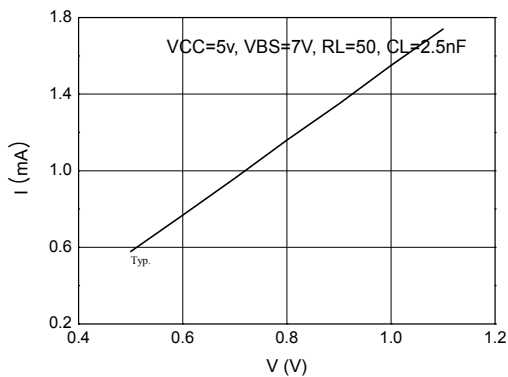


Figure 15. Recharge FET I-V curve

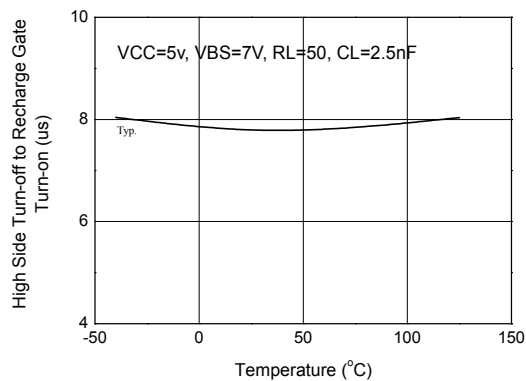
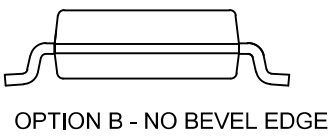
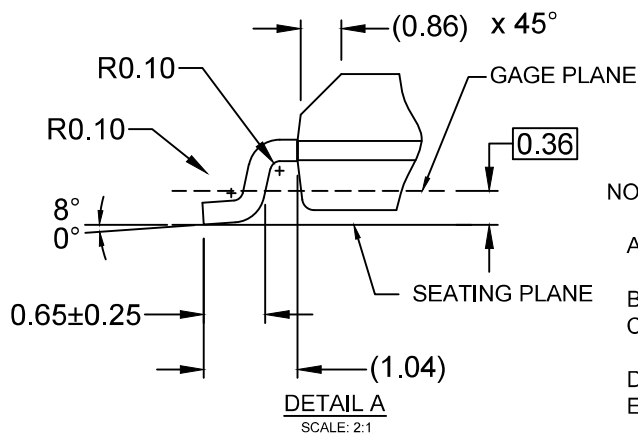
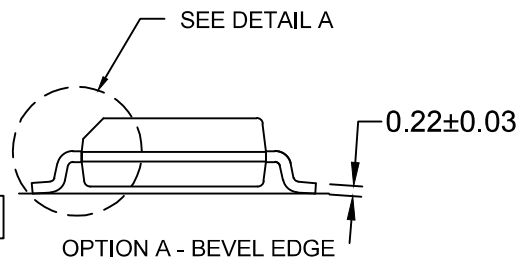
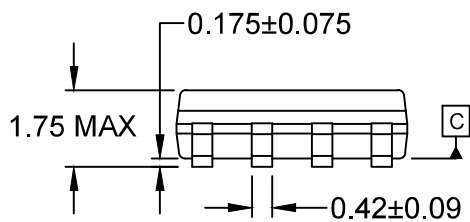
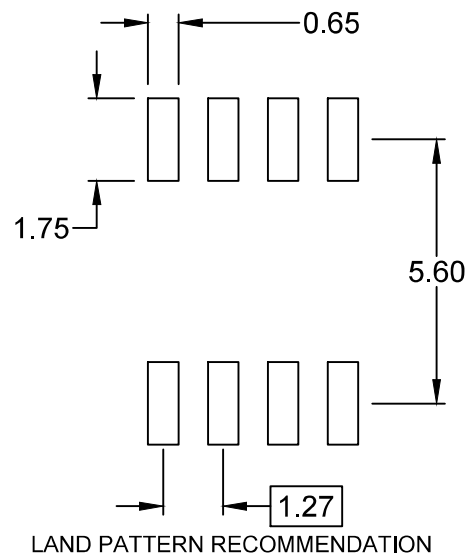
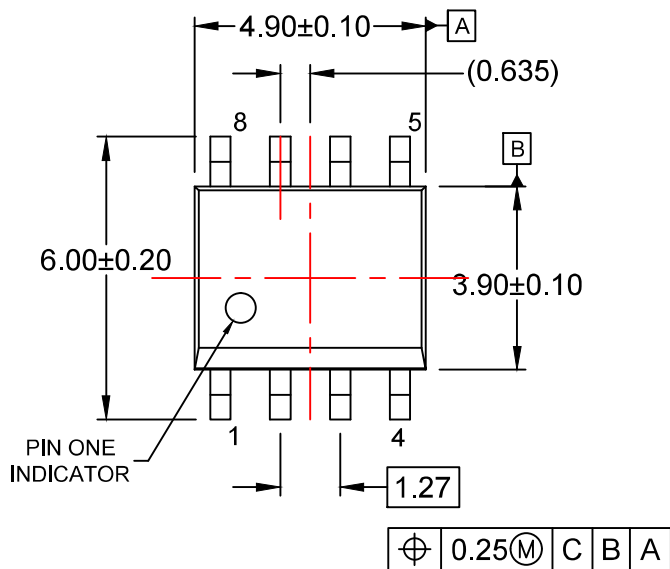


Figure 16. High Side Turn-off to Recharge FET turn-on VS Temperature



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16



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