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November 2009

FAN7361, FAN7362 High-Side Gate Driver

Features

- Floating Channel Designed for Bootstrap Operation to +600V
- Typically 250mA/500mA Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- V_{CC} & V_{BS} Supply Range from 10V to 20V
- UVLO Function for V_{BS}
- Output In-phase with Input Signal
- 8-SOP

Applications

- PDP Scan Driver
- Motor Control
- SMPS
- Electronic Ballast

Description

The FAN7361/FAN7362, a monolithic high-side gate drive IC, can drive MOSFETs and IGBTs that operate up to +600V. Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit offers high-side gate driver operation up to V_S =-9.8V(typ.) for V_{BS} =15V.

The UVLO circuit prevents malfunction when V_{BS} is lower than the specified threshold voltage. Output drivers typically source/sink 250mA/500mA, respectively, which is suitable for fluorescent lamp ballast, PDP scan driver, motor control, and so on.





Ordering Information

Part Number	Package	Operating Temperature Range	© Eco Status	Packing Method
FAN7361M ⁽¹⁾				Tube
FAN7361MX ⁽¹⁾	8-SOP	40°C 425°C Dalle	Dalle	Tape & Reel
FAN7362M ⁽¹⁾		-40°C ~ 125°C	RoHS Ta	Tube
FAN7362MX ⁽¹⁾				Tape & Reel

Note:

1. These devices passed wave soldering test by JESD22A-111.



For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Circuit

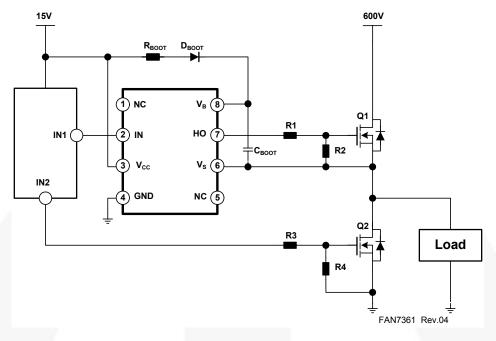


Figure 1. Typical Application Circuit

Internal Block Diagram

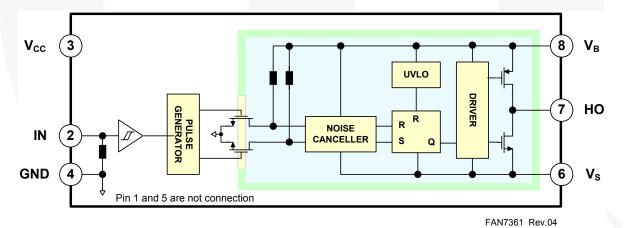


Figure 2. Functional Block Diagram

Pin Assignments

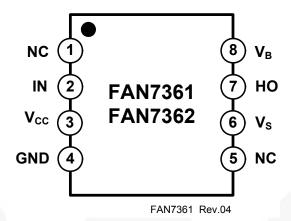


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin	Name	Function/ Description
1	NC	No Connection
2	IN	Logic Input for High-Side Gate Driver Output
3	V _{CC}	Supply Voltage
4	GND	Logic Ground
5	NC	No Connection
6	V _S	High-Voltage Floating Supply Return
7	НО	High-Side Driver Output
8	V _B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}C$, unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V _S	High-Side Offset Voltage	V _B -25	V _B +0.3	
V _B	High-Side Floating Supply Voltage	-0.3	625	
V _{HO}	High-Side Floating Output Voltage	V _S -0.3	V _B +0.3	V
V _{CC}	Logic Fixed Supply Voltage	-0.3	25	
V _{IN}	Logic Input Voltage	-0.3	V _{CC} +0.3	
dV _S /dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
P _D ⁽²⁾⁽³⁾⁽⁴⁾	Power Dissipation		0.625	W
θ_{JA}	Thermal Resistance, Junction-to-Ambient		200	°C/W
T _J	Junction Temperature		+150	°C
T _S	Storage Temperature		+150	°C
T _A	Ambient Temperature	-40	+125	°C

Notes:

- 2. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- 3. Refer to the following standards:
 - JESD51-2: Integral circuits thermal test method environmental conditions Natural convection JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- 4. Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _B	High-Side Floating Supply Voltage	V _S +10	V _S +20	7
Vs	High-Side Floating Supply Offset Voltage	6-V _{CC}	600	
V _{HO}	High-Side Output Voltage	V _S	V _B	V
V _{IN}	Logic Input Voltage GND V _{CC}			
V _{CC}	Logic Supply Voltage	10	20	

Electrical Characteristics

 $V_{BIAS}(V_{CC}, V_{BS})$ =15.0V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to V_S and are applicable to the respective output HO.

Symbol	Characteristics	Test Condi	tion	Min.	Тур.	Max.	Unit
V _{BSUV} +	V _{BS} Supply Under-Voltage Positive Going	V _{BS} =Sweep	FAN7361	8.2	9.2	10.2	
VBSUV'	Threshold	v _{BS} -Sweep	FAN7362	7.6	8.6	9.6	
V	V _{BS} Supply Under-Voltage Negative	V _{BS} =Sweep	FAN7361	7.4	8.6	9.2	V
V _{BSUV} -	Going Threshold	FAN730	FAN7362	7.2	8.2	9.2	\ \ \ \
V= 0.11.0	V _{BS} Supply Under-Current Lockout	V _{BS} =Sweep	FAN7361		0.5		
V _{BSHYS}	Hysteresis	v _{BS} -Sweep	FAN7362		0.4		
I _{LK}	Offset Supply Leakage Current	V _B =V _S =600V				10	
I _{QBS}	Quiescent V _{BS} Supply Current	V _{IN} =0V or 5V			50	80	μA
I _{QCC}	Quiescent V _{CC} Supply Current	V _{IN} =0V	- //		30	75	μΑ
I _{PBS}	Operating V _{BS} Supply Current	C _L =1nF, f=10kHz			420	550	
V	Logic "1" Input Voltage		FAN7361	3.6			
V _{IH}	Logic 1 input voitage		FAN7362	2.9			
V	Logic "0" Input Voltage		FAN7361			1.0	V
V_{IL}	Logic o input voltage	FAN7362	FAN7362			0.8	V
V _{OH}	High Level Output Voltage, V _B -V _{HO}	No load				0.1	
V _{OL}	Low Level Output Voltage, V _{HO}	No load				0.1	
I _{IN+}	Logic "1" Input Bias Current V _{IN} =5V			50	90		
I _{IN-}	Logic "0" Input Bias Current	V _{IN} =0V			1.0	2.0	μA
I _{O+}	Output High Short Circuit Pulse Current	V _{HO} =0V, V _{IN} =5V, PV	V ≤ 10µs	200	250		mΛ
I _{O-}	Output Low Short Circuit Pulse Current V _{HO} =15V, V _{IN} =		W ≤ 10µs	400	500		mA
Vs	Allowable Negative V _S Pin Voltage for IN Signal Propagation to HO				-9.8	-7.0	٧

Dynamic Electrical Characteristics

 $V_{BIAS}(V_{CC}, V_{BS})$ =15.0V, V_{S} =GND, C_{L} =1000pF and T_{A} = 25°C, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
t _{on}	Turn-on Propagation Delay	V _S =0V		120	200	
t _{off}	Turn-off Propagation Delay ⁽⁵⁾	V _S =0V or 600V		90	180	ne
t _r	Turn-on Rise Time			70	160	ns
t _f	Turn-off Fall Time			30	100	

Note:

5. This parameter guaranteed by design.

Typical Characteristics

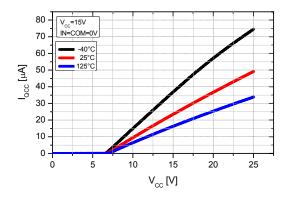


Figure 4. I_{QCC} vs. Supply Voltage

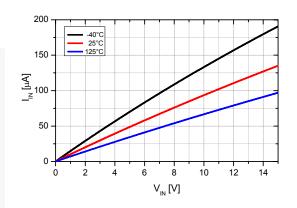


Figure 5. Input Bias Current vs. Input Voltage

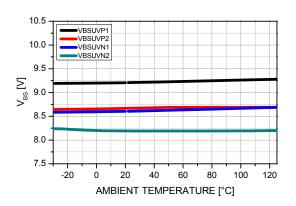


Figure 6. V_{BS} UVLO vs. Temp.

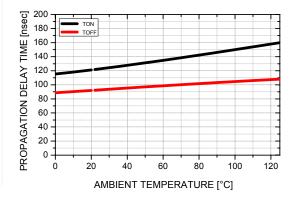


Figure 7. Turn On/Off Propagation Time vs. Temp.

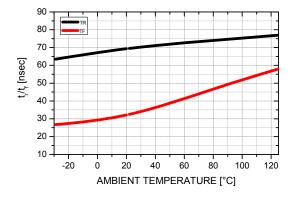


Figure 8. Rising/Falling Time vs. Temp.

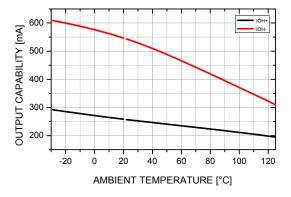


Figure 9. Output Sinking/Sourcing Current vs. Temp.

Switching Time Definition

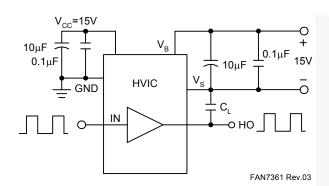


Figure 10. Switching Time Test Circuit

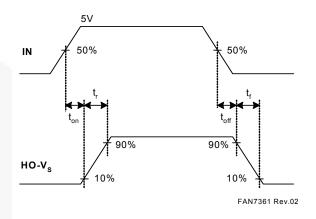
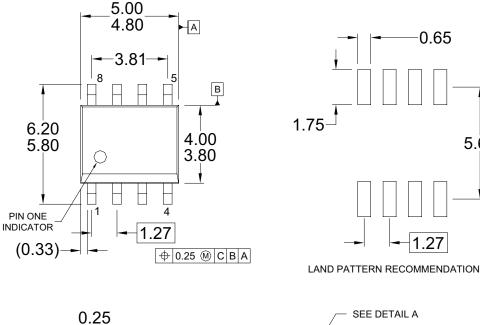
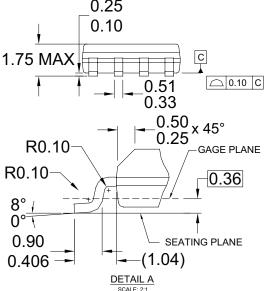


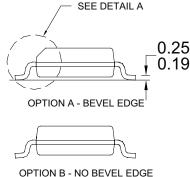
Figure 11. Input / Output Timing Diagram

5.60

Physical Dimensions







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- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
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- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08AREV13

Figure 12. 8-Lead Small Outline Package (SOP)

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