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July 2012

# FAN7390 High-Current, High & Low-Side, Gate-Drive IC

### **Features**

- Floating Channels for Bootstrap Operation to +600V
- Typically 4.5A/4.5A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- Logic (V<sub>SS</sub>) and Power (COM) Ground +/- 7V Offset
- 3.3V and 5V Input Logic Compatible
- Output In-phase with Input

### **Applications**

- PDP Sustain Driver
- HID Lamp Ballast
- SMPS
- Motor Driver

### **Description**

The FAN7390 is a monolithic high- and low-side gatedrive IC, which can drive high speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level shift circuit offers high-side gate driver operation up to  $V_S=-9.8V$  (typical) for  $V_{BS}=15V$ .

The UVLO circuit prevents malfunction when  $V_{DD}$  and  $V_{BS}$  are lower than the specified threshold voltage.

The high current and low output voltage drop feature make this device suitable for the PDP sustain pulse driver, motor driver, switching power supply, and high-power DC-DC converter applications.

8-SOP





### **Ordering Information**

Part Number	Package	Operating Temperature Range	Packing Method
FAN7390MX	8-SOP	-40°C ~ 125°C	Tape & Reel
FAN7390M1X	14-SOP	-40 0 % 125 0	Tape & Reel

# **Typical Application Circuit**

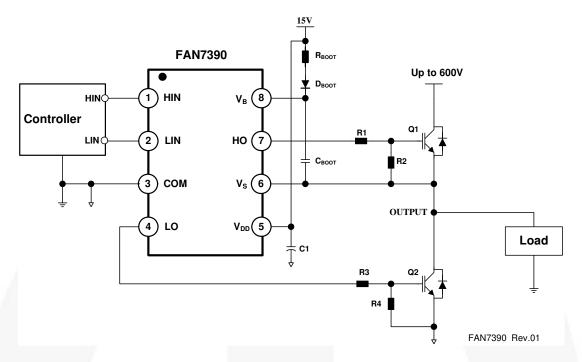


Figure 1. Application Circuit for Half-Bridge (Referenced 8-SOP)

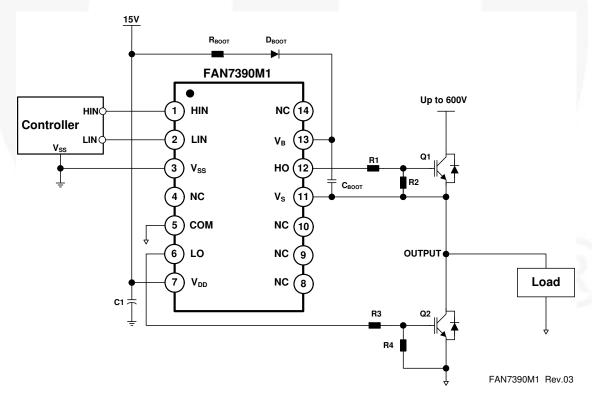


Figure 2. Application Circuit for Half-Bridge (Referenced 14-SOP)

## **Internal Block Diagram**

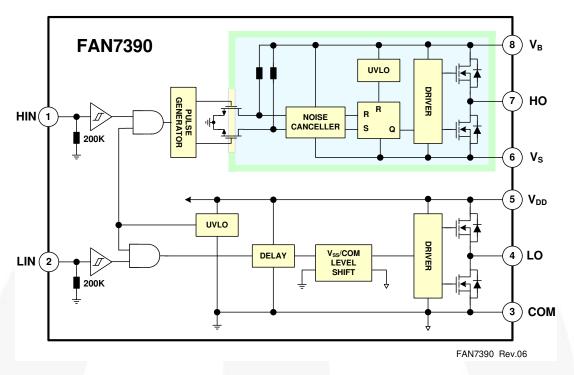


Figure 3. Functional Block Diagram (Referenced 8-SOP)

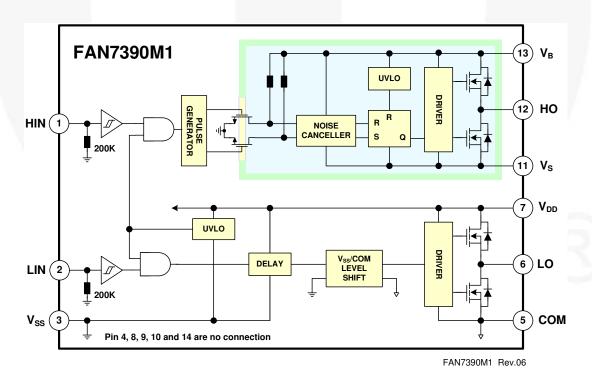


Figure 4. Functional Block Diagram (Referenced 14-SOP)

# **Pin Configurations**

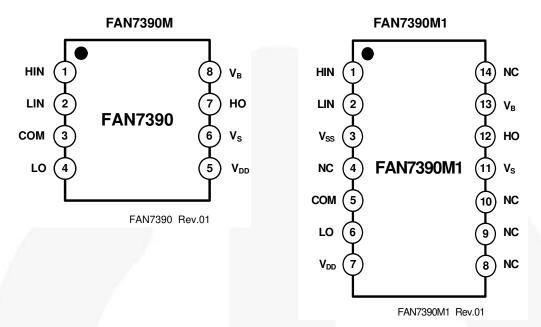


Figure 5. Pin Assignments (Top View)

### **Pin Definitions**

8-Pin	14-Pin	Name	Description	
1	1	HIN	Logic Input for High-Side Gate Driver Output	
2	2	LIN	Logic Input for Low-Side Gate Driver Output	
	3	V <sub>SS</sub>	Logic Ground (FAN7390M1 only)	
3	5	COM	Low-Side Driver Return	
4	6	LO	Low-Side Driver Output	
5	7	$V_{DD}$	Low-Side and Logic Part Supply Voltage	
6	11	V <sub>S</sub>	High-Voltage Floating Supply Return	
7	12	НО	High-Side Driver Output	
8	13	V <sub>B</sub>	High-Side Floating Supply	
	4, 8, 9, 10, 14	NC	No Connect	

### **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}C$ , unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V <sub>S</sub>	High-Side Floating Supply Offset Voltage	V <sub>B</sub> -25	V <sub>B</sub> +0.3	V
V <sub>B</sub>	High-Side Floating Supply Voltage	-0.3	625.0	V
V <sub>HO</sub>	High-Side Floating Output Voltage HO	V <sub>S</sub> -0.3	V <sub>B</sub> +0.3	V
$V_{DD}$	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
$V_{LO}$	Low-Side Output Voltage LO	-0.3	V <sub>DD</sub> +0.3	V
V <sub>IN</sub>	Logic Input Voltage (HIN and LIN)	V <sub>SS</sub> -0.3	V <sub>DD</sub> +0.3	V
V <sub>SS</sub>	Logic Ground (FAN7390M1 only)	V <sub>DD</sub> -25	V <sub>DD</sub> +0.3	V
dV <sub>S</sub> /dt	Allowable Offset Voltage Slew Rate		50	V/ns
Pn <sup>(1)(2)(3)</sup>	Power Dissipation	8-SOP	0.625	W
LD	Power Dissipation	14-SOP	1.000	VV
0	Thermal Pagistance Junction to Ambient	8-SOP	200	°C/W
$\theta_{\sf JA}$	Thermal Resistance, Junction-to-Ambient	14-SOP	110	C/VV
T <sub>J</sub>	Junction Temperature		+150	°C
T <sub>STG</sub>	Storage Temperature		+150	°C

#### Notes:

- 1. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- 2. Refer to the following standards:
  - JESD51-2: Integral circuits thermal test method environmental conditions natural convection
  - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- 3. Do not exceed PD under any circumstances.

### **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>B</sub>	High-Side Floating Supply Voltage	V <sub>S</sub> +10	V <sub>S</sub> +22	V
V <sub>S</sub>	High-Side Floating Supply Offset Voltage	6-V <sub>DD</sub>	600	V
$V_{HO}$	High-Side Output Voltage	V <sub>S</sub>	$V_{B}$	V
$V_{DD}$	Low-Side and Logic Supply Voltage	10	22	V
$V_{LO}$	Low-Side Output Voltage	COM	$V_{DD}$	V
V <sub>IN</sub>	Logic Input Voltage (HIN and LIN)	V <sub>SS</sub>	$V_{DD}$	٧
$T_A$	Operating Ambient Temperature	-40	+125	°C

### **Electrical Characteristics**

 $V_{BIAS} \ (V_{DD}, \ V_{BS}) = 15.0 V, \ V_S = V_{SS} = COM, \ T_A = 25 ^{\circ}C, \ unless \ otherwise \ specified. \ The \ V_{IL}, \ V_{IH}, \ and \ I_{IN} \ parameters \ are referenced to V_{SS}/COM \ and \ are applicable to the respective input signals HIN and LIN. The V_O \ and I_O \ parameters \ are referenced to COM \ and V_S \ is applicable to the respective output signals HO \ and LO.$ 

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
POWER S	SUPPLY SECTION (V <sub>DD</sub> AND V <sub>BS</sub> )		II.			
V <sub>DDUV+</sub> V <sub>BSUV+</sub>	V <sub>DD</sub> and V <sub>BS</sub> Supply Under-Voltage Positive-going Threshold		8.0	8.8	9.8	
V <sub>DDUV-</sub> V <sub>BSUV-</sub>	V <sub>DD</sub> and V <sub>BS</sub> Supply Under-Voltage Negative-going Threshold		7.4	8.3	9.0	V
V <sub>DDUVH</sub> V <sub>BSUVH</sub>	V <sub>DD</sub> and V <sub>BS</sub> Supply Under-Voltage Lockout Hysteresis Voltage			0.5		
I <sub>LK</sub>	Offset Supply Leakage Current	V <sub>B</sub> =V <sub>S</sub> =600V			50	
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>IN</sub> =0V or 5V		45	80	μΑ
I <sub>QDD</sub>	Quiescent V <sub>DD</sub> Supply Current	V <sub>IN</sub> =0V or 5V		75	110	
I <sub>PBS</sub>	Operating V <sub>BS</sub> Supply Current	f <sub>IN</sub> =20kHz, rms value		530	640	^
I <sub>PDD</sub>	Operating V <sub>DD</sub> Supply Current	f <sub>IN</sub> =20kHz, rms value		530	640	μΑ
LOGIC IN	PUT SECTION (HIN, LIN)			•		
V <sub>IH</sub>	Logic "1" Input Voltage		2.5		6.	V
$V_{IL}$	Logic "0" Input Voltage				1.2	V
$I_{IN+}$	Logic "1" Input Bias Current	V <sub>IN</sub> =5V		25	50	
I <sub>IN-</sub>	Logic "0" Input Bias Current	V <sub>IN</sub> =0V		1.0	2.0	μΑ
R <sub>IN</sub>	Input Pull-down Resistance		100	200		ΚΩ
GATE DR	IVER OUTPUT SECTION (HO, LO)			I.		
V <sub>OH</sub>	High-level Output Voltage, V <sub>BIAS</sub> -V <sub>O</sub>	No Load			1.0	V
V <sub>OL</sub>	Low-level Output Voltage, V <sub>O</sub>	No Load			35	mV
I <sub>O+</sub>	Output High, Short-circuit Pulsed Current <sup>(4)</sup>	$V_O=0V$ , $V_{IN}=5V$ with PW<10 $\mu$ s	3.5	4.5		А
I <sub>O-</sub>	Output Low, Short-circuit Pulsed Current <sup>(4)</sup>	V <sub>O</sub> =15V, V <sub>IN</sub> =0V with PW<10µs	3.5	4.5		A
V <sub>S</sub>	Allowable Negative V <sub>S</sub> Pin Voltage for HIN Signal Propagation to HO		/	-9.8	-7.0	V
V <sub>SS</sub> - COM	V <sub>SS</sub> -COM/COM-V <sub>SS</sub> Voltage Endurability	/	-7.0	_	7.0	٧

### Note:

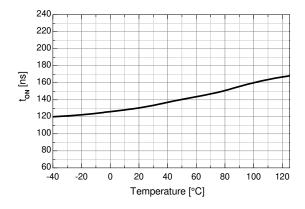
4. This parameter guaranteed by design.

## **Dynamic Electrical Characteristics**

V<sub>BIAS</sub> (V<sub>DD</sub>, V<sub>BS</sub>)=15.0V, V<sub>S</sub>=V<sub>SS</sub>=COM=0V, C<sub>L</sub>=1000pF and T<sub>A</sub>=25°C unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
t <sub>on</sub>	Turn-on Propagation Delay	V <sub>S</sub> =0V		140	200	
t <sub>off</sub>	Turn-off Propagation Delay	V <sub>S</sub> =0V		140	200	
MT	Delay Matching, HS & LS Turn-on/off			0	50	ns
t <sub>r</sub>	Turn-on Rise Time			25	50	
t <sub>f</sub>	Turn-off Fall Time			20	45	

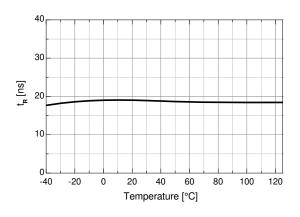
# **Typical Characteristics**



240 220 200 180 to 160 140 120 100 80 60 l -40 -20 40 60 80 100 Temperature [°C]

Figure 6. Turn-on Propagation Delay vs. Temperature

Figure 7. Turn-off Propagation Delay vs. Temperature



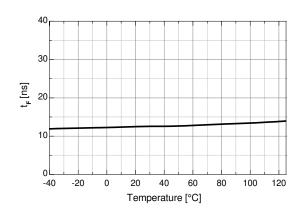
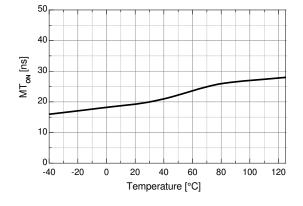


Figure 8. Turn-on Rise Time vs. Temperature

Figure 9. Turn-off Fall Time vs. Temperature



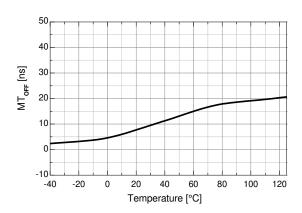
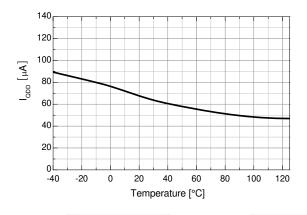


Figure 10. Turn-on Delay Matching vs. Temperature

Figure 11. Turn-off Delay Matching vs. Temperature

## Typical Characteristics (Continued)



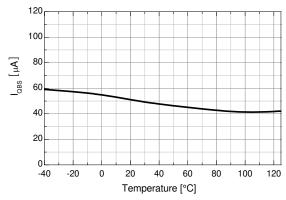
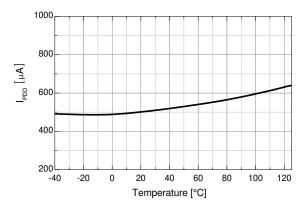


Figure 12. Quiescent V<sub>DD</sub> Supply Current vs. Temperature

Figure 13. Quiescent V<sub>BS</sub> Supply Current vs. Temperature



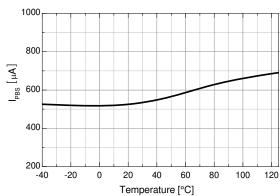
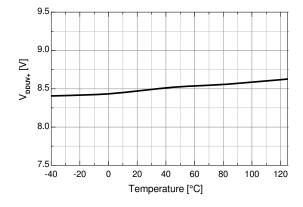


Figure 14. Operating V<sub>DD</sub> Supply Current vs. Temperature

Figure 15. Operating V<sub>BS</sub> Supply Current vs. Temperature.



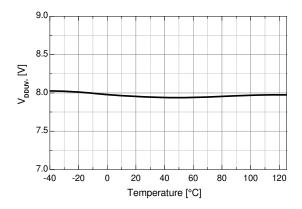
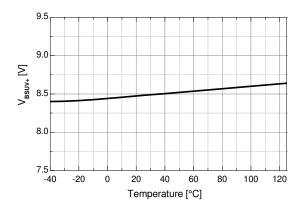


Figure 16. V<sub>DD</sub> UVLO+ vs. Temperature

Figure 17. V<sub>DD</sub> UVLO- vs. Temperature

## Typical Characteristics (Continued)



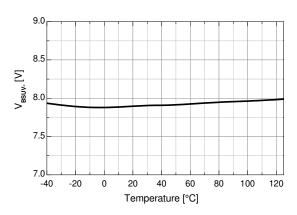
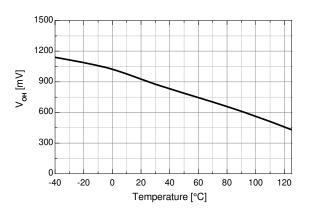


Figure 18. V<sub>BS</sub> UVLO+ vs. Temperature

Figure 19. V<sub>BS</sub> UVLO- vs. Temperature



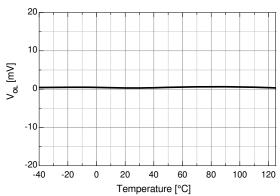
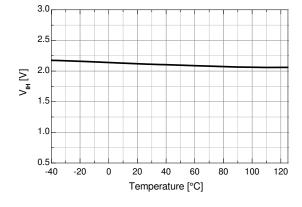


Figure 20. High-Level Output Voltage vs. Temperature

Figure 21. Low-Level Output Voltage vs. Temperature



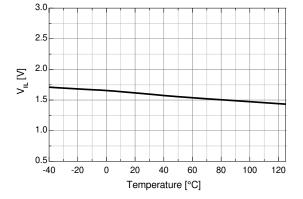
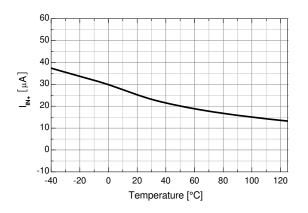


Figure 22. Logic High Input Voltage vs. Temperature

Figure 23. Low Input Voltage vs. Temperature

# Typical Characteristics (Continued)



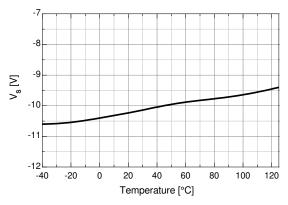


Figure 24. Logic Input High Bias Current vs. Temperature

Figure 25. Allowable Negative V<sub>S</sub> Voltage vs. Temperature

# **Switching Time Definitions**

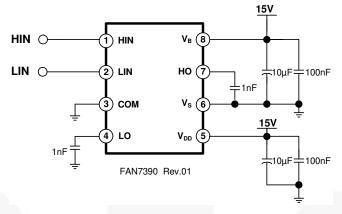


Figure 26. Switching Time Test Circuit (Referenced 8-SOP)

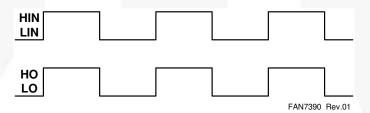


Figure 27. Input/Output Timing Diagram

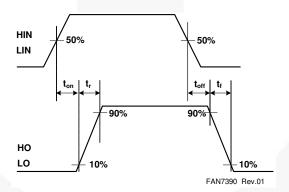


Figure 28. Switching Time Waveform Definitions

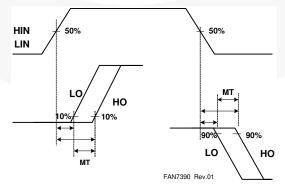
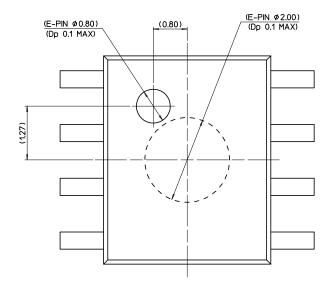
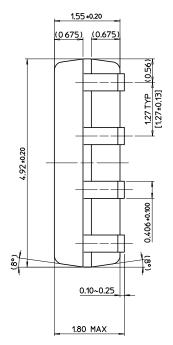


Figure 29. Delay Matching Waveform Definitions

### **Physical Dimensions**





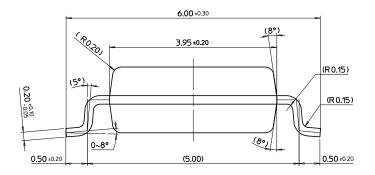


Figure 30. 8-Lead Small Outline Package (SOP)

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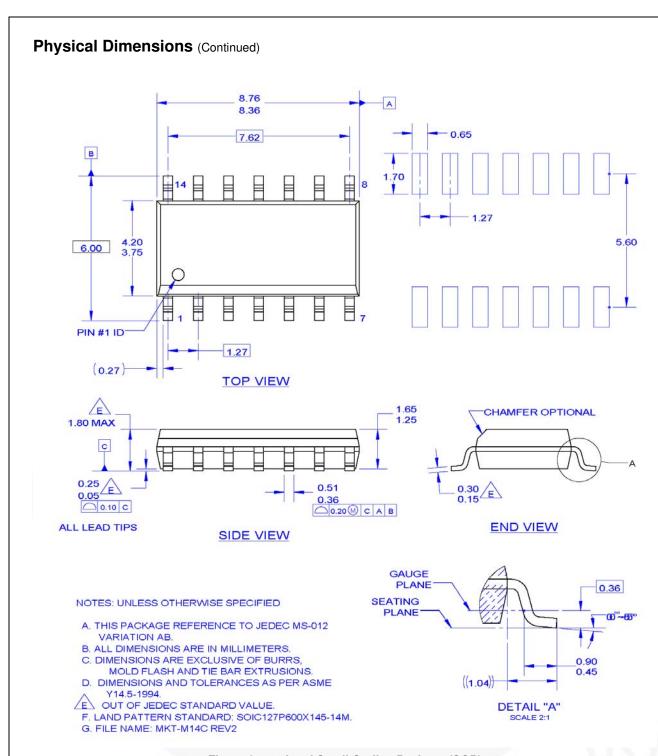


Figure 31. 14-Lead Small Outline Package (SOP)

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#### Definition of Terms

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