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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# FCBS0550

## Smart Power Module (SPM)

### Features

- UL Certified No.E209204(SPM27-BA package)
- 500V-5A 3-phase MOSFET inverter bridge including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Isolation rating of 2500Vrms/min.
- Very low leakage current due to using ceramic substrate

### Applications

- AC 200V three-phase inverter drive for small power ac motor drives
- Home appliances applications like refrigerator.

### General Description

It is an advanced smart power module (SPM) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting low-power inverter-driven application like refrigerator. It combines optimized circuit protection and drive matched to low-loss MOSFETs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides opto-coupler-less single-supply MOSFET gate driving capability that further reduce the overall size of the inverter system design. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.

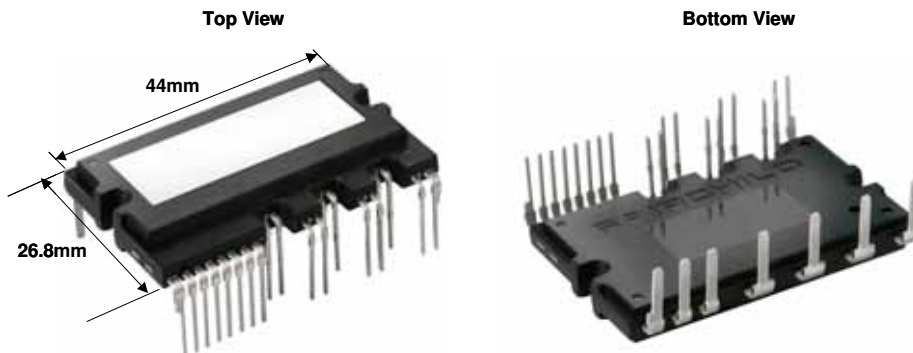


Figure 1.

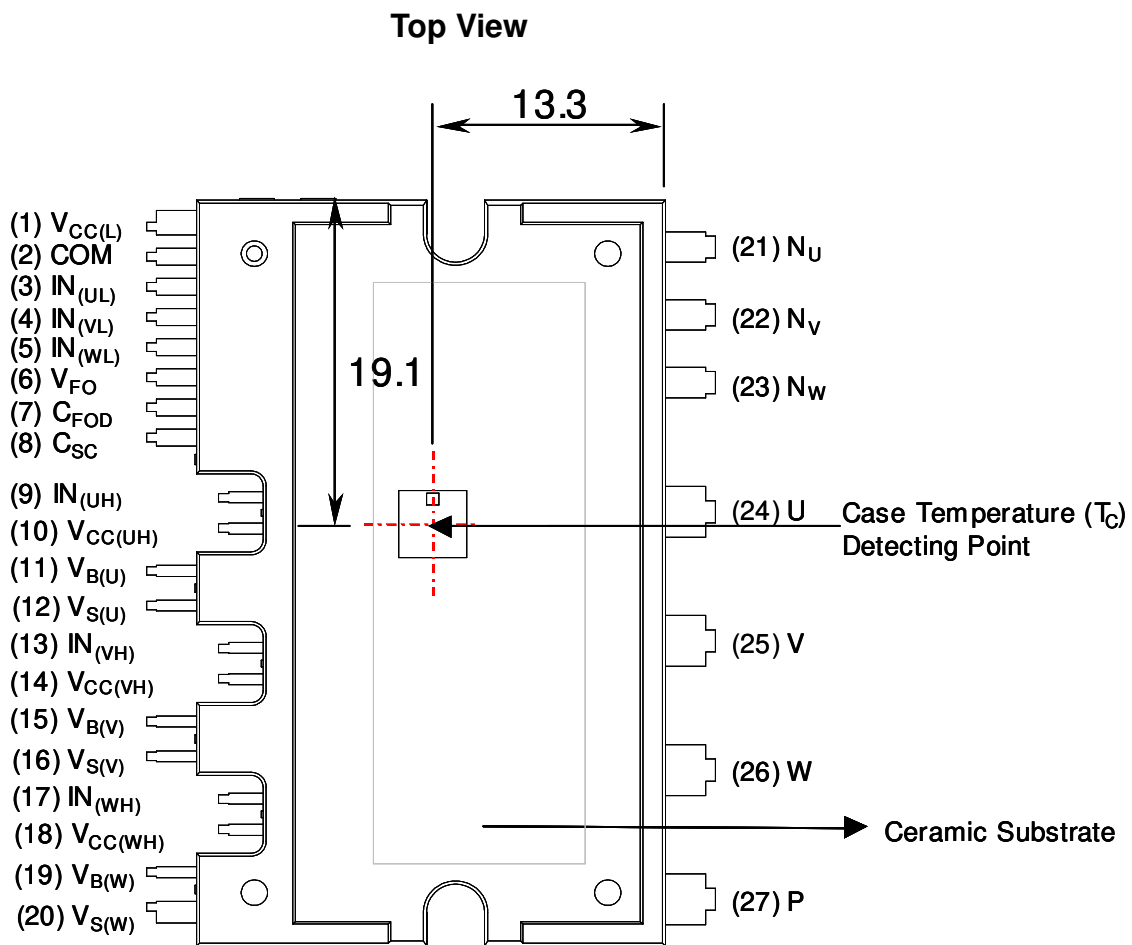
### Integrated Power Functions

- 500V-5A MOSFET inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)

### Integrated Drive, Protection and System Control Functions

- For inverter high-side MOSFETs: Gate drive circuit, High voltage isolated high-speed level shifting  
Control circuit under-voltage (UV) protection  
Note) Available bootstrap circuit example is given in Figs. 10 and 11.
- For inverter low-side MOSFETs: Gate drive circuit, Short circuit protection (SC)  
Control supply circuit under-voltage (UV) protection
- Fault signaling: Corresponding to a UV fault (Low-side supply), SC fault
- Input interface: 3.3/5V CMOS/LSTTL compatible, Schmitt trigger input

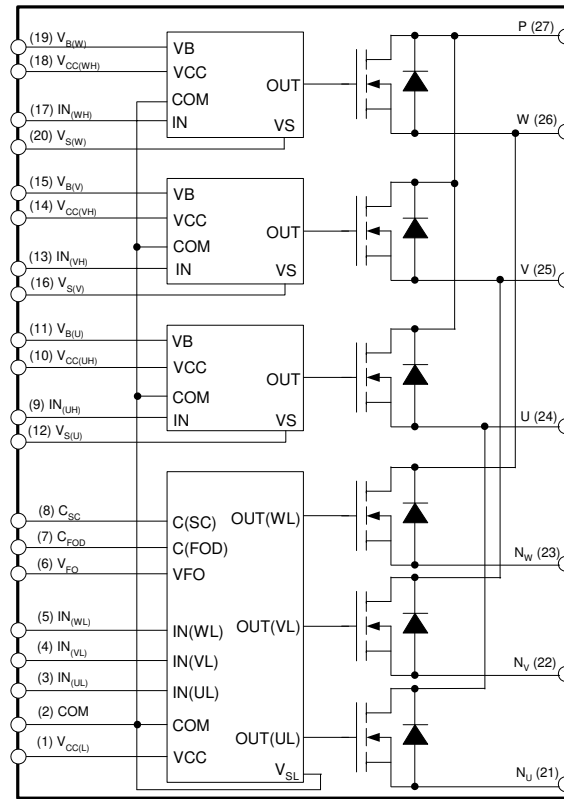
### Pin Configuration



## Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and MOSFETs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	$V_{FO}$	Fault Output
7	$C_{FOD}$	Capacitor for Fault Output Duration Time Selection
8	$C_{SC}$	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U Phase
10	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
11	$V_{B(U)}$	High-side Bias Voltage for U Phase MOSFET Driving
12	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase MOSFET Driving
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
15	$V_{B(V)}$	High-side Bias Voltage for V Phase MOSFET Driving
16	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase MOSFET Driving
17	$IN_{(WH)}$	Signal Input for High-side W Phase
18	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
19	$V_{B(W)}$	High-side Bias Voltage for W Phase MOSFET Driving
20	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase MOSFET Driving
21	$N_U$	Negative DC-Link Input for U Phase
22	$N_V$	Negative DC-Link Input for V Phase
23	$N_W$	Negative DC-Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC-Link Input

### Internal Equivalent Circuit and Input/Output Pins



**Note:**

1. Inverter low-side is composed of three MOSFETs, and one control IC. It has gate driving and protection functions.
2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three MOSFETs and three drive ICs for each MOSFET.

**Figure 3.**

## Absolute Maximum Ratings ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

### Inverter Part

Symbol	Parameter	Conditions	Rating	Units
$V_{PN}$	Supply Voltage	Applied between P- $N_U$ , $N_V$ , $N_W$	400	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P- $N_U$ , $N_V$ , $N_W$	450	V
$V_{DSS}$	Drain-Source Voltage		500	V
$\pm I_D$	Each MOSFET Drain Current	$T_C = 25^\circ\text{C}$ , Peak Sinusoidal Current	5	A
$\pm I_{DP}$	Each MOSFET Drain Current (Peak)	$T_C = 25^\circ\text{C}$ , Under 1ms Pulse Width	7	A
$P_C$	Collector Dissipation	$T_C = 25^\circ\text{C}$ per One Chip	25	W
$T_J$	Operating Junction Temperature	(Note 1)	-20 ~ 125	$^\circ\text{C}$

**Note:**

1. The maximum junction temperature rating of the power chips integrated within the SPM is  $150^\circ\text{C}$  ( $@T_C \leq 100^\circ\text{C}$ ). However, to insure safe operation of the SPM, the average junction temperature should be limited to  $T_{J(\text{ave})} \leq 125^\circ\text{C}$  ( $@T_C \leq 100^\circ\text{C}$ )

### Control Part

Symbol	Parameter	Conditions	Rating	Units
$V_{CC}$	Control Supply Voltage	Applied between $V_{CC(UH)}$ , $V_{CC(VH)}$ , $V_{CC(WH)}$ , $V_{CC(L)}$ - COM	20	V
$V_{BS}$	High-side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$ , $V_{B(V)}$ - $V_{S(V)}$ , $V_{B(W)}$ - $V_{S(W)}$	20	V
$V_{IN}$	Input Signal Voltage	Applied between $IN_{(UH)}$ , $IN_{(VH)}$ , $IN_{(WH)}$ , $IN_{(UL)}$ , $IN_{(VL)}$ , $IN_{(WL)}$ - COM	-0.3~17	V
$V_{FO}$	Fault Output Supply Voltage	Applied between $V_{FO}$ - COM	$-0.3 \sim V_{CC} + 0.3$	V
$I_{FO}$	Fault Output Current	Sink Current at $V_{FO}$ Pin	5	mA
$V_{SC}$	Current Sensing Input Voltage	Applied between $C_{SC}$ - COM	$-0.3 \sim V_{CC} + 0.3$	V

### Total System

Symbol	Parameter	Conditions	Rating	Units
$T_{SC}$	Short Circuit Withstanding Time	$V_{CC} = V_{BS} = 13.5 \sim 16.5\text{V}$ , $T_J = 125^\circ\text{C}$ , Non-repetitive, $V_{PN} = 400\text{V}$ , $R_{\text{Shunt}} = 0\text{m}\Omega$	10	$\mu\text{s}$
$T_C$	Module Case Operation Temperature	$-20^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ , See Figure 2	-20 ~ 100	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
$V_{ISO}$	Isolation Voltage	60Hz, Sinusoidal, AC 1 minute, Connection Pins to ceramic substrate	2500	$V_{\text{rms}}$

### Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)}$	Junction to Case Thermal Resistance	Inverter MOSFET part (per 1/6 module)	-	-	4	$^\circ\text{C}/\text{W}$

**Note:**

2. For the measurement point of case temperature( $T_C$ ), please refer to Figure 2.

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCBS0550	FCBS0550	SPM27BA	-	-	10

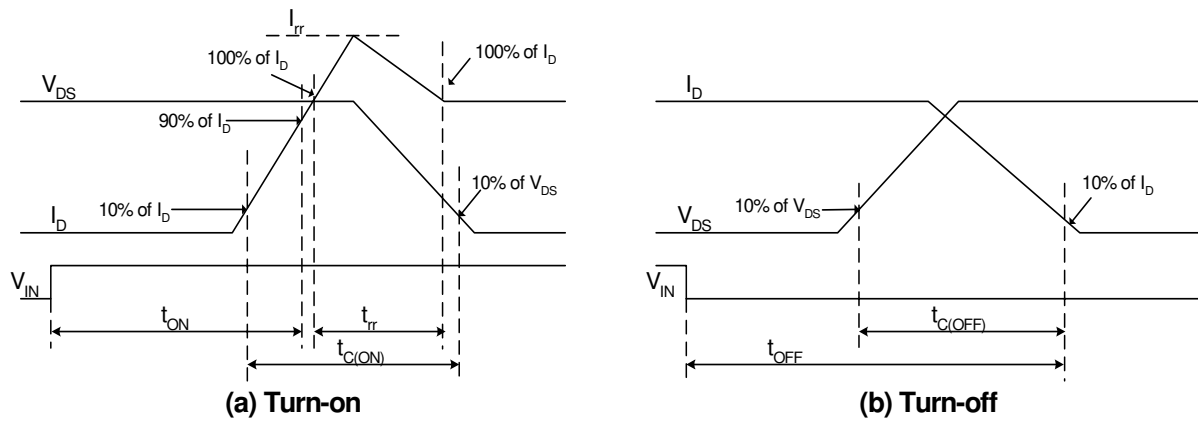
### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

#### Inverter Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{DS(ON)}$	Static Drain-Source On Resistance	$V_{CC} = V_{BS} = 15\text{V}$ $V_{IN} = 5\text{V}$ $I_D = 2.5\text{A}, T_J = 25^\circ\text{C}$	-	1.35	1.75	$\Omega$
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{CC} = V_{BS} = 15\text{V}$ $V_{IN} = 0\text{V}$ $I_D = 2.5\text{A}, T_J = 25^\circ\text{C}$	-	-	1.20	V
HS	$t_{ON}$	Switching Times $V_{PN} = 300\text{V}, V_{CC} = V_{BS} = 15\text{V}$ $I_D = 2.5\text{A}$ $V_{IN} = 0\text{V} \leftrightarrow 5\text{V}$ , Inductive Load (Note 3)	-	0.51	-	$\mu\text{s}$
	$t_{C(ON)}$		-	0.16	-	$\mu\text{s}$
	$t_{OFF}$		-	0.72	-	$\mu\text{s}$
	$t_{C(OFF)}$		-	0.10	-	$\mu\text{s}$
	$t_{rr}$		-	0.16	-	$\mu\text{s}$
LS	$t_{ON}$	$V_{PN} = 300\text{V}, V_{CC} = V_{BS} = 15\text{V}$ $I_D = 2.5\text{A}$ $V_{IN} = 0\text{V} \leftrightarrow 5\text{V}$ , Inductive Load (Note 3)	-	0.52	-	$\mu\text{s}$
	$t_{C(ON)}$		-	0.18	-	$\mu\text{s}$
	$t_{OFF}$		-	0.74	-	$\mu\text{s}$
	$t_{C(OFF)}$		-	0.10	-	$\mu\text{s}$
	$t_{rr}$		-	0.16	-	$\mu\text{s}$
$I_{DSS}$	Drain - Source Leakage Current	$V_{DS} = V_{DSS}$	-	-	250	$\mu\text{A}$

**Note:**

3.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive IC.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.



**Figure 4. Switching Time Definition**

## Electrical Characteristics (T<sub>J</sub> = 25°C, Unless Otherwise Specified)

### Control Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
I <sub>QCCL</sub>	Quiescent V <sub>CC</sub> Supply Current	V <sub>CC</sub> = 15V I <sub>N(U<sub>L</sub>, V<sub>L</sub>, W<sub>L</sub>)</sub> = 0V	V <sub>CC(L)</sub> - COM	-	-	23	mA
I <sub>QCCH</sub>		V <sub>CC</sub> = 15V I <sub>N(U<sub>H</sub>, V<sub>H</sub>, W<sub>H</sub>)</sub> = 0V	V <sub>CC(U<sub>H</sub>)</sub> , V <sub>CC(V<sub>H</sub>)</sub> , V <sub>CC(W<sub>H</sub>)</sub> - COM	-	-	100	μA
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>BS</sub> = 15V I <sub>N(U<sub>H</sub>, V<sub>H</sub>, W<sub>H</sub>)</sub> = 0V	V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	-	-	500	μA
V <sub>FOH</sub>	Fault Output Voltage	V <sub>SC</sub> = 0V, V <sub>FO</sub> Circuit: 4.7kΩ to 5V Pull-up	4.5	-	-	V	
V <sub>FOL</sub>		V <sub>SC</sub> = 1V, V <sub>FO</sub> Circuit: 4.7kΩ to 5V Pull-up	-	-	0.8	V	
V <sub>SC(ref)</sub>	Short Circuit Trip Level	V <sub>CC</sub> = 15V (Note 4)	0.45	0.5	0.55	V	
UV <sub>CCD</sub>	Supply Circuit Under-Voltage Protection	Detection Level	10.7	11.9	13.0	V	
UV <sub>CCR</sub>		Reset Level	11.2	12.4	13.2	V	
UV <sub>BSD</sub>		Detection Level	10.1	11.3	12.5	V	
UV <sub>BSR</sub>		Reset Level	10.5	11.7	12.9	V	
t <sub>FOD</sub>	Fault-out Pulse Width	C <sub>FOD</sub> = 33nF (Note 5)	1.0	1.8	-	ms	
V <sub>IN(ON)</sub>	ON Threshold Voltage	Applied between I <sub>N(U<sub>H</sub>)</sub> , I <sub>N(V<sub>H</sub>)</sub> , I <sub>N(W<sub>H</sub>)</sub> , I <sub>N(U<sub>L</sub>)</sub> , I <sub>N(V<sub>L</sub>)</sub> , I <sub>N(W<sub>L</sub>)</sub> - COM	2.9	-	-	V	
V <sub>IN(OFF)</sub>	OFF Threshold Voltage		-	-	0.8	V	

**Note:**

4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width t<sub>FOD</sub> depends on the capacitance value of C<sub>FOD</sub> according to the following approximate equation : C<sub>FOD</sub> = 18.3 × 10<sup>-6</sup> × t<sub>FOD</sub>[F]

### Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V <sub>PN</sub>	Supply Voltage	Applied between P - N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub>	-	300	400	V
V <sub>CC</sub>	Control Supply Voltage	Applied between V <sub>CC(U<sub>H</sub>)</sub> , V <sub>CC(V<sub>H</sub>)</sub> , V <sub>CC(W<sub>H</sub>)</sub> , V <sub>CC(L)</sub> - COM	13.5	15	16.5	V
V <sub>BS</sub>	High-side Bias Voltage	Applied between V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	13.0	15	18.5	V
dV <sub>CC</sub> /dt, dV <sub>BS</sub> /dt	Control supply variation		-1	-	1	V/μs
t <sub>dead</sub>	Blanking Time for Preventing Arm-short	For Each Input Signal	2	-	-	μs
f <sub>PWM</sub>	PWM Input Signal	-20°C ≤ T <sub>C</sub> ≤ 100°C, -20°C ≤ T <sub>J</sub> ≤ 125°C	-	-	20	kHz
V <sub>SEN</sub>	Voltage for Current Sensing	Applied between N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub> - COM (Including surge voltage)	-4		4	V



### Mechanical Characteristics and Ratings

Parameter	Conditions		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: - M3	Recommended 0.62N•m	0.51	0.62	0.72	N•m
Device Flatness		Note Fig. 5	0	-	+120	μm
Weight			-	15.4	-	g

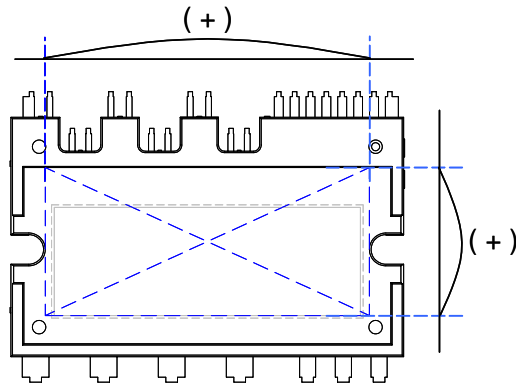
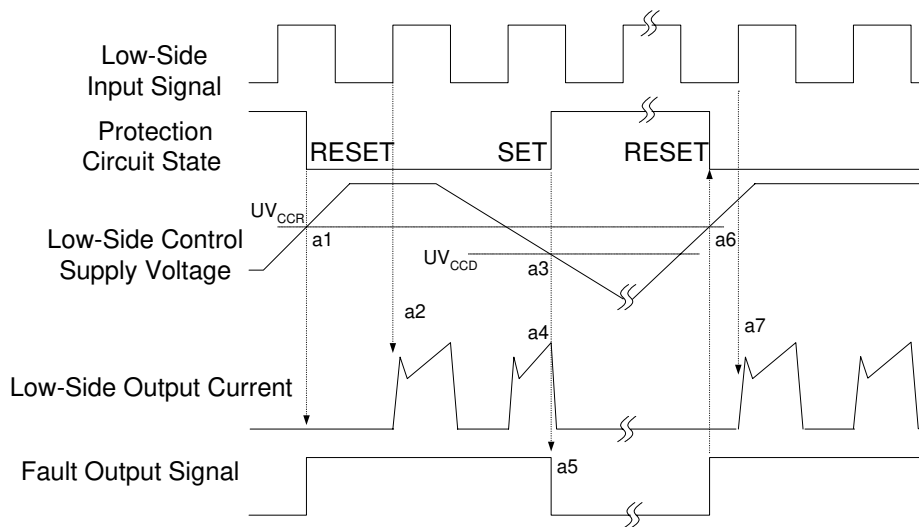


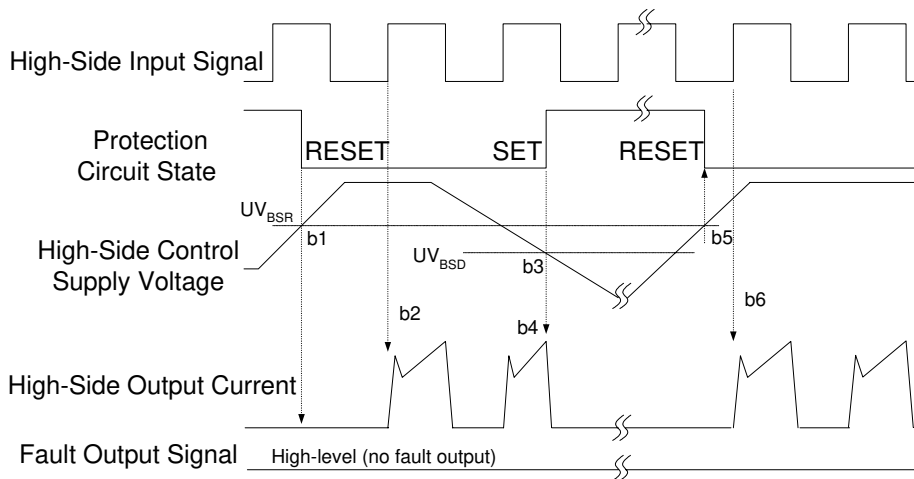
Figure 5. Flatness Measurement Position

### Time Charts of SPMs Protective Function



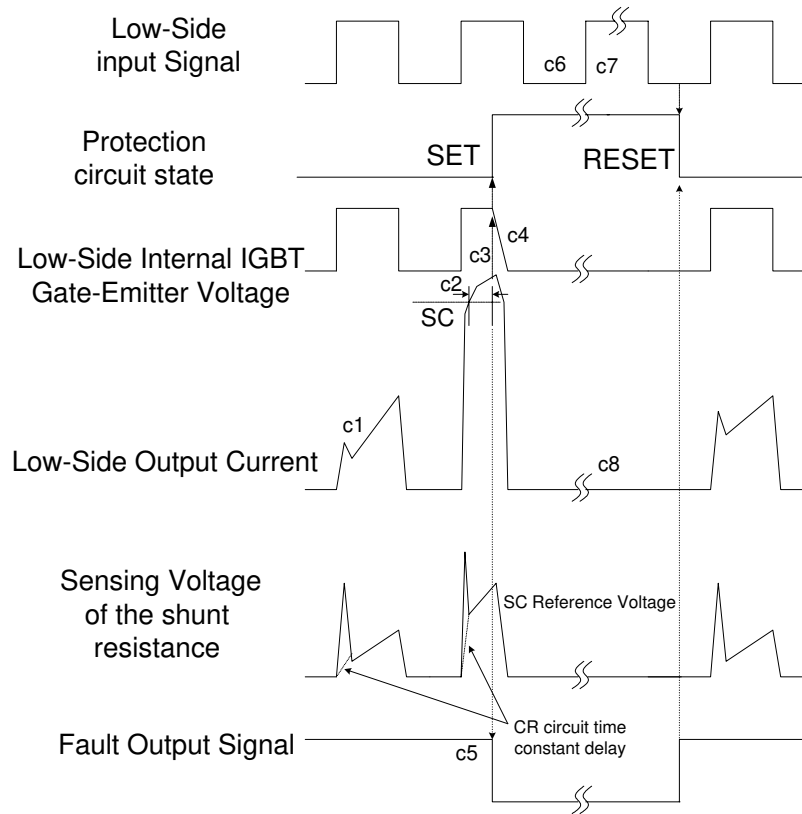
- a1 : Control supply voltage rises: After the voltage rises  $UV_{CCR}$ , the circuits start to operate when next input is applied.
- a2 : Normal operation: MOSFET ON and carrying current.
- a3 : Under voltage detection ( $UV_{CCD}$ ).
- a4 : MOSFET OFF in spite of control input condition.
- a5 : Fault output operation starts.
- a6 : Under voltage reset ( $UV_{CCR}$ ).
- a7 : Normal operation: MOSFET ON and carrying current.

**Figure 6. Under-Voltage Protection (Low-side)**



- b1 : Control supply voltage rises: After the voltage reaches  $UV_{BSR}$ , the circuits start to operate when next input is applied.
- b2 : Normal operation: MOSFET ON and carrying current.
- b3 : Under voltage detection ( $UV_{BSD}$ ).
- b4 : MOSFET OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under voltage reset ( $UV_{BSR}$ )
- b6 : Normal operation: MOSFET ON and carrying current

**Figure 7. Under-Voltage Protection (High-side)**



(with the external shunt resistance and CR connection)

c1 : Normal operation: MOSFET ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard MOSFET gate interrupt.

c4 : MOSFET turns OFF.

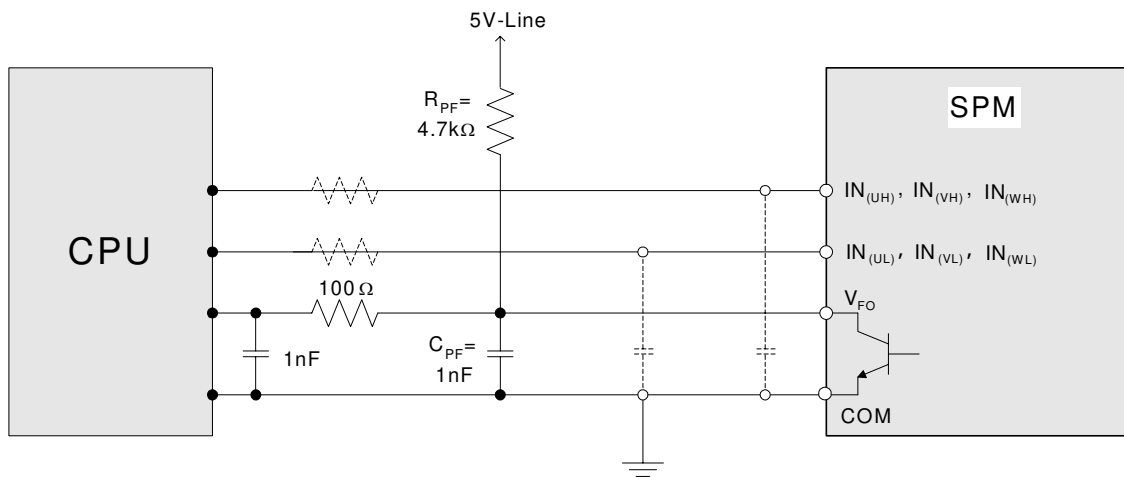
c5 : Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor  $C_{FO}$ .

c6 : Input "L" : MOSFET OFF state.

c7 : Input "H": MOSFET ON state, but during the active period of fault output the MOSFET doesn't turn ON.

c8 : MOSFET OFF state

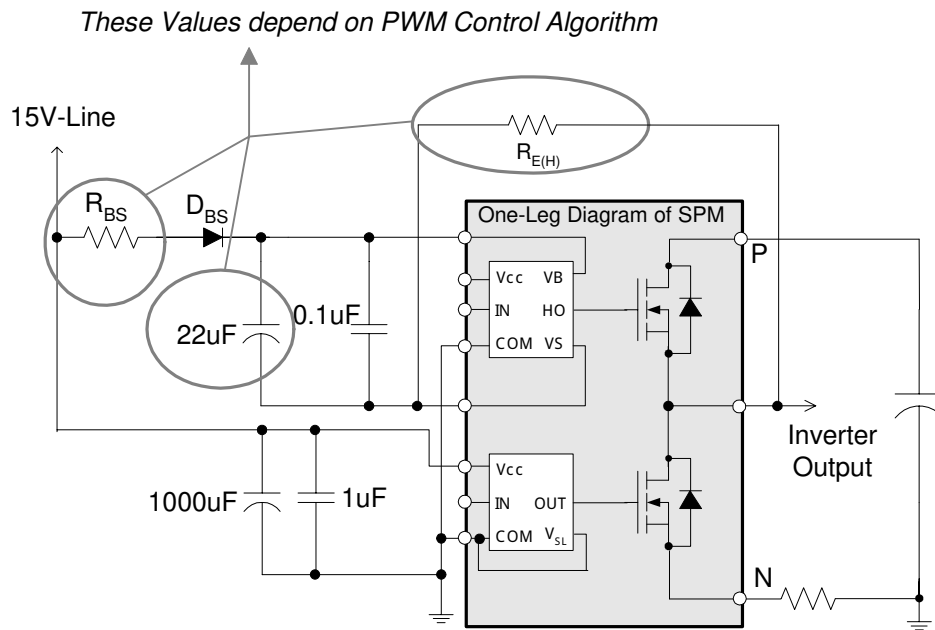
**Figure 8. Short-Circuit Current Protection (Low-side Operation only)**



**Note:**

1. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The SPM input signal section integrates 3.3kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.
2. The logic input is compatible with standard CMOS or LSTTL outputs.

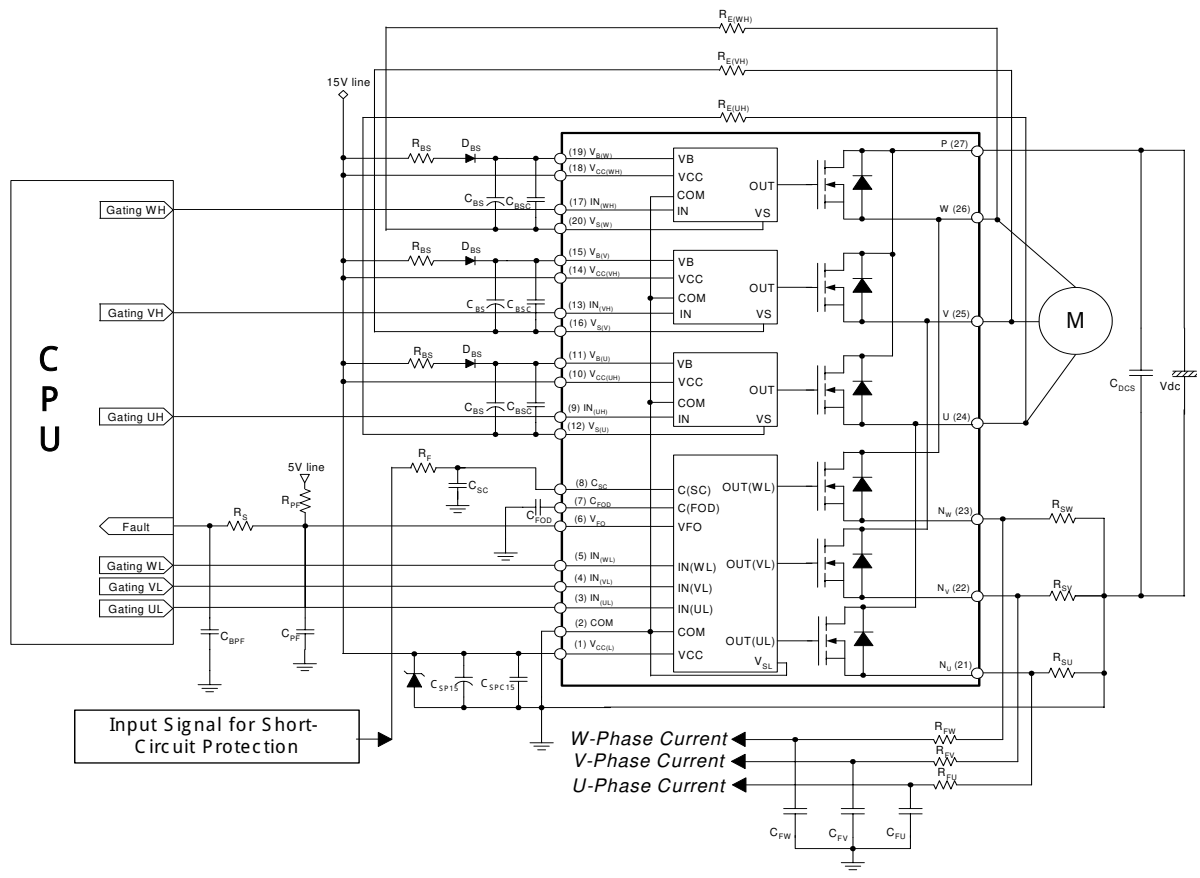
**Figure 9. Recommended CPU I/O Interface Circuit**



**Note:**

1. It would be recommended that the bootstrap diode,  $D_{BS}$ , has soft and fast recovery characteristics.
2. The bootstrap resistor ( $R_{BS}$ ) should be 3 times greater than  $R_{E(H)}$ . The recommended value of  $R_{E(H)}$  is 5.6Ω, but it can be increased up to 20Ω (maximum) for a slower dv/dt of high-side.
3. The ceramic capacitor placed between  $V_{CC}$ -COM should be over 1uF and mounted as close to the pins of the SPM as possible.

**Fig. 10. Recommended Bootstrap Operation Circuit and Parameters**

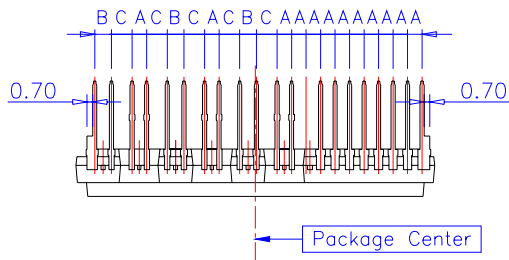


**Note:**

1. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
2. By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. V<sub>FOD</sub> output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Figure 9.
4. C<sub>SP15</sub> of around 7 times larger than bootstrap capacitor C<sub>BS</sub> is recommended.
5. V<sub>FOD</sub> output pulse width should be determined by connecting an external capacitor (C<sub>FOD</sub>) between C<sub>FOD</sub>(pin7) and COM(pin2). (Example : if C<sub>FOD</sub> = 33 nF, then t<sub>FO</sub> = 1.8ms (typ.)) Please refer to the note 5 for calculation method.
6. Input signal is High-Active type. There is a 3.3kΩ resistor inside the IC to pull down each input signal line to GND. When employing RC coupling circuits, set up such RC couple that input signal agree with turn-off/turn-on threshold voltage.
7. To prevent errors of the protection function, the wiring around R<sub>F</sub> and C<sub>SC</sub> should be as short as possible.
8. In the short-circuit protection circuit, please select the R<sub>F</sub>C<sub>SC</sub> time constant in the range 1.5~2 μs.
9. Each capacitor should be mounted as close to the pins of the SPM as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P&COM pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P&COM pins is recommended.
11. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.
12. C<sub>SP15</sub> should be over 1μF and mounted as close to the pins of the SPM as possible.

**Fig. 11. Typical Application Circuit**

Detailed Package Outline Drawings

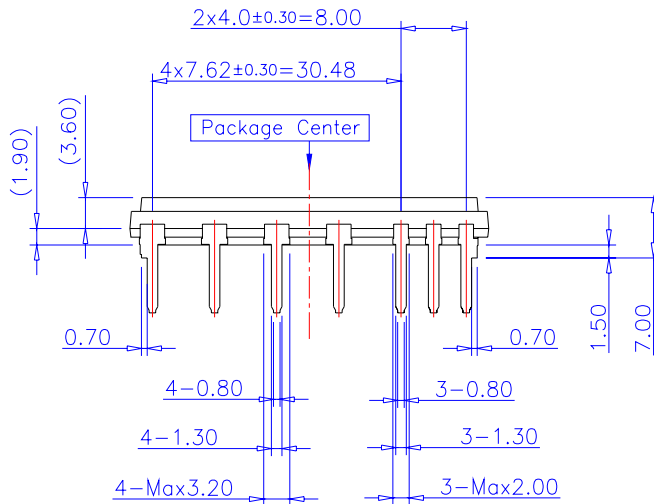
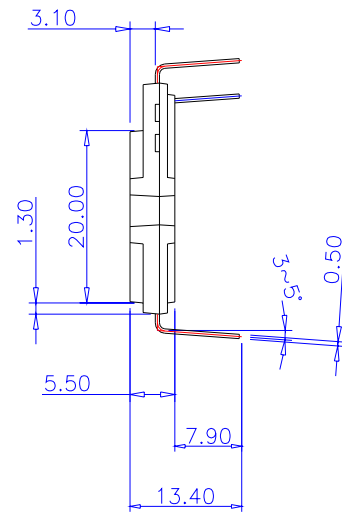
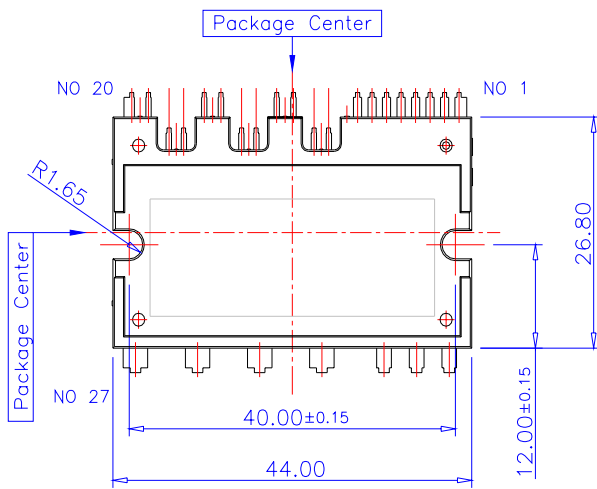


Lead Pitch :  $\pm 0.30$

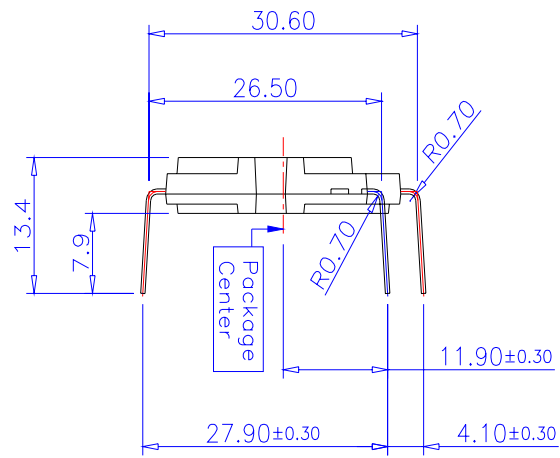
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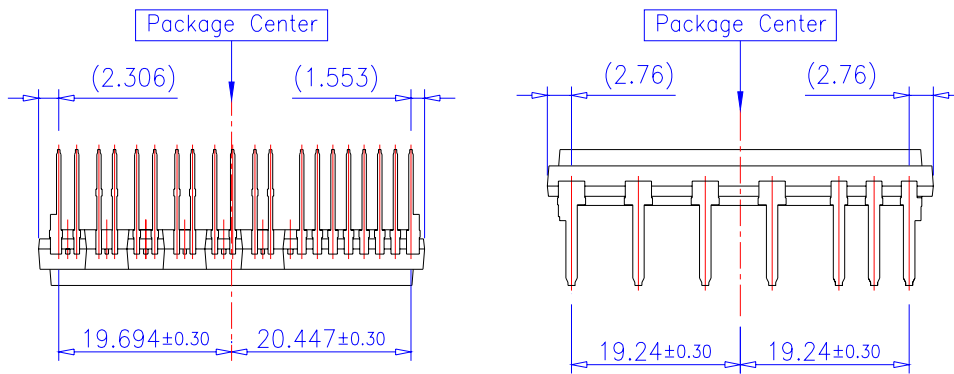
C : 2.531



Detailed Package Outline Drawings (Continued)

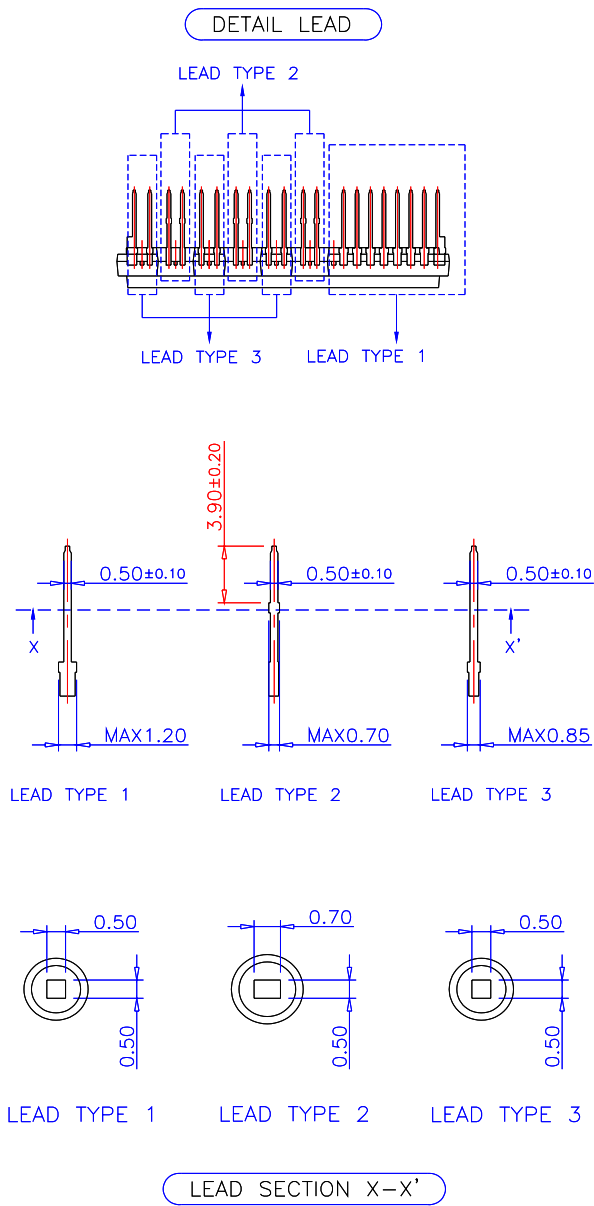


Lead Forming Dimension



PKG Center to Lead Distance

Detailed Package Outline Drawings (Continued)





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DOME™	GTO™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	HiSeC™	MICROWIRE™	QS™	SyncFET™
E <sup>2</sup> C MOS™	I <sup>2</sup> C™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	i-Lo™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	μSerDes™	UltraFET®
The Power Franchise®		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
Programmable Active Droop™		PACMAN™	SMART START™	VCX™

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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