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FAIRCHILD

SEMICONDUCTOR®

March 2013

FCM8202
3-Phase Sinusoidal Brushless DC Motor Controller

Features

- Supports Space Vector Modulation (SVM)
- Supports Sine-Wave & Square-Wave Solutions
- Built-in Clock Generator
- Built-in Error Amplifier for Torque Loop Control
- Direct Duty Control
- Square-Wave 120°, Sine-Wave 180° Turn-on
- PLL Angle Detection (Hall Sensors)
- Current Leading Phase Correction
- Two Selectable Dead Times
- Synchronous Rectifying
- Over-Voltage and Under-Voltage Protections
- Motor and Power Transistors for Over-Voltage Protections (OVP)
- Three Levels of Over-Current Protections (OCP)
- Adjustable OC Timer
- Over-Temperature Protection (OTP)

Applications

- BLDC Motor or PMSM Control
- Low Noise Motor Applications
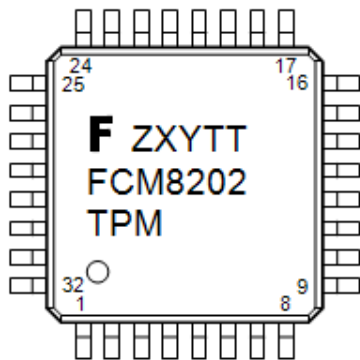- Fan, Pump, Tools, etc.

Description

FCM8202 is a three-phase sinusoidal Brushless DC (BLDC) motor or Permanent Magnet Synchronous Motor (PMSM) controller. It comes with the advanced Hall sensor design. Using the Hall sensor signals, the control system is able to execute the PWM commutation by switching the three-phase inverter. There are two PWM modes: Sine-Wave Mode and Square-Wave Mode. The Square-Wave Mode includes PWM-PWM and PWM-ON approaches to improve the efficiency of the motor drive.

Complete protection functions including over-voltage, over-current, over-temperature, and short-circuit protections prevent the control circuits and the motor from being damaged, particularly under stressed applications and demanding environments.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FCM8202QY	-40°C to 125°C	32-Lead, LQFP, JEDEC MS-026, Variation BBA, 7 mm Square	Tray

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Typical Application Circuit

Figure 1.   Typical Application Circuit

Block Diagram

Figure 2.   System Block Diagram

Marking Information

Figure 3. Top Mark

F- Fairchild Logo
Z- Plant Code
X- 1-Digit Year Code
Y- 1-Digit Week Code
TT: 2-Digit Die Run Code
T: Package Type (Q=LQFP)
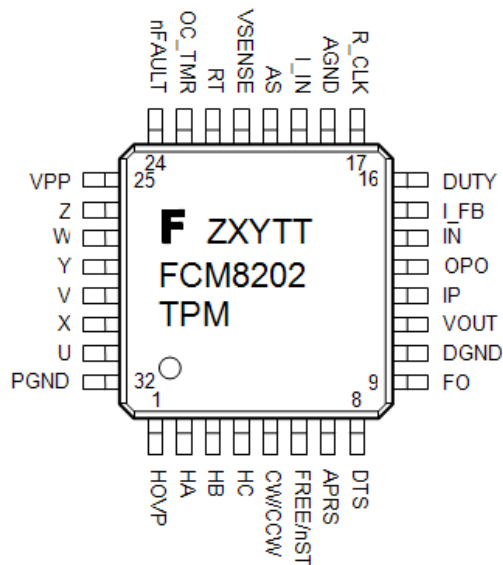P: Y=Green Package
M: Die Run Code

Pin Configuration

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	HOVP	Motor Drive Over-Voltage Protection Output. Can be connected to an external power transistor for discharging the Back-EMF.
2	HA	Hall A Sensor Input. Phase-U magnetic field detection.
3	HB	Hall B Sensor Input. Phase-V magnetic field detection.
4	HC	Hall C Sensor Input. Phase-W magnetic field detection.
5	CW/CCW	Direction Control Input. This pin has a 200 kΩ internal pull-up. HIGH: CW, LOW: CCW.
6	FREE/nST	Free and Start Control Input. This pin has a 200 kΩ internal pull-up. HIGH: Free, LOW: Start.
7	APRS	Angle Predict Range Selection Input. This pin has a 200 kΩ internal pull-up. LOW: 0.8 ~ 80 Hz, HIGH: 3.2 ~ 320 Hz Hall Frequency.
8	DTS	Dead-Time Selection Input. This pin has a 200 kΩ internal pull-up. LOW: 3 µs, HIGH: 4 µs.
9	FO	Revolution Pulse Output. Pulses per revolution = motor poles ÷ 2 × 3.
10	DGND	Digital Ground
11	VOUT	Voltage Regulator Output. A 0.1 µF (minimum) capacitor should be connected between this pin and ground.
12	IP	Positive Input of Torque Error Amplifier
13	OPO	Output of Torque Error Amplifier
14	IN	Negative Input of Torque Error Amplifier
15	I_FB	Current Feedback Output
16	DUTY	PWM Duty Control Input. Designed to directly control the PWM duty cycle.
17	R_CLK	External Resistor of Clock Generator. Designed for determining the frequency of internal clock generator.
18	AGND	Analog Ground
19	I_IN	Current Feedback Input
20	AS	Angle Shift Input. Designed for correcting the lead angle of PWM output signals. The range is from 0° to 60° related to the induced magnetic voltage.
21	VSENSE	Motor Drive Voltage-Sensing Resistor. Designed for determining the voltage level of over-voltage protections.
22	RT	Thermistor Voltage Input. Connect to a Negative Temperature Coefficient (NTC) thermistor for the over-temperature protection.
23	OC_TMR	Overload Time-Out Programmable Input. Connect to a capacitor for determining the time delay of overload protection.
24	nFAULT	Fault Flag. Open-drain output, LOW: system failure.
25	VPP	Supply Voltage Input
26	Z	PWM Output of W-Phase, Low-Side
27	W	PWM Output of W-Phase, High-Side
28	Y	PWM Output of V-Phase, Low-Side
29	V	PWM Output of V-Phase, High-Side
30	X	PWM Output of U-Phase, Low-Side
31	U	PWM Output of U-Phase, High-Side
32	PGND	High-Voltage Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{PP}	Supply Voltage		0	30	V
θ_{JA}	Thermal Resistance, Junction-to-ambient			82	°C/W
θ_{JC}	Thermal Resistance, Junction-to-case			29	°C/W
T_J	Junction Temperature			+150	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model, JESD22-A114		2.50	kV
		Charged Device Model, JESD22-C101		1.25	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	-40		+125	°C
V_{PP}	Supply Voltage	10	12	17	V
f_{SYS}	System Clock	0.96	1.28	1.92	MHz
R_CLK	Clock Generator External Resistor		12		kΩ
R_{I_IN}	I_IN Bias Resistor		10		kΩ

Electrical Characteristics

V_{PP} = 12 V and T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PP} Section						
V_{PP_ON}	Turn-On Threshold Voltage		8.5	9.0	9.5	V
V_{PP_OFF}	Turn-Off Threshold Voltage		7.5	8.0	8.5	V
I_{DD_OP}	Operating Supply Current	V_{PP} = 12 V, f_{SYS} = 1.28 MHz	4.0	5.0	6.5	mA
Voltage Regulator Section						
V_{VOUT}	Regulator Output Voltage	Output Current 5 mA	5.0	5.2	5.5	V
I_{VOUT}	Regulator Output Current	V_{VOUT} = 5.2 V			10	mA
C_{VOUT}	Regulator External Capacitor		0.1			µF
Digital I/O Section						
V_{IH_HALL}	Hall Signals Input High-Level		4.0			V
V_{IL_HALL}	Hall Signals Input Low-Level				1.0	V
V_{HYS_HALL}	Hall Signals Hysteresis Voltage		2.0	2.5	3.0	V
t_{DEB_HALL}	Hall Signals De-bounce Time			5		µs
R_{DIO_UP}	Digital I/O Internal Pull High Resistor		150	200	250	kΩ
High-Voltage I/O Section						
V_{OH_PWM}	PWM Signals Output High-Level (U/V/W/X/Y/Z)	V_{PP} = 12 V, I_O = 4 mA	10			V
V_{OL_PWM}	PWM Signals Output Low-Level (U/V/W/X/Y/Z)	V_{PP} = 12 V, I_O = 4 mA			1	V
V_{OH_HOVP}	HOVP Output High-Level	V_{PP} = 12 V, I_O = 1 mA	9.0	9.7	10.0	V
V_{OL_HOVP}	HOVP Output Low-Level	V_{PP} = 12 V, I_O = 1 mA			1	V
PWM Control Section						
V_{FD}	Full Duty Voltage of DUTY Pin		4.0	4.3	4.6	V
V_{ZD}	Zero Duty Voltage of DUTY Pin			0.7		V
t_{PWM_MIN}	PWM Minimum On Time	R_CLK = 12 kΩ		1		µs
t_{DEAD0}	PWM Dead Time 3 µs	DTS = LOW	2.15	2.88	3.45	µs
t_{DEAD1}	PWM Dead Time 4 µs	DTS = HIGH	3.35	3.91	4.65	µs
f_{PWM_20K}	PWM Frequency 20 kHz	R_CLK = 12 kΩ	18.5	20.0	21.5	kHz
I_{SOURCE_OPO}	Current Source Capability of OPO Pin	IP = 5 V, IN = 0 V, OPO = 0 V	4.0	5.0	6.0	mA
I_{SINK_OPO}	Current Sink Capability of OPO Pin	IP = 0 V, IN = 5 V, OPO = 5 V	-4.0	-5.0	-6.0	mA
Av_{ERR}	Gain of Torque Error Amplifier			60		dB
GBW_{ERR}	Unit-Gain Bandwidth of Torque Error Amplifier			10		MHz
Sine Wave PWM Generator						
V_{SIN_ENA}	Sine Wave Enable Threshold of DUTY Pin			0.75		V
V_{SIN_DIS}	Sine Wave Disable Threshold of DUTY Pin			0.65		V
t_{SIN_ENA}	Sine Wave Enable Debounce Time			1		ms
t_{SIN_DIS}	Sine Wave Disable Debounce Time			100		ms

Continued on the following page...

Electrical Characteristics (Continued)

V_{PP} = 12 V and T_A = 25°C unless otherwise noted.

| Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Over-Current Protection Section						
V_{OCP_SH}	Short-Circuit Current Protection Threshold Voltage			2.5		V
V_{OCP_CYC}	Cycle-by-Cycle Current Protection Threshold Voltage			1.5		V
V_{OCP_OL}	Overload Current Protection Threshold Voltage			1.4		V
V_{OC_TMR}	OC_TMR Threshold Voltage			2.5		V
I_{TMR_CHG}	OC_TMR Charge Current	OC_TMR = 0 V	30	40	50	µA
I_{TMR_DIS}	OC_TMR Discharge Current	OC_TMR = 5 V	5	10	15	µA
$I_{BIAS\_I\_IN}$	Bias Current of I_IN	R_{I_IN} = 10 kΩ	40	50	60	µA
$I_{O\_I\_FB}$	I_FB Output Current			0.5		mA
G_{I_FB}	I_FB Output Gain			8		
Over- / Under-Voltage Protection (OVP/UVP) Section						
V_{OV_VPP}	System OVP Threshold Voltage			18		V
$V_{OV\_VPP\_RLS}$	System OVP Release Voltage			17		V
t_{OV_VPP}	System OVP Debounce Time			100		µs
V_{UV_VPP}	System UVP Threshold Voltage		7.5	8.0	8.5	V
$V_{UV\_VPP\_RLS}$	System UVP Release Voltage		8.5	9.0	9.5	V
V_{UV_VOUT}	V_{OUT} UVP Threshold Voltage			4		V
$V_{UV\_VOUT\_RLS}$	V_{OUT} UVP Release Voltage			4.5		V
V_{OV_MOTOR}	Motor Drive Voltage OVP Threshold Voltage		4.3	4.5	4.8	V
V_{RL_MOTOR}	Motor Drive Voltage OVP Release Voltage			4.0		V
Over-Temperature Protection (OTP) Section						
V_{RT}	OTP Threshold Voltage		0.9	1.0	1.1	V
V_{RT_RLS}	OTP Release Voltage		1.15	1.20	1.25	V
I_{RT}	RT Pin Source Current		40	50	60	µA
Pin Open / Short Protection Section						
V_{SHORT}	Pin Short Protection Level	R_CLK Pin		0.2		V
V_{OPEN}	Pin Open Protection Level	R_CLK and RT Pins	4.6	4.8	5.2	V

Typical Performance Characteristics
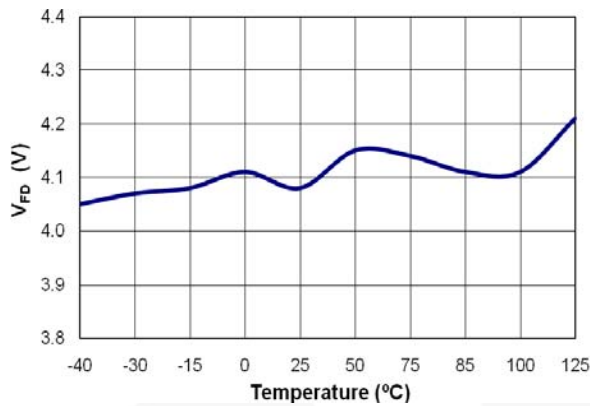
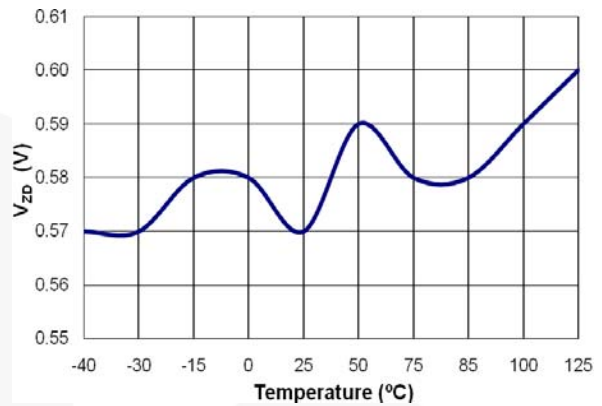**Figure 5. PWM-Full Duty Voltage (V_{FD}) vs. Temperature**

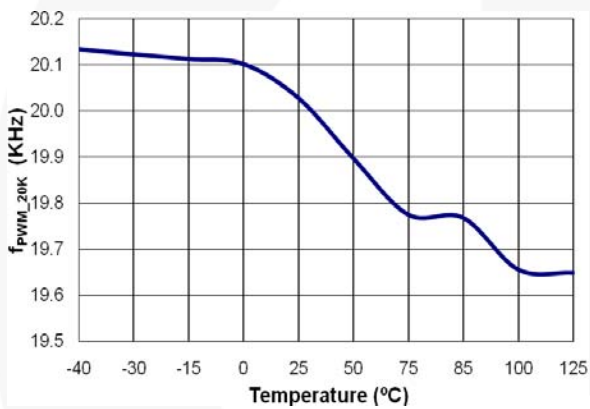**Figure 6. PWM Zero-Duty Voltage (V_{ZD}) vs. Temperature**

Figure 7. PWM Frequency 20 kHz (f_{PWM_20K}) vs. Temperature
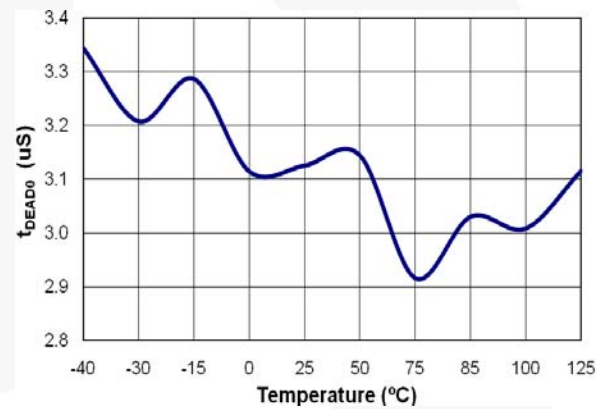
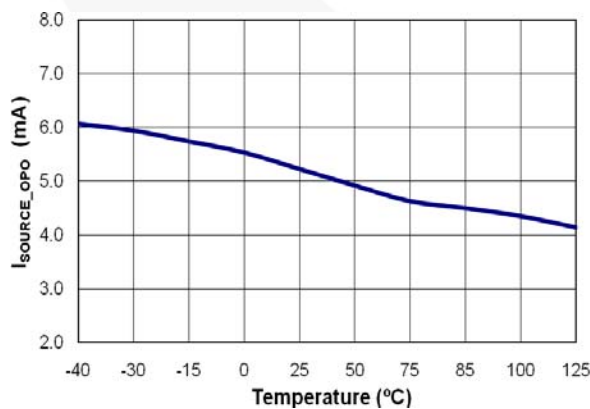**Figure 8. PWM Dead Time 3 µs (t_{DEAD0}) vs. Temperature**

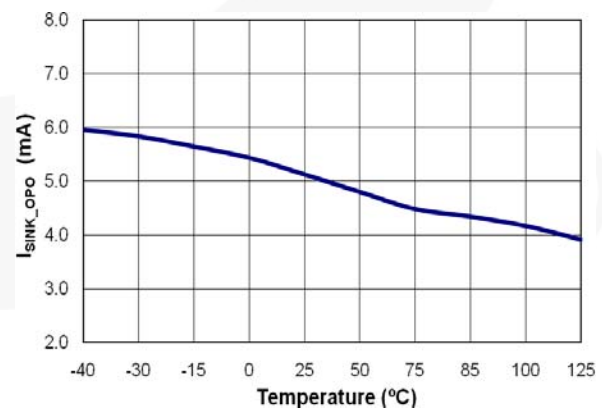**Figure 9. OPO Current Source (I_{SOURCE_OPO}) vs. Temperature**

Figure 10. OPO Current Sink (I_{SINK_OPO}) vs. Temperature

Typical Performance Characteristics (Continued)
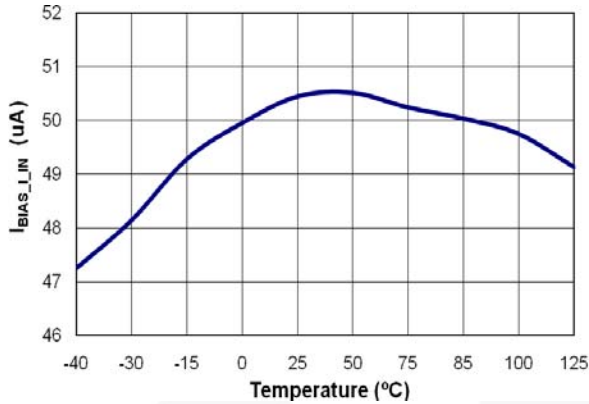

Figure 11.   I_IN Bias Current ($I_{BIAS\_I\_IN}$)
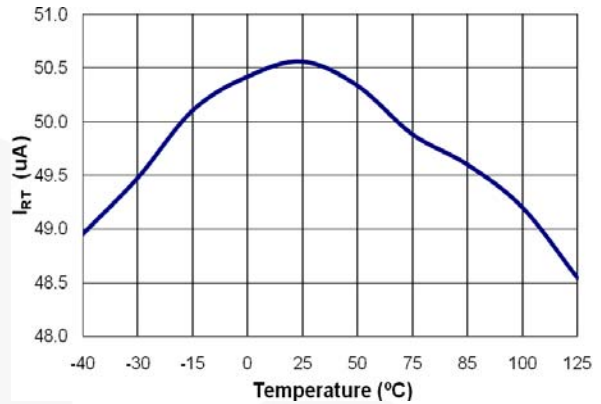vs. Temperature

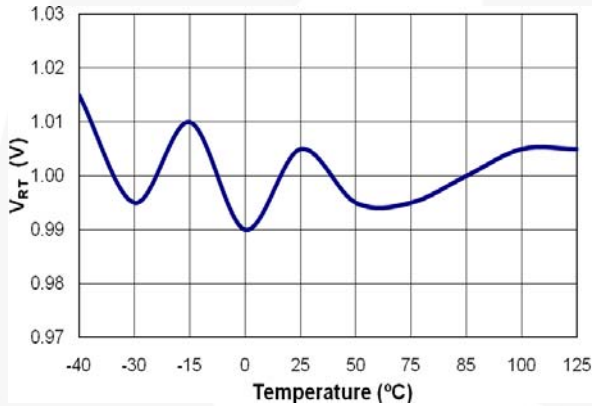Figure 12.   RT Current Source (I_{RT})
vs. Temperature

Figure 13.   OTP Threshold Voltage (V_{RT})
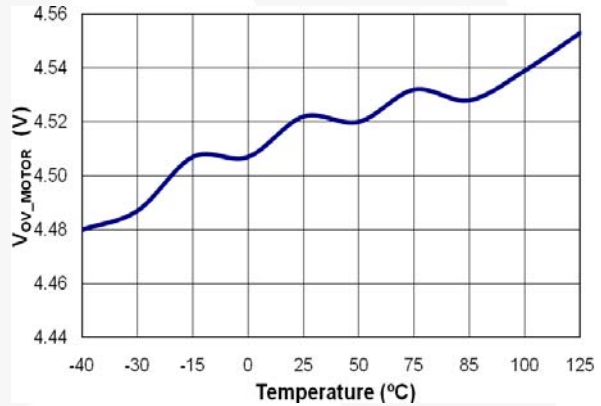vs. Temperature

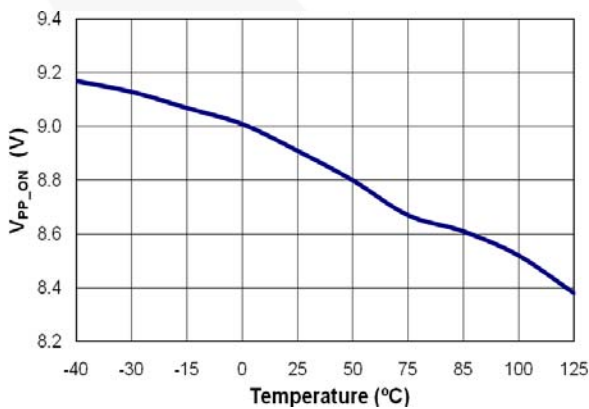Figure 14.   Motor OVP Threshold Voltage
(V_{OV_MOTOR}) vs. Temperature

Figure 15. V_{PP} Turn-On Threshold Voltage
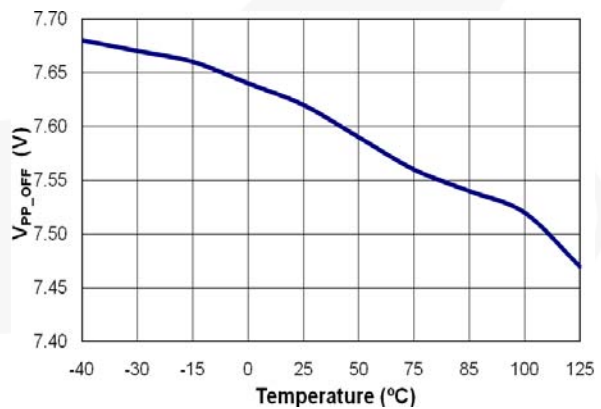(V_{PP_ON}) vs. Temperature

Figure 16. V_{PP} Turn-Off Threshold Voltage
(V_{PP_OFF}) vs. Temperature

Functional Description

Power Management and Regulator

FCM8202 can operate in a wide input voltage (V_{PP}) range from 10 V to 17.5 V. The VOUT pin is the output terminal of an internal voltage regulator. The typical output voltage range is between 5.0 V to 5.2 V. To stabilize the VOUT circuit, an external capacitor must be connected closely between this terminal and the ground. If the V_{PP} voltage is lower than the 8 V threshold, the FCM8202 is shut down and the internal registers are reset.

Clock Generator

FCM8202 comes with a programmable oscillator. Being determined by an externally added resistor, the system clock, R_CLK, can be programmed from 960 kHz to 1920 kHz. The switching frequency of the PWM signal is equal to 1/64 (divided by 64) of the system clock. Therefore, when the system clock is configured as 960 kHz, PWM is 960 kHz / 64 = 15 kHz. Similarly, if a 20 kHz PWM is intended, the system clock should be set as 1.28 MHz.

PWM Commutation

FCM8202 supports both square-wave PWM and sine-wave PWM for the BLDC motor control. The controller comes with the Hall-sensor design used to align the rotor position of the motor. For Square-Wave Mode, the PWM output commutation is shown at Table 1.

Table 1. Square Wave Commutation

CW	Hall	Hall	U-V-W	X-Y-Z
X	000	0	0-0-0	0-0-0
X	111	7	0-0-0	0-0-0
1	001	1	P-0-0	Pb-1-0
1	011	3	0-0-P	0-1-Pb
1	010	2	0-0-P	1-0-Pb
1	110	6	0-P-0	1-Pb-0
1	100	4	0-P-0	0-Pb-1
1	101	5	P-0-0	Pb-0-1
0	101	5	0-0-P	1-0-Pb
0	100	4	0-0-P	0-1-Pb
0	110	6	P-0-0	Pb-1-0
0	010	2	P-0-0	Pb-0-1
0	011	3	0-P-0	0-Pb-1
0	001	1	0-P-0	1-Pb-0

Note:
1. P = PWM, Pb = PWM inverse.
2. X = don't care.

HALL Signals Input

FCM8202 provides a 3 ~ 6 µs debounce time for each Hall signal input to reduce the glitch of the Hall signals. When the transition of the Hall signal is slow, a glitch might be produced and an error follow. Through a built-in Hall signal debounce circuit, FCM8202 minimizes the risk of the glitches and related errors.

PWM Duty Cycle and Operation

The PWM duty is proportional to the voltage levels on the OPO pin and DUTY pin. A FREE/nST pin is utilized to enable the PWM signals. When FREE/nST pin is set as logic HIGH, the PWM state is in Free Mode and all PWM outputs (U, V, W, X, Y, Z pins) are logic LOW. Once the FREE/nST pin goes logic LOW, the FCM8202 starts operating the PWM.

Sine-Wave Generator

FCM8202 includes space vector modulation (SVM) for the sine-wave PWM. An angle-detect circuit phase-locks the rotor position using the Hall signals of the motor. The resolution is 32 steps per 60°. Through the PWM operation, the motor current of each phase is sine-wave. The angle shift between each phase is 120°.
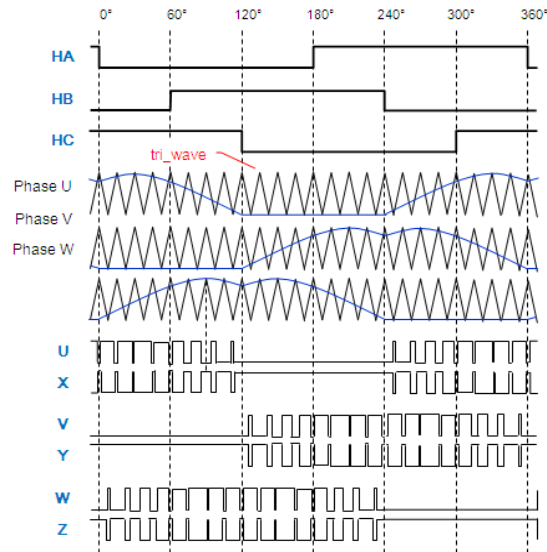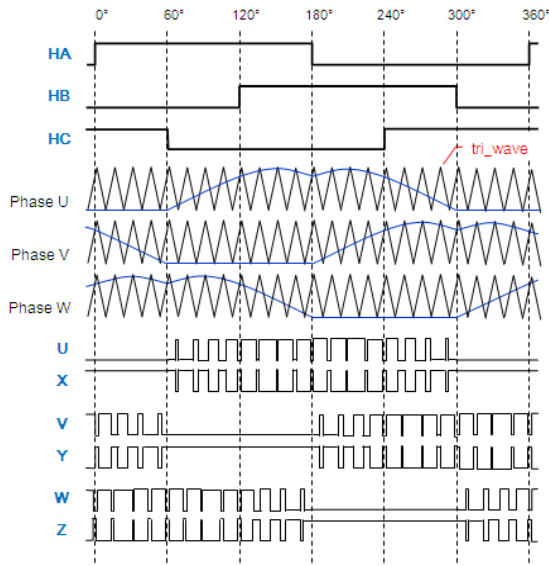

Figure 17. Sine-Wave Output at CW = 1

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Figure 18. Sine-Wave Output at CW = 0

Current Feedback and Protections

The current feedback circuit performs two major functions: (1) for generating a current feedback signal for the motor control (2) for the over-current protection. The I_IN pin outputs 50 µA current to provide a DC bias on the I_IN terminal to prevent a negative voltage. Equation 1 shows the I_FB and the I_IN. A 0.5 V DC bias on I_IN is recommended. The maximum average current signal is 1 V. By using these parameters, the maximum I_FB signal swing is 0.5 V ~ 4.5 V.

$$V_{I\_FB} = (V_S \times 8) + (I_{BIAS\_I\_IN} \times R_{BIAS}) \qquad (1)$$

Figure 19. Current Feedback Flow

FCM8202 provides three levels of over-current protection (OCP). The first level is 1.4 V, is used for overload current protection with the OCP timer delay. If the I_IN is higher than 1.4 V, the OC timer is triggered. The OC_Latch is enabled once the timer is exceeds its time-out limit. The second level is 1.5 V, used for the cycle-by-cycle current limit. The PWM signal is turned off immediately when the I_IN is > 1.5 V. The third level is 2.5 V, designed for short-circuit protection. If the I_IN is > 2.5 V for over three PWM pulses, all PWM outputs (U, V, W, X, Y, Z pins) are turned off.

Protections and Faults

Table 2. Faults Table

Type	State	Trigger	Release
V_{PP} OV	Free	$V_{PP} > 18$ V	$V_{PP} < 17$ V
V_{PP} UV	Free, Reset	$V_{PP} < 8$ V	$V_{PP} > 9$ V
V_{OUT} UV	Free	$V_{OUT} < 4$ V	$V_{OUT} > 4.5$ V
RT	Free	$R_T < 1.0$ V	$R_T > 1.2$ V
OS	Free	Open and Short	FREE/nST ↗
Hall Error	Free	Hall = 000 or 111	
HOVP	Free	$V_{SENSE} > 4.5$ V	$V_{SENSE} < 4.0$ V
OC_Latch	Free	I_IN > 1.4 V	FREE/nST ↗
SHORT	Free	I_IN > 2.5 V	FREE/nST ↗

Physical Dimensions

```
        9.0
        7.0

    D

    24          17
  25              16
A                       B

                 7.0
                 9.0

  32              9
   1              8

PIN #1 IDENT
TOP VIEW
```

| △ | 0.20 | C | A-B | D |

ALL LEADTIPS

```
                 8.70
  0.80

                 8.70

  1.80

          0.45
```

LAND PATTERN
RECOMMENDATION

```
1.45
1.35        SEE DETAIL A
              0.8
              32X

C    SEATING PLANE

      0.45
      0.30
  7.1  32X
  6.9
```

| ⊕ | 0.20 Ⓜ | C | A-B | D |

SIDE VIEW

NOTES:

A) CONFORMS TO JEDEC MS-026 VARIATION BBA
B) ALL DIMENSIONS IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME
   Y14.5M-1994.
E) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
   FLASH, AND TIE BAR PROTRUSIONS.
F) LANDPATTERN STANDARD:
   QFP80P900X900X160-32BM.
G) DRAWING FILE NAME: MKT-VBE32AREV2

```
                R0.08 MIN
R0.08-0.20                    12° TOP & BOTTOM
         0.25
GAGE PLANE                         1.6 MAX

                    0.20 MIN
  0.75
  0.45                        0.15
  1.0                         0.05
                          | △ | 0.10 | C |
                DETAIL A
```
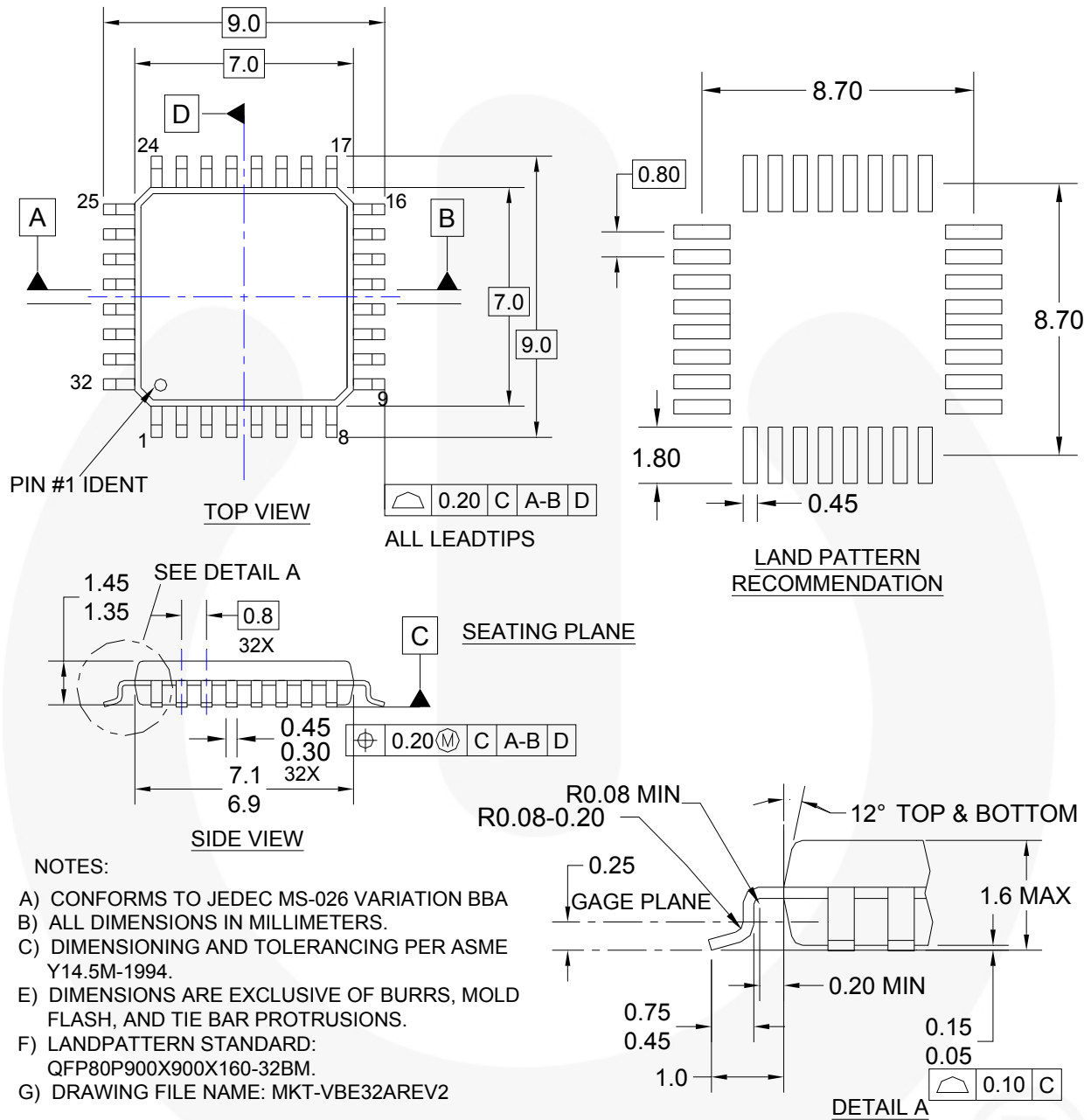
Figure 20. 32-Low-Profile, Quad Flat Pack Package (LQFP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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http://www.fairchildsemi.com/packaging/.

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AccuPower™	F-PFS™	®	SYSTEM GENERAL℠
AX-CAP®*	FRFET®	PowerTrench®	
BitSiC™	Global Power Resource℠	PowerXS™	TinyBoost™
Build it Now™	GreenBridge™	Programmable Active Droop™	TinyBuck™
CorePLUS™	Green FPS™	QFET®	TinyCalc™
CorePOWER™	Green FPS™ e-Series™	QS™	TinyLogic®
CROSSVOLT™	Gmax™	Quiet Series™	TINYOPTO™
CTL™	GTO™	RapidConfigure™	TinyPower™
Current Transfer Logic™	IntelliMAX™	℗™	TinyPWM™
DEUXPEED®	ISOPLANAR™	Saving our world, 1mW/W/kW at a time™	TinyWire™
Dual Cool™	Making Small Speakers Sound Louder and Better™	SignalWise™	TranSiC™
EcoSPARK®		SmartMax™	TriFault Detect™
EfficientMax™	MegaBuck™	SMART START™	TRUECURRENT®*
ESBC™	MICROCOUPLER™	Solutions for Your Success™	μSerDes™
	MicroFET™	SPM®	
ℱ®	MicroPak™	STEALTH™	μSerDes™
Fairchild®	MicroPak2™	SuperFET®	UHC™
Fairchild Semiconductor®	MillerDrive™	SuperSOT™-3	Ultra FRFET™
FACT Quiet Series™	MotionMax™	SuperSOT™-6	UniFET™
FACT®	mWSaver™	SuperSOT™-8	VCX™
FAST®	OptoHiT™	SupreMOS®	VisualMax™
FastvCore™	OPTOLOGIC®	SyncFET™	VoltagePlus™
FETBench™	OPTOPLANAR®		XS™

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As used herein:

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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