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August 2014

FCMT199N60

N-Channel SuperFET® II MOSFET

600 V, 20.2 A, 199 mΩ

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- $R_{DS(on)} = 170\text{ m}\Omega$ (Typ.)
- Ultra Low Gate Charge (Typ. $Q_g = 57\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 160\text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant

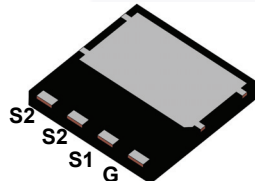
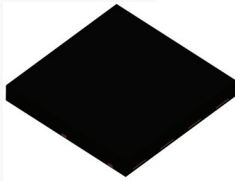
Applications

- Server and Telecom Power Supplies
- Solar Inverters
- Adaptors

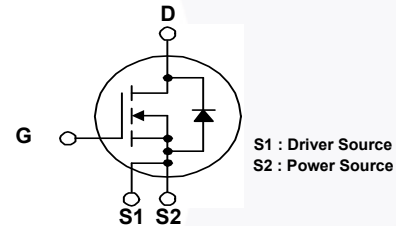
Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as server/telecom power, adaptor and solar inverter applications.

The Power88 package is an ultra-slim surface-mount package (1 mm high) with a low profile and small footprint ($8 \times 8\text{ mm}^2$). SuperFET II MOSFET in a Power88 package offers excellent switching performance due to lower parasitic source inductance and separated power and drive sources. Power88 offers Moisture Sensitivity Level 1 (MSL 1).



Power88



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCMT199N60	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	-DC	± 20
		-AC ($f > 1\text{ Hz}$)	± 30
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	20.2
		-Continuous ($T_C = 100^\circ\text{C}$)	12.7
I_{DM}	Drain Current - Pulsed (Note 1)	60.6	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	400	mJ
I_{AR}	Avalanche Current (Note 1)	4.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	2.1	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
	MOSFET dv/dt	100	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	208	W
		- Derate above 25°C	1.67
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCMT199N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (* 1 in ² pad of 2 oz copper), Max.	45	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCMT199N60	FCMT199N60	Power88	-	-	3000

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_C = 150^\circ\text{C}$	650	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.67	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	2.2	-	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.170	0.199	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	-	20	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	2043	2715	pF
C_{oss}	Output Capacitance		-	45	60	pF
C_{rSS}	Reverse Transfer Capacitance		-	7	-	pF
$C_{oss\ eff.}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	160	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}$	-	57	74	nC
Q_{gs}	Gate to Source Gate Charge		-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	21	-
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	1	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$	-	20	50	ns
t_r	Turn-On Rise Time		-	10	30	ns
$t_{d(off)}$	Turn-Off Delay Time		-	64	138	ns
t_f	Turn-Off Fall Time		(Note 4)	-	5	20

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	20.2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60.6	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A}$	-	320	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	5.1	-	μC

Notes:

1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
2. $I_{AS} = 4\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 10\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature typical characteristics.

Typical Characteristics

Figure 1. On-Region Characteristics

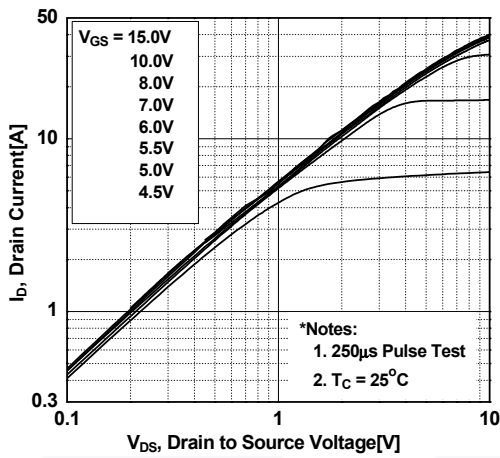


Figure 2. Transfer Characteristics

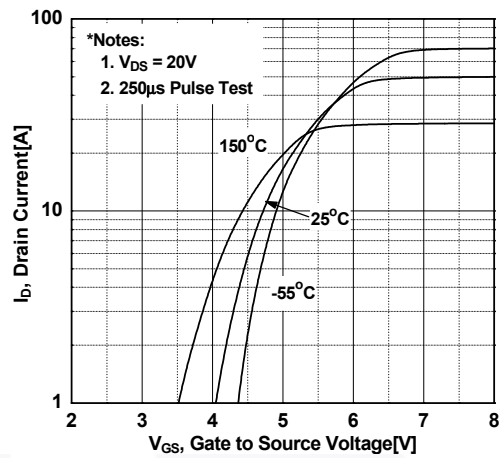


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

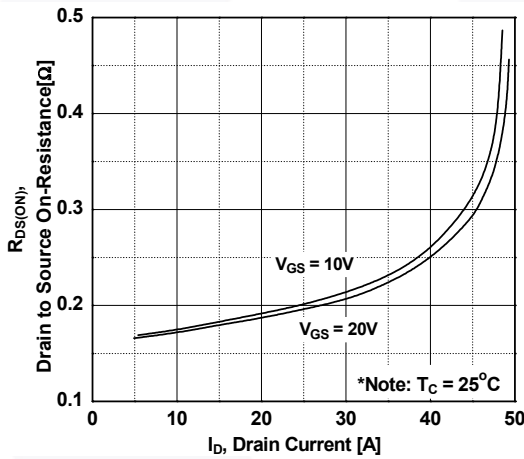


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

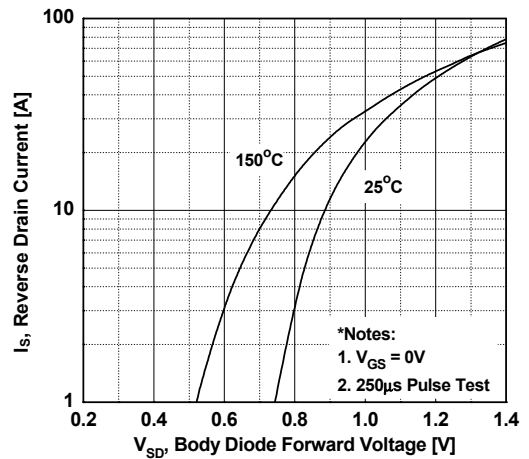


Figure 5. Capacitance Characteristics

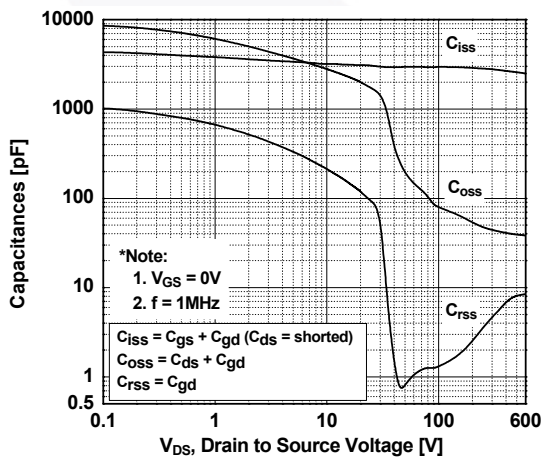
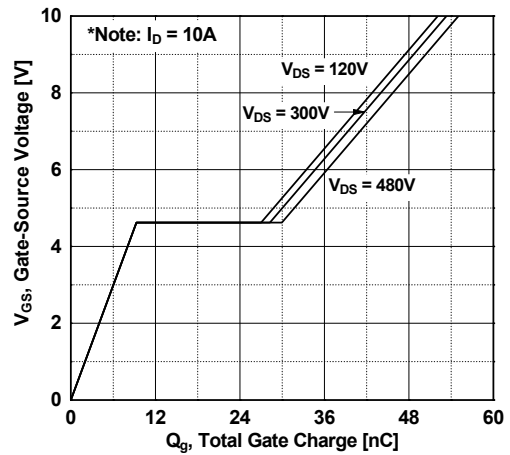


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

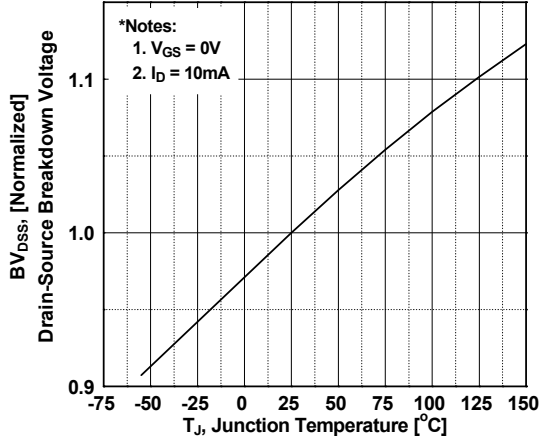


Figure 8. On-Resistance Variation vs. Temperature

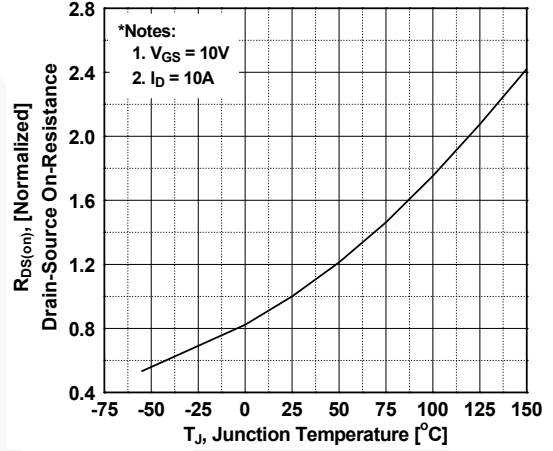


Figure 9. Maximum Safe Operating Area

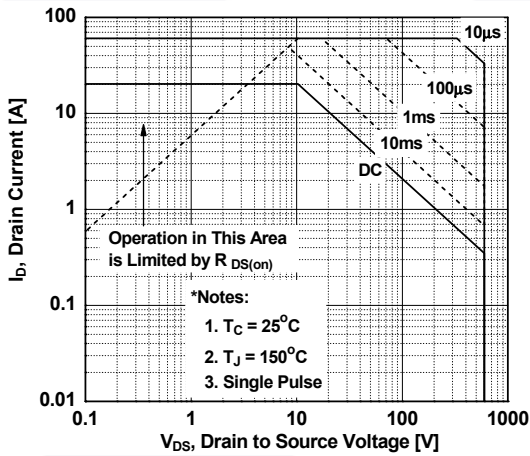


Figure 10. Maximum Drain Current vs. Case Temperature

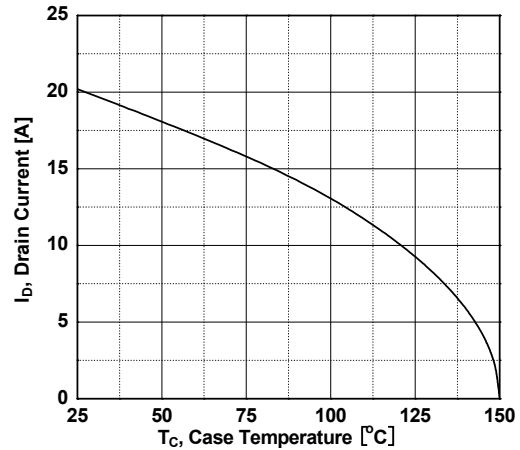
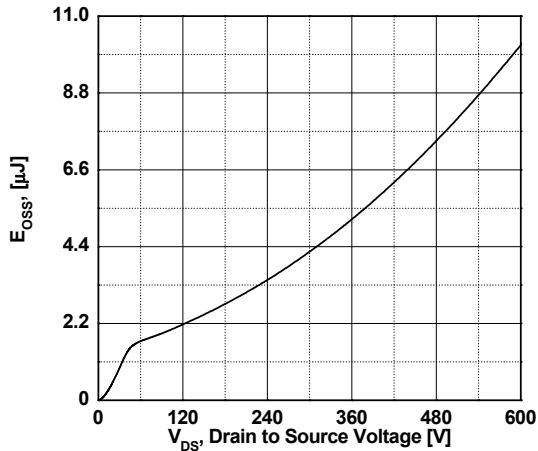
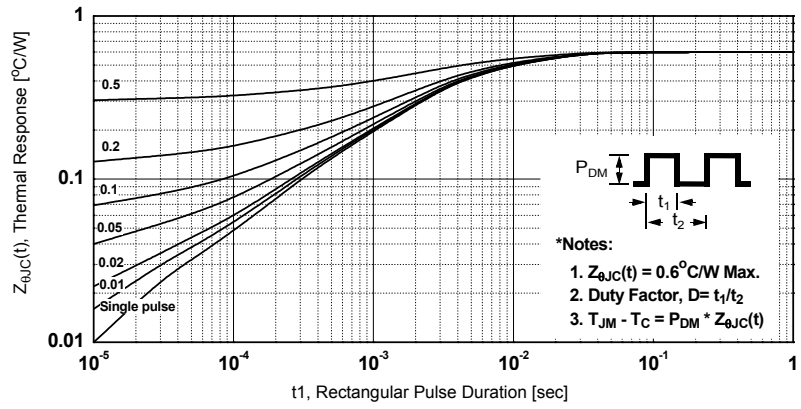


Figure 11. E_oss vs. Drain to Source Voltage Switching Capability



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



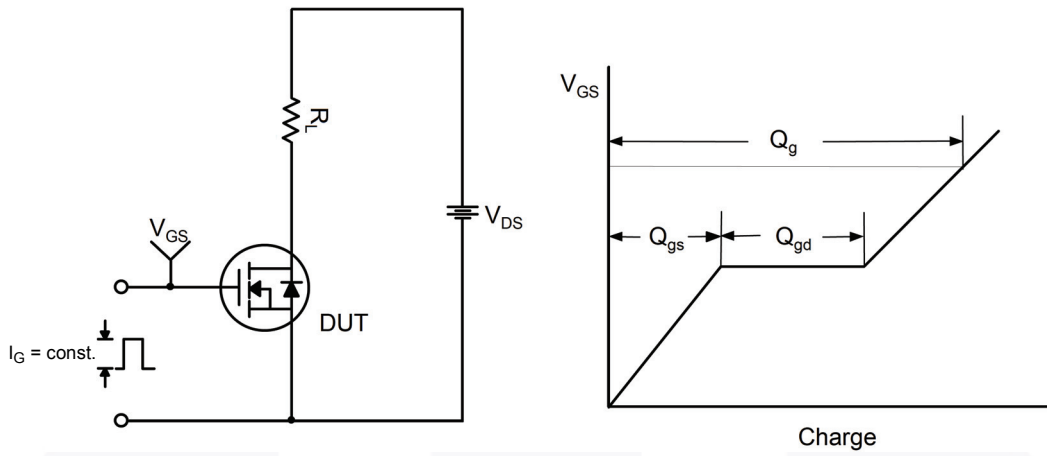


Figure 13. Gate Charge Test Circuit & Waveform

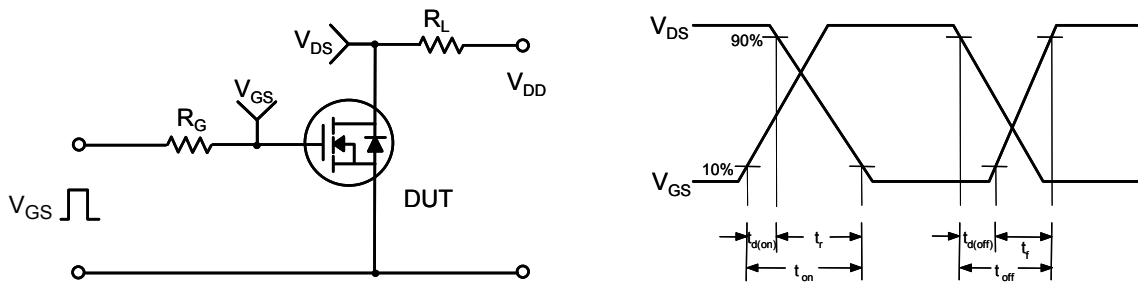


Figure 14. Resistive Switching Test Circuit & Waveforms

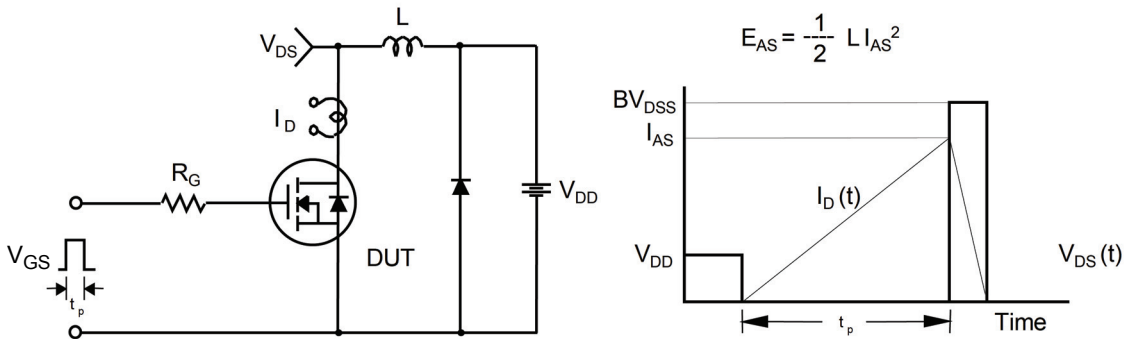
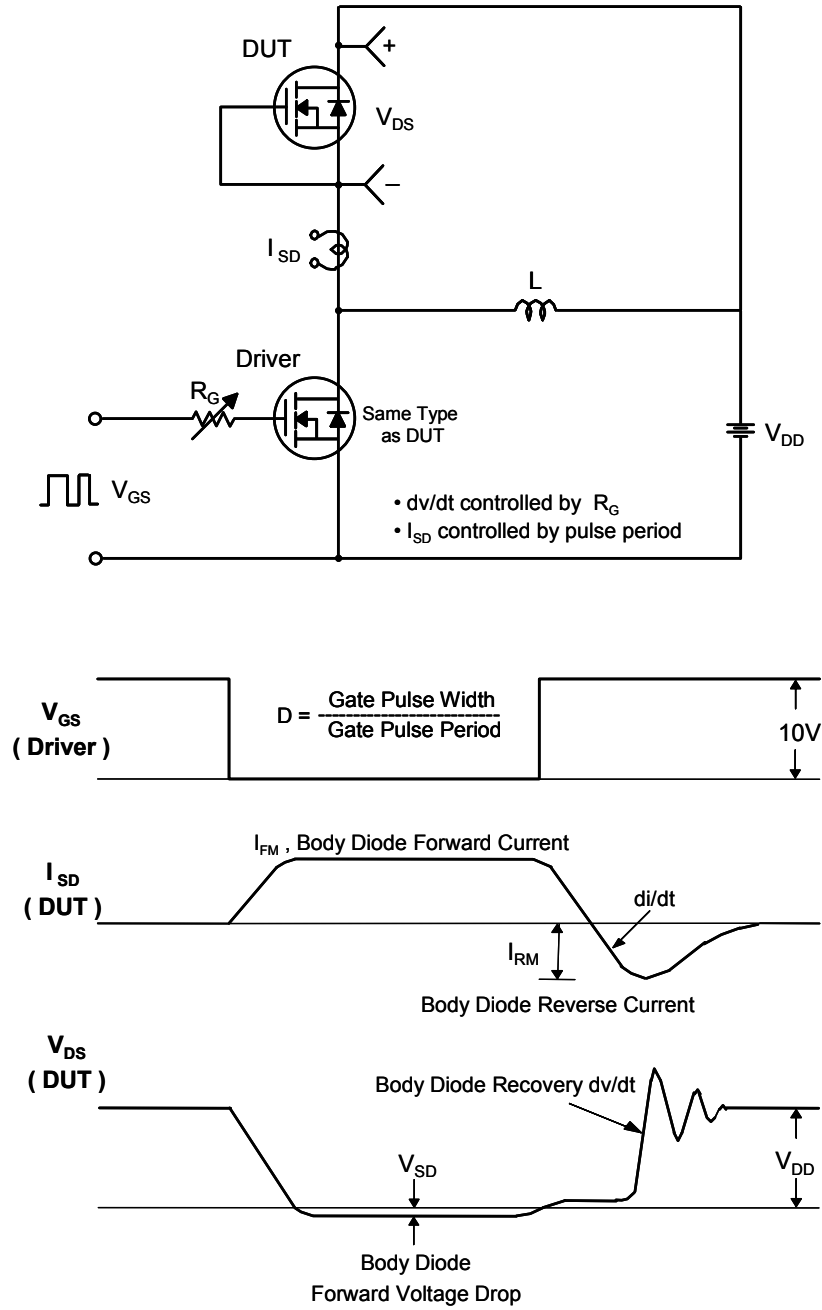


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

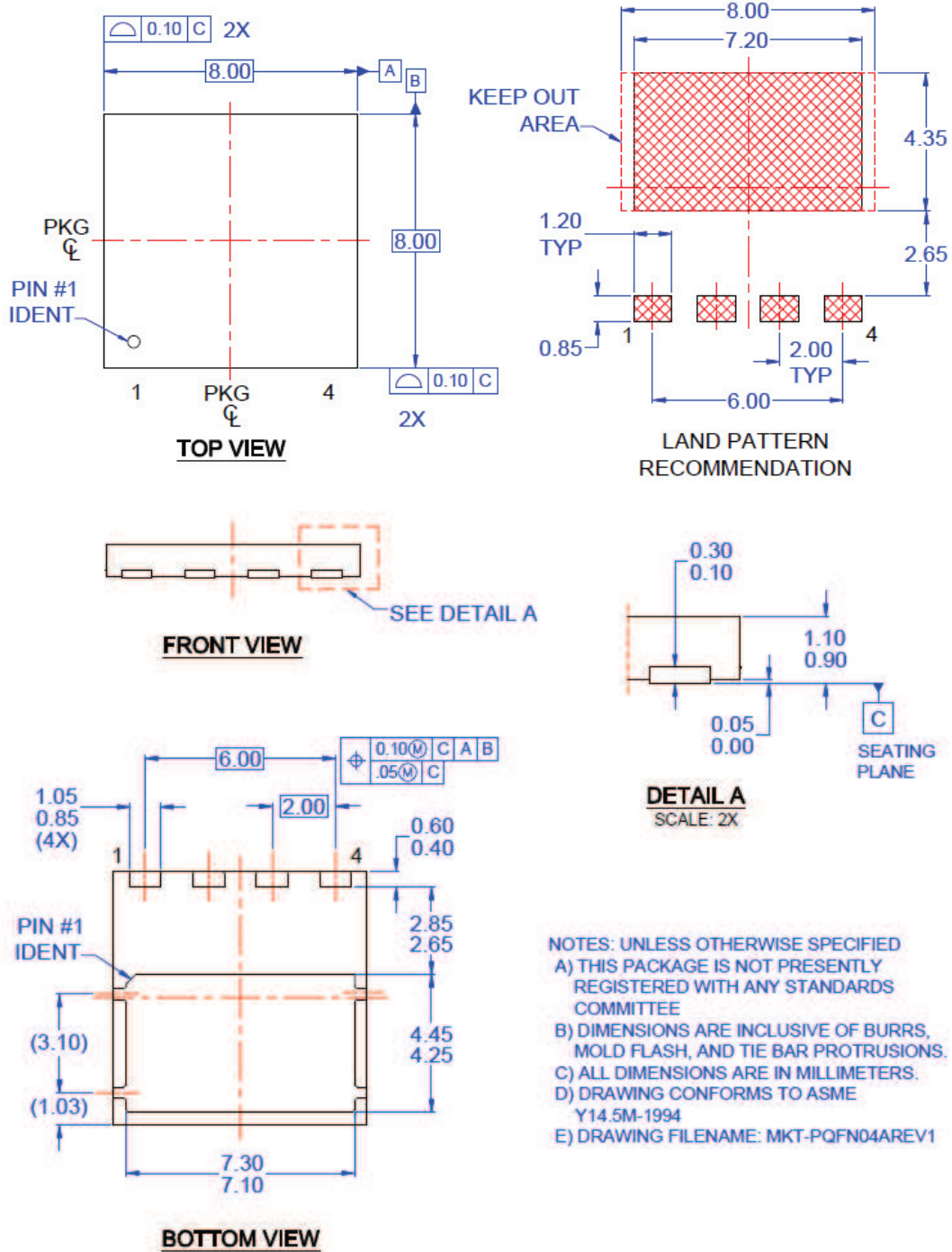


Figure 17. Molded Package, Power88, 4 Lead

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