Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

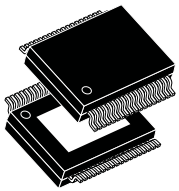
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

FDA803D

1 x 45 W class D digital input automotive power amplifier with diagnostics, wide voltage operation range for car audio and telematic

Datasheet - production data



PowerSSO-36
(Exp. pad down)

GADG2111170824PS

Features

- AEC-Q100 qualified
- Integrated 108 dB D/A conversion
- I^2S and TDM digital input (4/8/16CH TDM)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Full I^2C bus driving (3.3/1.8 V)
- CISPR 25 - Class V (Fourth edition)
- Very low quiescent current
- Output lowpass filter included in the feedback allowing outstanding audio performances
- Wide operating supply range from 3.3 to 18 V, suitable for car radio, telematics and e-call
- MOSFET power outputs allowing high output power capability
  - 1 x 25 W /4 Ω @ 14.4 V, 1 kHz THD = 1%
  - 1 x 30 W /4 Ω @ 14.4 V, 1 kHz THD = 10%
- 2 Ω loads driving
- Power limiting function (configurable through I^2C)
- I^2C bus diagnostics:
  - Short to V_{CC}/GND
  - Short load and open load detection (also in play mode)
  - Four thermal warnings
- DC offset detector (also in play) and 'hot spot' detection
- Clipping detector
- Integrated thermal protection
- Legacy mode ('no I^2C' mode), 4 configurable settings
- Short circuit and ESD integrated protections
- Package: PowerSSO-36 exposed pad down

Table 1. Device summary

Order code	Package	Packing
FDA803D-EHT	PowerSSO-36 (exposed pad down)	Tape & reel
FDA803D-EHX		Tube

Contents

List of tables

List of figures

1 Description

The FDA803D is a single bridge class D amplifier, designed in the most advanced BCD technology, intended for any automotive audio application (car radio, telematics and e-call, noise and tone generators, etc).

The FDA803D integrates a high performance D/A converter together with powerful MOSFET outputs in class D, so it is very compact and powerful, moreover reaches outstanding efficiency performances (90%).

It has a very wide operating range: it can be operated both with standard car battery levels (5.5-18 V operating, compatible to load dump pulse) and with external step-down generated voltages or emergency battery (since it is compatible to minimum 3.3 V operative).

The feedback loop is including the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion.

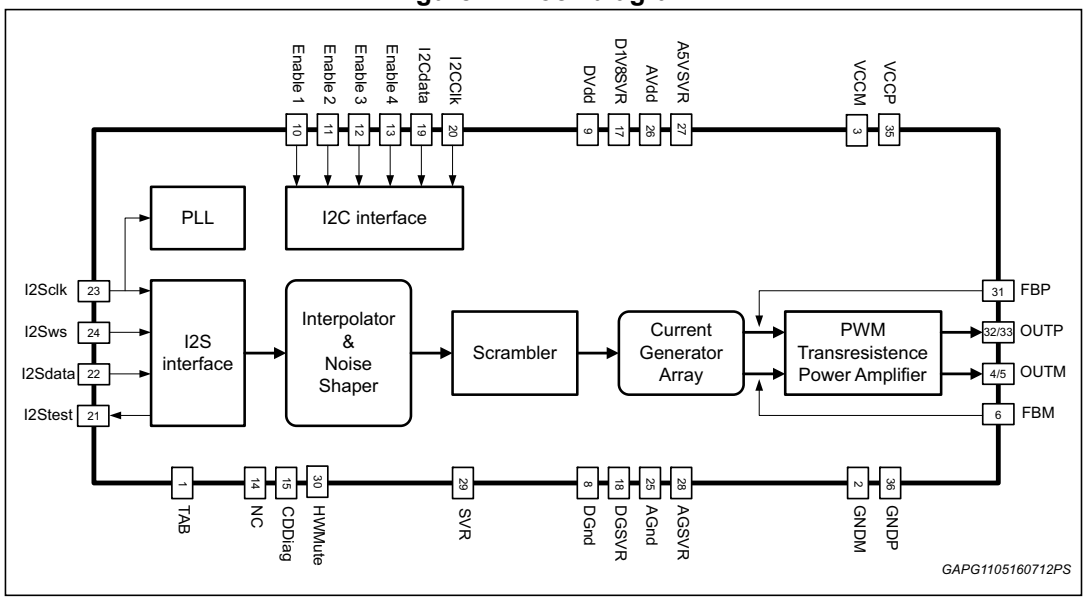
FDA803D is configurable through I^2C bus interface and is integrating a complete diagnostics array specially intended for automotive applications including innovative open load and DC offset detection in play mode.

Thanks to the solutions implemented to solve the EMI problems, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover FDA803D features a configurable power limiting function, and can be optionally operated under no I^2C mode ('legacy mode').

2 Block diagram

Figure 1. Block diagram



3 Pins description

Figure 2. Pins connection diagram

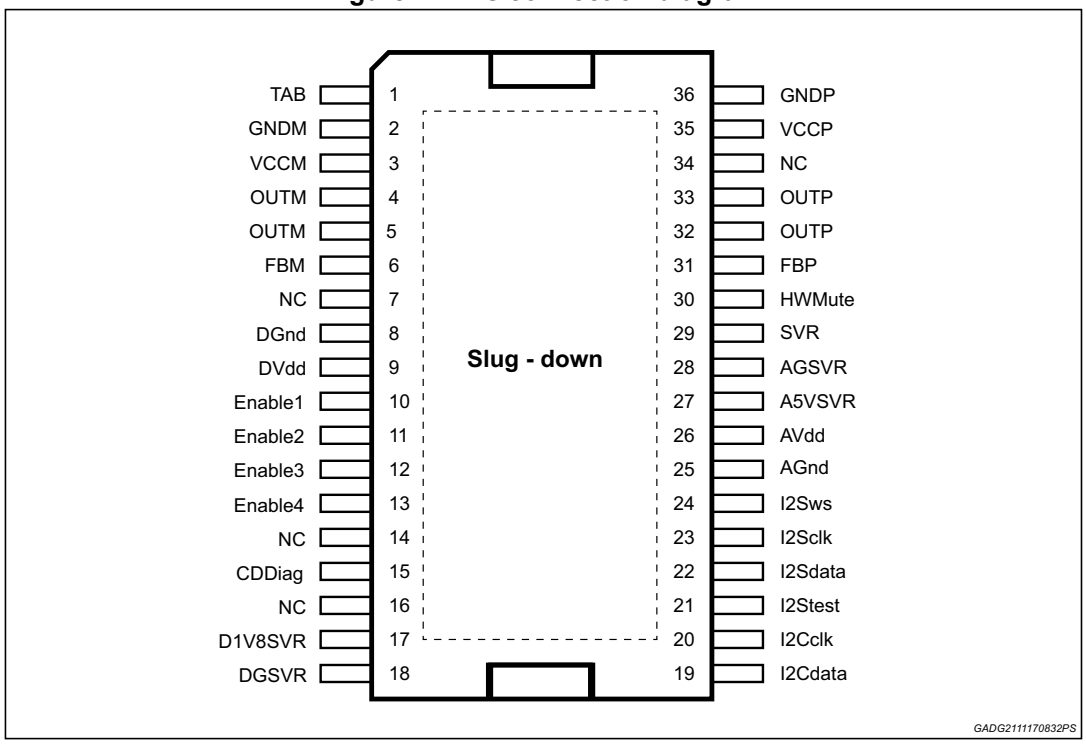


Table 2. Pins list function

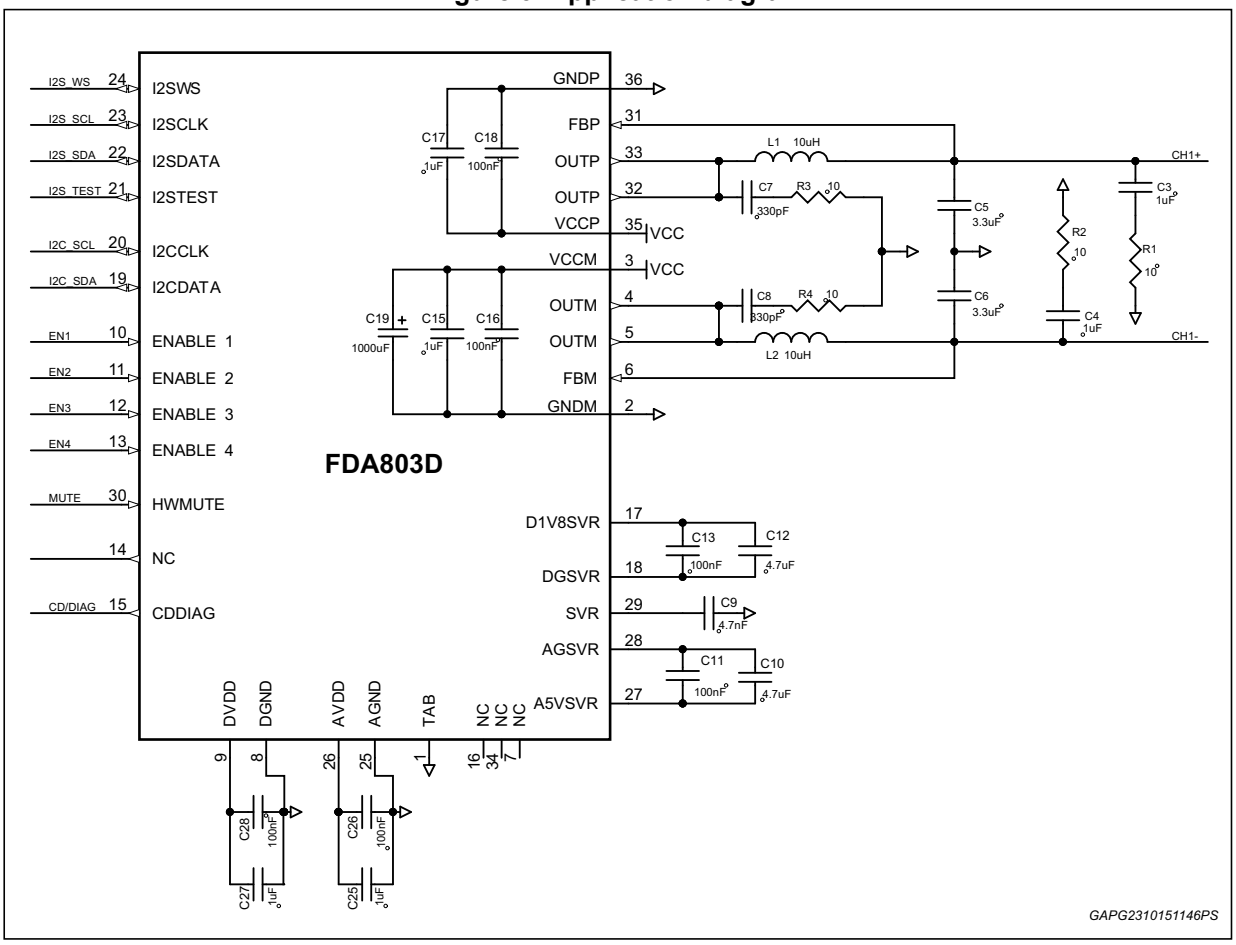
Pin #	Pin name	Function
1	TAB	Device slug connection
2	GNDM	Channel half bridge minus, Power Ground
3	VCCM	Channel half bridge minus, Power Supply
4	OUTM	Channel half bridge minus, Output
5	OUTM	Channel half bridge minus, Output
6	FBM	Channel half bridge minus, Feedback
7	NC	Not connected
8	DGnd	Digital ground
9	DVdd	Digital supply
10	Enable1	Enable 1
11	Enable2	Enable 2
12	Enable3	Enable 3
13	Enable4	Enable 4
14	NC	Not connected
15	CDDiag	Clipping detector and diagnostic output pin

Table 2. Pins list function

Pin #	Pin name	Function
16	NC	Not connected
17	D1V8SVR	Positive digital supply V(SVR)+0.9V (Internally generated)
18	DGSVR	Negative digital supply V(SVR)-0.9V (Internally generated)
19	I2Cdata	I2C Data
20	I2Cclk	I2C Clock
21	I2Stest	test pin, left open
22	I2Sdata	I2S/TDM data
23	I2Sclk	I2S/TDM Clock input
24	I2Sws	I2S/TDM Sync input /Word Select input
25	AGnd	Analog ground
26	AVdd	Analog supply
27	A5VSVR	Positive Analog Supply V(SVR)+2.5V (Internally generated)
28	AGSVR	Negative Analog Supply V(SVR)-2.5V (Internally generated)
29	SVR	Supply Voltage Ripple Rejection Capacitor
30	HWMute	Hardware mute pin
31	FBP	Channel half bridge plus, Feedback
32	OUTP	Channel half bridge plus, Output
33	OUTP	Channel half bridge plus, Output
34	NC	Not connected
35	VCCP	Channel half bridge plus, Power Supply
36	GNDP	Channel half bridge plus, Power Ground

4 Application diagram

Figure 3. Application diagram



5 Electrical specifications

5.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC} [V_{CCP} ,V_{CCM}, A_{VDD}, D_{VDD}]	DC supply voltage	-0.3 to 28	V
	Transient supply voltage for t = 100 ms(1)	-0.3 to 40	V
GND_{max} [D_{GND}, A_{GND}, GNDP, GNDM]	Ground pin voltage difference	-0.3 to 0.3	V
$I^2C_{data,}$ I^2C_{clk}	I^2C bus pins voltage	-0.3 to 5.5	V
$I^2S_{test,}$ $I^2S_{data,}$ $I^2S_{clk,}$ I^2S_{ws}	I^2S bus pins voltage	-0.3 to 5.5	V
$Enable_{1,2,3,4}$	Enables	-0.3 to 5.5	V
HWMute	Hardware mute	-0.3 to 7	V
CDDiag	Clip detection	-0.3 to 5.5	V
I_o	Output current (repetitive f > 10 Hz)	Internally limited	A
T_{amb}	Ambient operating temperature	-40 to 125	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C
ESDHBM	ESD protection HBM	2000	V
ESDCDM	ESD protection CDM	500	V

1. V_{CC} = 35 V for t < 400 ms as per ISO16750-2 load dump with centralized load dump suppression.

5.2 Thermal data

Table 4. Thermal data - PowerSSO36 slug-down package

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient (2s board)	56	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$	Thermal resistance junction-to-ambient (2s2p board)	31	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$	Thermal resistance junction-to-ambient (2s2p+vias)	26	°C/W

5.3 Electrical characteristics

V_{cc} = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; I^2C defaults, unless otherwise specified. LC filter: L = 10 µH, C = 3.3 µF. PWM in In-phase modulation, feedback connected after the filter.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage range	R_L = 4 Ω	3.3	-	18	V
		R_L = 2 Ω (1)	3.3	-	16	
I_{VCC}	Quiescent current	Device in Standby	-	1	5	µA
		Device on (MUTE state)	-	35	-	mA
		ECO MODE	-	22	-	mA
V_{os}	Offset voltage	Mute & Play	-10	-	+10	mV
D_{VDD}	Digital supply voltage range	-	3.3	-	18	V
A_{VDD}	Analog supply voltage range	-	3.3	-	18	V
I_{op}	Overcurrent protection	IB11 D5-4 = 00	9.5	11	12.5	A
		IB11 D5-4 = 01	6.7	8	9.3	A
		IB11 D5-4 = 10	5	6	7	A
		IB11 D5-4 = 11	3	4	5	A
I_{AVDD}	Analog current	Device on (MUTE state)	-	9	20	mA
I_{DVDD}	Digital current	Device on (MUTE state)	-	13	20	mA
-	Overvoltage shutdown	Attenuation = 0.5 dB(2)	18.5	19.5	20.5	V
V_{lowM}	V_{cc} low supply mute threshold	Attenuation <0.5 dB Low voltage mode (IB0D0=1)	2.7	2.9	3.3	V
		Attenuation <0.5 dB Standard mode (IB0D0=0)	4.5	4.7	5	V
V_{highM}	V_{cc} high voltage mute(2)	-	18	18.9	20.3	V
$UVLO_{VCC}$	V_{cc} supply UVLO threshold	Standard mode (IB0D0=0)	4.4	4.6	4.8	V
		Low voltage mode (IB0D0=1)	2.55	2.7	2.85	V
T_{sh}	Thermal shutdown	-	165	175	185	°C
T_{pl}	Thermal protection junction temperature	Attenuation = 0.5 dB	150	160	170	°C
T_{w1}	Thermal warning junction temperature(3)	-	-	Tpl-5	-	°C
T_{w2}		-	-	Tpl-15	-	°C
T_{w3}		-	-	Tpl-35	-	°C
T_{w4}		-	-	Tpl-50	-	°C

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Audio performances						
P_o	Output power	THD = 10 %	-	30	-	W
		THD = 1 %		25	-	W
		Max power; V_{cc} = 15.2 V	-	50	-	W
		R_L = 2 Ω THD = 10% (1)		55	-	W
		R_L = 2 Ω THD = 1% (1)	-	45	-	W
		R_L = 2 Ω, max power(1)	-	80	-	W
P_o	Output power	THD = 10% V_{cc} = 5 V	-	3.8	-	W
		THD = 10% V_{cc} = 3.3 V	-	1.6	-	W
PSRR	Power supply rejection ratio	f = 1 kHz; Vr = 1Vpk;	70	80	-	-
THD	Total harmonic distortion	P_O = 1 W, f = 1 kHz	-	0.01	0.05	%
Gain	Standard gain	at Amplitude = -10 dBFs	5.5	5.9	6.3	Vp
	Low gain(4)		3.3	3.6	3.9	Vp
DR	Dynamic range	A-wtd and brickwall 20 kHz filter	102	107.5	-	dB
SNR	Signal to noise ratio	A-wtd and brickwall 20 kHz filter	107	112	-	dB
Eout1	Output noise	A-wtd and brickwall 20 kHz filter used, no output signal;	-	35	55	µV
Eout2	Output noise	CCIR 468 filtered	-	84	130	µV
ΔV_{OITU}	ITU Pop filter output voltage	Standby to Mute and Mute to Standby transition	-7.5	-	+7.5	mV
Mute						
V_{Mth}(5)	Mute pin voltage threshold	Attenuation <0.5 dB, and digital mute disabled	2.3	-	-	V
		Attenuation ≥60 dB, and digital mute disabled	-	-	1	
I_M	Mute pin source current	-	9	11	13	µA
V_{Mcl}	Mute pin internal clamp voltage	-	5.5	6	6.5	V
I_{feed}	Peak current flowing in the feedback pins	Standby condition, all feedbacks forced to V_{cc}, output floating	-	110	130	µA
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	I2C pins low voltage	-	-	-	0.8	V
V_{IH}	I2C pins high voltage	-	1.3	-	-	V
V_{OLMAX}	Maximum I2C data pin low voltage when current I_{sink} is sinked	I_{sink} = 4 mA	-	0.12	0.5	V
I_{LIMAX}	Maximum input leakage current	V = 3.6 V	-	-	1	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I^2S bus interface						
V_{IL-I2S}	I2S pins low voltage	-	-	-	0.8	V
I_L	Input logic current, low	V_I = 0 V	-	-	500	nA
V_{IH-I2S}	I2S pins high voltage	-	1.3	-	-	V
I_H	Input logic current, high	V_I = TBD	-	-	500	nA
Control pins characteristics						
V_{ENL}	Enable pins low voltage	-	-	-	0.9	V
V_{ENH}	Enable pins high voltage	-	2.4	-	-	V
Clipping and offset detector						
CD_{THD}	Clip det THD (6)	THD @ 100 Hz with average $V_{clipdet}$ = 2 V	5	7	9	%
CDSAT	Clip det sat. voltage	CD on; I_{CD} = 1 mA	-	150	300	mV
CD_{LK}	Clip det leakage current	CD pin at 3.6 V	-	-	15	µA
V_{offlin}	Input DC offset detection threshold	Theshold at which an offset present at inputs is detected	-	-18	-	dB
V_{offout}	Output DC offset detection threshold(7)	Input high pass filter disable	±1.4	±2	±2.6	V

1. If outphase modulation selected, slow slope configuration must be used (IB11,D3)
2. Parameter values based on bench measurements (guaranteed by correlation with overvoltage shutdown).
3. The thermal warnings are always in tracking.
4. When selecting the low gain, also the thresholds for "DC diagnostic" function and "Open load in play detector" function scale of the same factor with respect to standard gain configuration.
5. See *Chapter 8: Muting function architecture* for more details.
6. Guaranteed by correlation.
7. Measured at bench during product validation.

5.4 Typical curves of the main electrical parameters

Figure 4. Efficiency and power dissipation (V_S = 14.4 V, R_L = 1 x 4 Ω, f = 1 kHz sine wave)

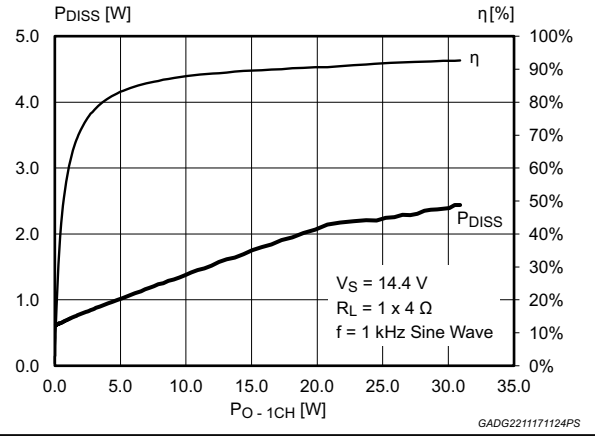


Figure 5. Efficiency and power dissipation (V_S = 14.4 V, R_L = 1 x 4 Ω, f = 1 kHz pink noise)

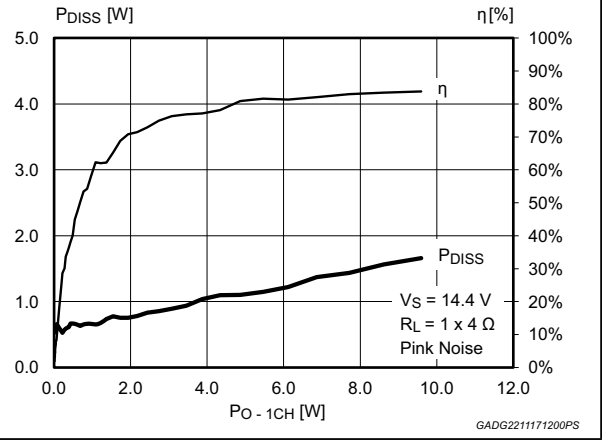


Figure 6. Efficiency and power dissipation (V_S = 14.4 V, R_L = 1 x 2 Ω, f = 1 kHz sine wave)

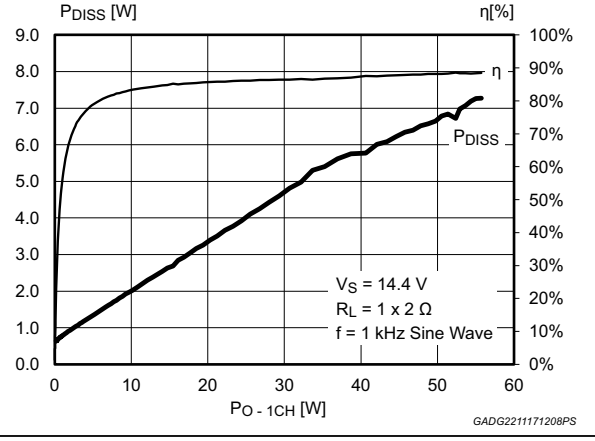


Figure 7. Efficiency and power dissipation (V_S = 14.4 V, R_L = 1 x 2 Ω, f = 1 kHz pink noise)

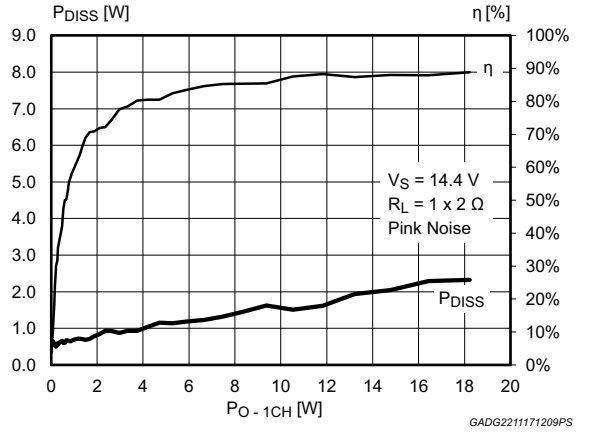


Figure 8. Efficiency and power dissipation (V_S = 14.4 V, R_L = 1 x 8 Ω, f = 1 kHz sine wave)

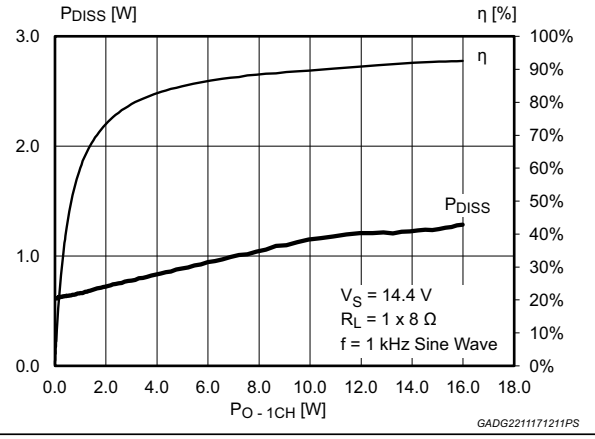


Figure 9. Efficiency and power dissipation (V_S = 14.4 V, R_L = 1 x 8 Ω, f = 1 kHz pink noise)

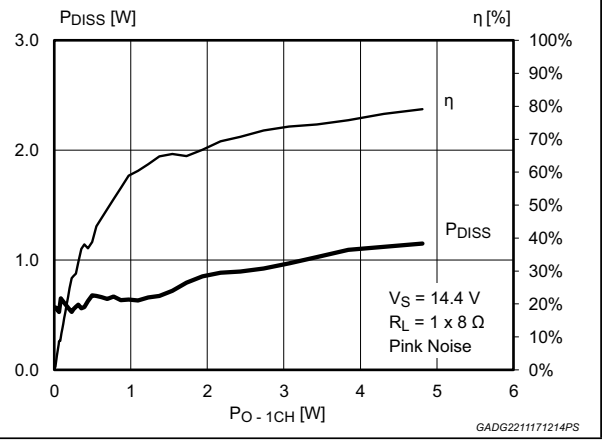


Figure 10. Efficiency and power dissipation (V_S = 18 V, R_L = 1 x 4 Ω, f = 1 kHz sine wave)

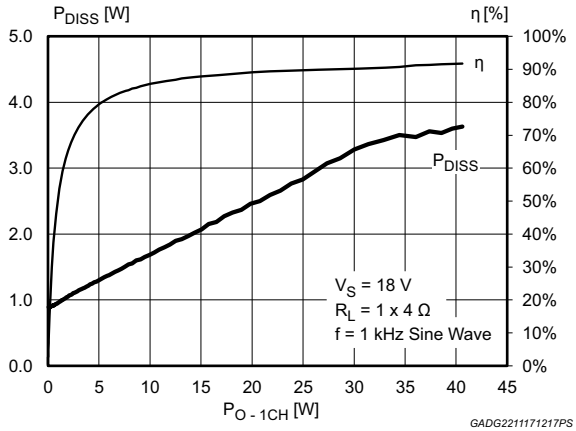


Figure 11. Efficiency and power dissipation (V_S = 18 V, R_L = 1 x 4 Ω, f = 1 kHz pink noise)

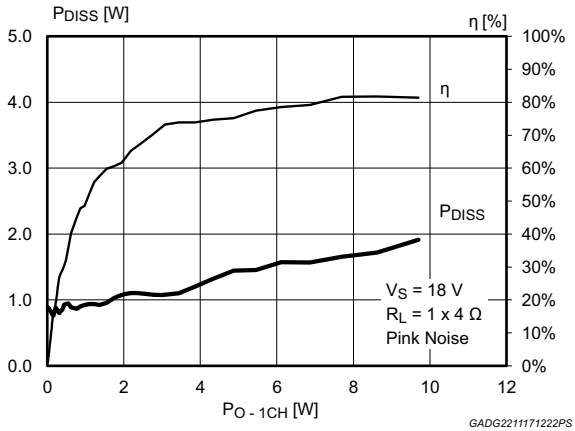


Figure 12. Efficiency and power dissipation (V_S = 16 V, R_L = 1 x 2 Ω, f = 1 kHz sine wave)

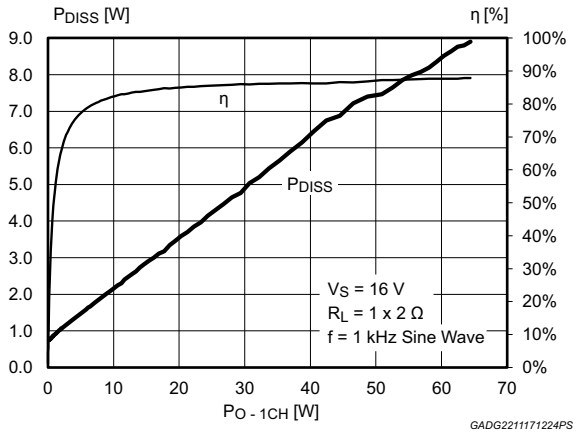


Figure 13. Efficiency and power dissipation (V_S = 16 V, R_L = 1 x 2 Ω, f = 1 kHz pink noise)

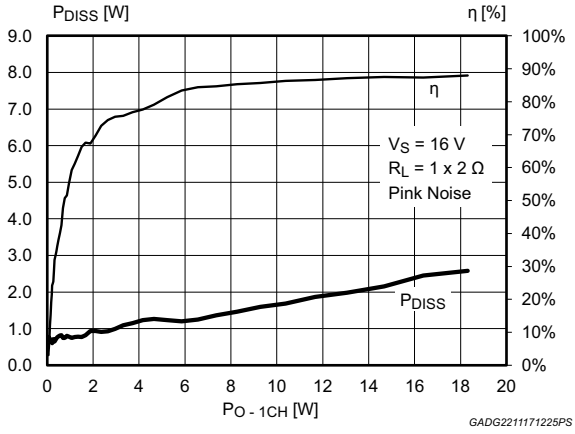


Figure 14. Efficiency and power dissipation (V_S = 18 V, R_L = 1 x 8 Ω, f = 1 kHz sine wave)

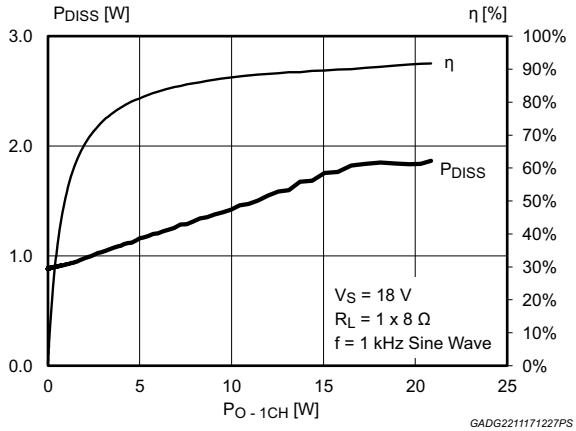


Figure 15. Efficiency and power dissipation (V_S = 18 V, R_L = 1 x 8 Ω, f = 1 kHz pink noise)

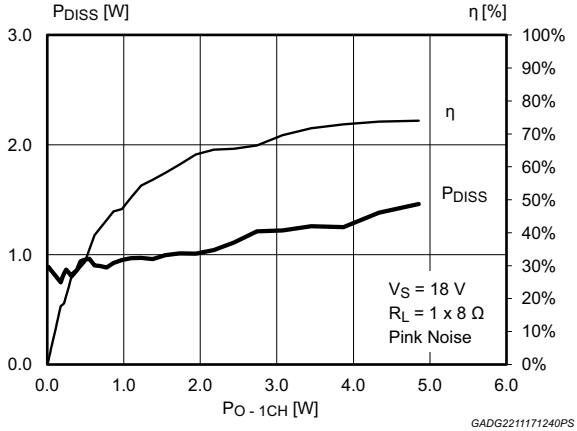


Figure 16. Efficiency and power dissipation (V_S = 3.3 V, R_L = 1 x 4 Ω, f = 1 kHz sine wave)

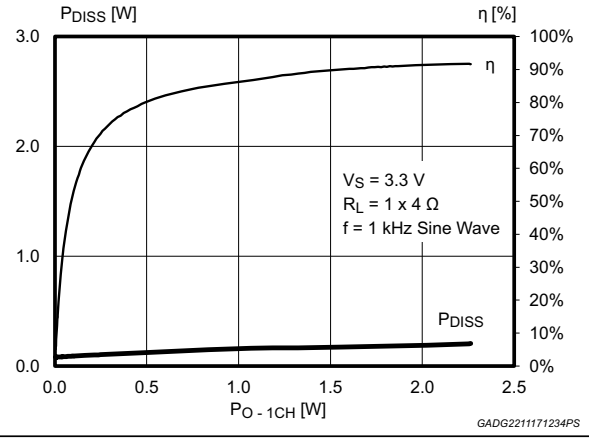


Figure 17. Efficiency and power dissipation (V_S = 3.3 V, R_L = 1 x 4 Ω, f = 1 kHz pink noise)

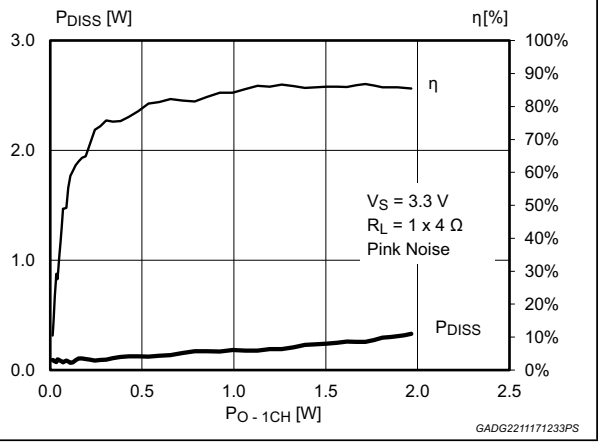


Figure 18. Efficiency and power dissipation (V_S = 3.3 V, R_L = 1 x 2 Ω, f = 1 kHz sine wave)

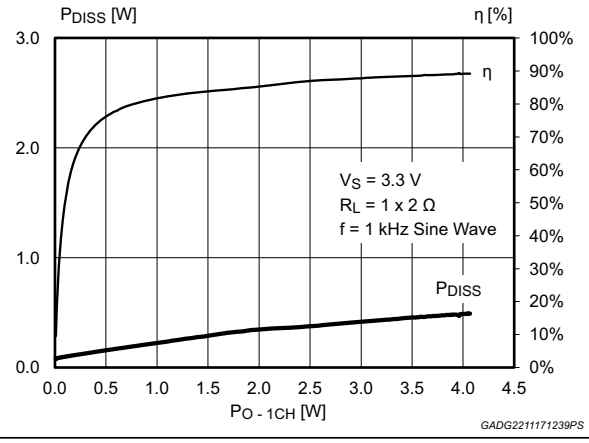


Figure 19. Efficiency and power dissipation (V_S = 3.3 V, R_L = 1 x 2 Ω, f = 1 kHz pink noise)

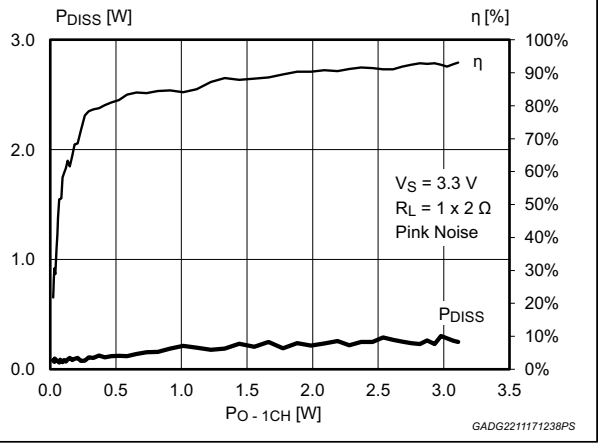


Figure 20. Efficiency and power dissipation (V_S = 3.3 V, R_L = 1 x 8 Ω, f = 1 kHz sine wave)

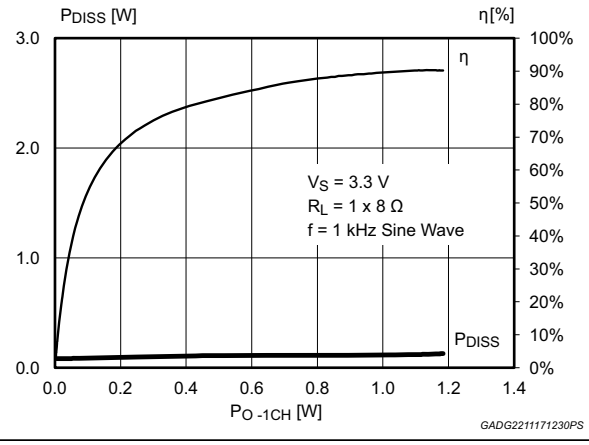


Figure 21. Efficiency and power dissipation (V_S = 3.3 V, R_L = 1 x 8 Ω, f = 1 kHz pink noise)

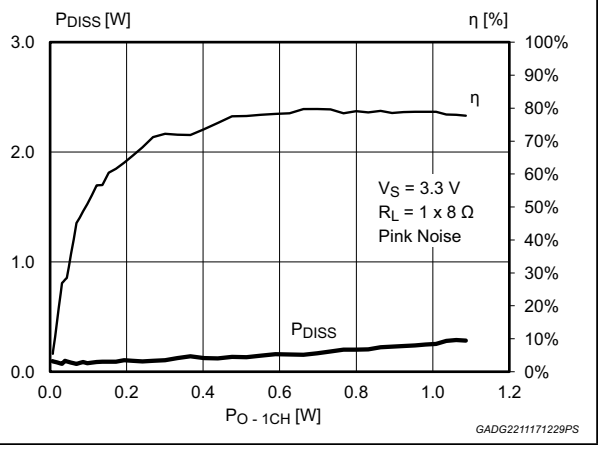


Figure 22. Output power vs. supply voltage (R_L = 4 Ω, sine wave)

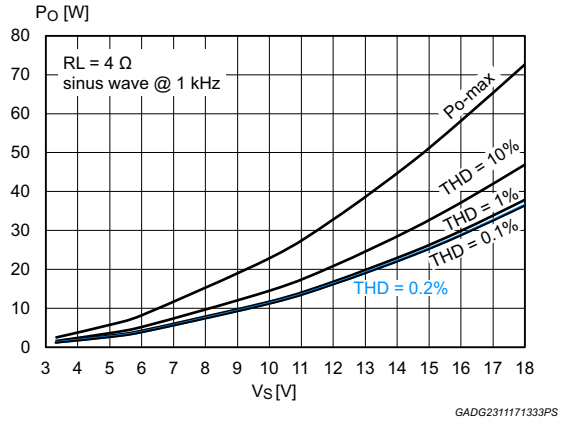


Figure 23. Output power vs. supply voltage (R_L = 2 Ω, sine wave)

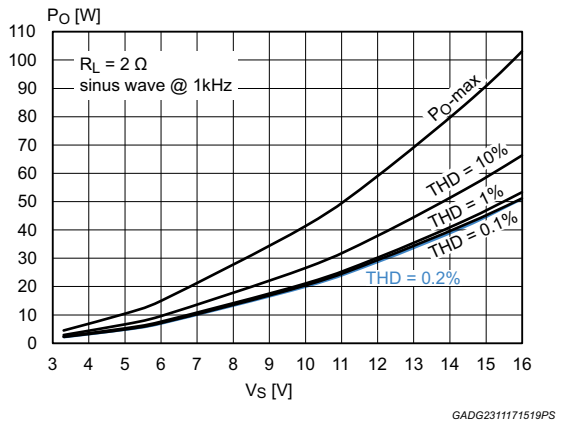


Figure 24. Output power vs. supply voltage (R_L = 8 Ω, sine wave)

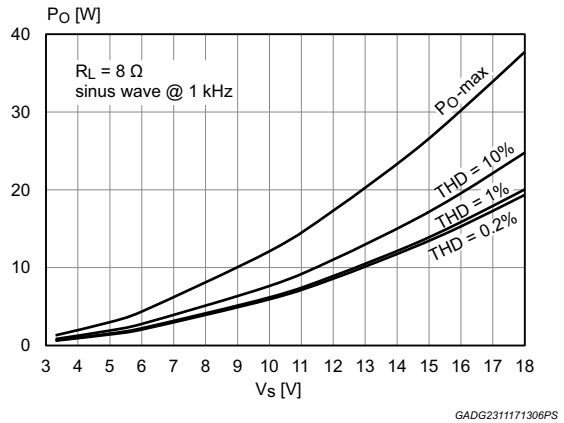


Figure 25. THD vs. output power (V_S = 14.4 V, R_L = 4 Ω)

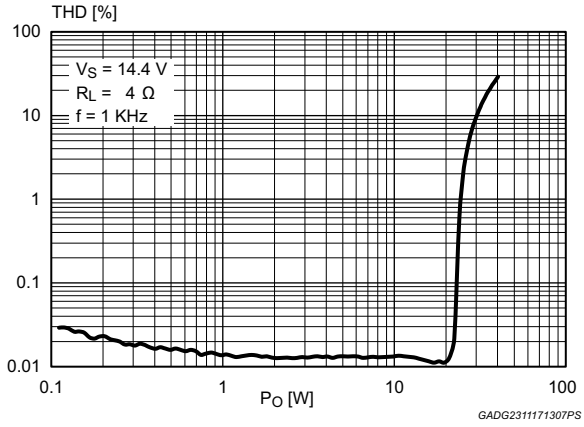


Figure 26. THD vs. output power (V_S = 14.4 V, R_L = 2 Ω)

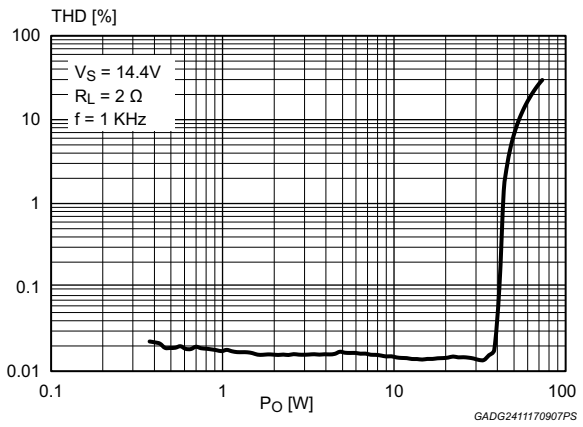


Figure 27. THD vs. output power (V_S = 14.4 V, R_L = 8 Ω)

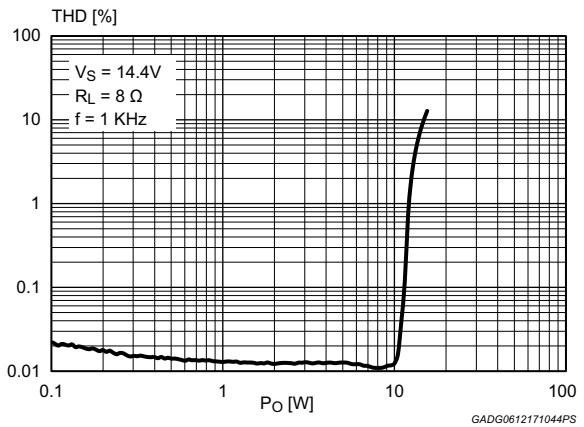


Figure 28. THD vs. frequency (V_S = 14.4 V, R_L = 4 Ω, P_O = 1 W)

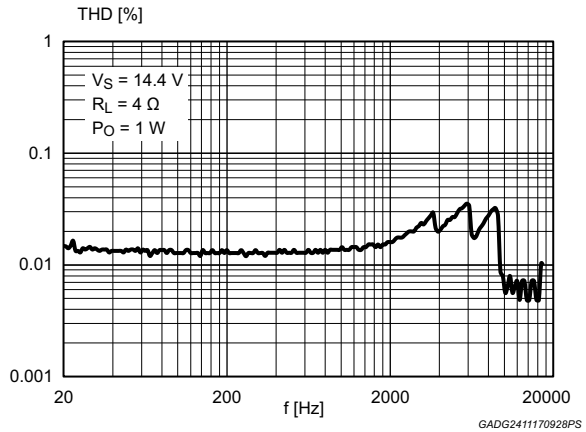


Figure 29. THD vs. frequency (V_S = 14.4 V, R_L = 2 Ω, P_O = 1 W)

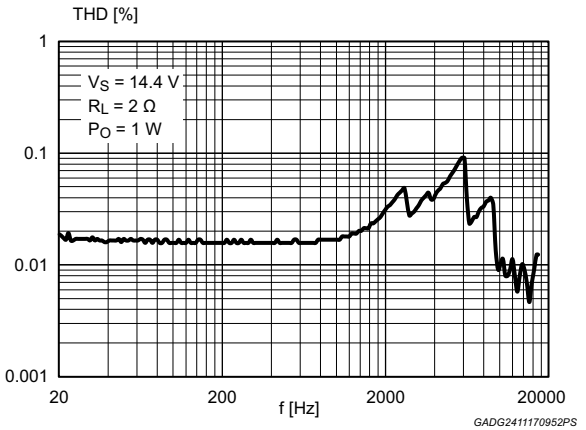


Figure 30. THD vs. frequency (V_S = 14.4 V, R_L = 8 Ω, P_O = 1 W)

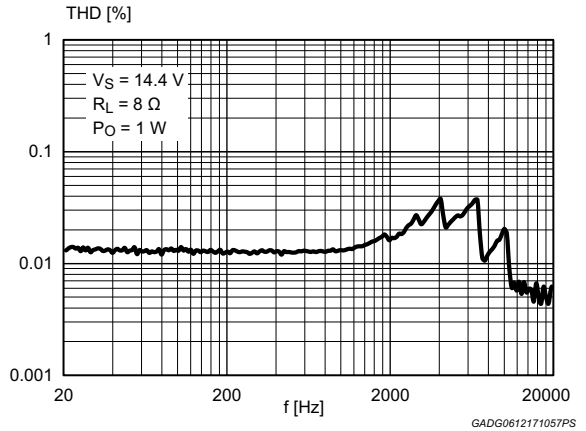


Figure 31. Frequency response (1 W, R_L = 4 Ω, f = 1 kHz)

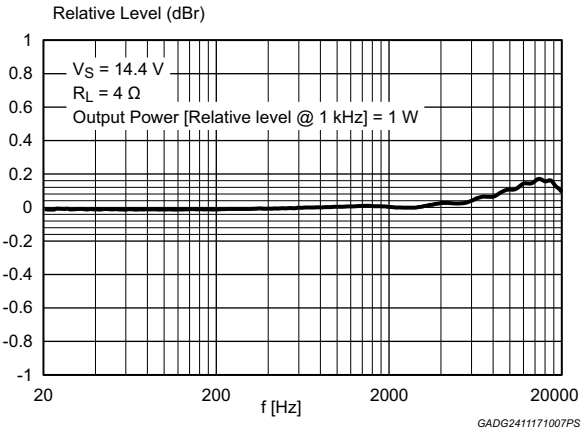


Figure 32. Frequency response (1 W, R_L = 2 Ω, f = 1 kHz)

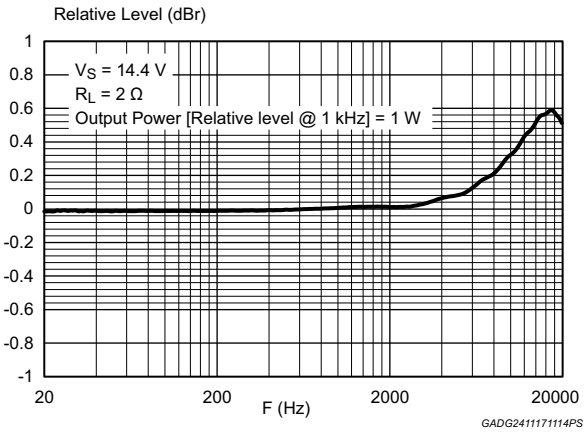


Figure 33. Frequency response (1 W, R_L = 8 Ω, f = 1 kHz)

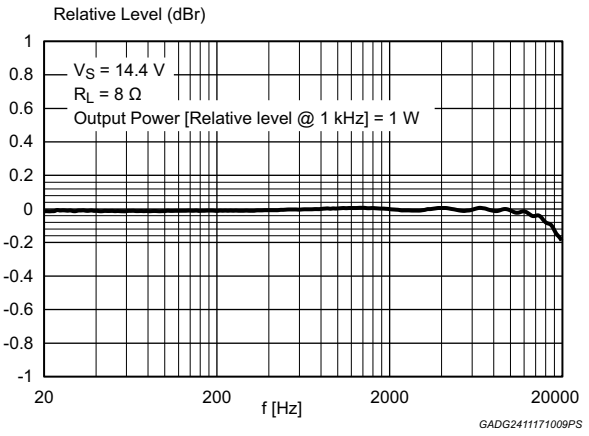


Figure 34. PSRR vs. frequency

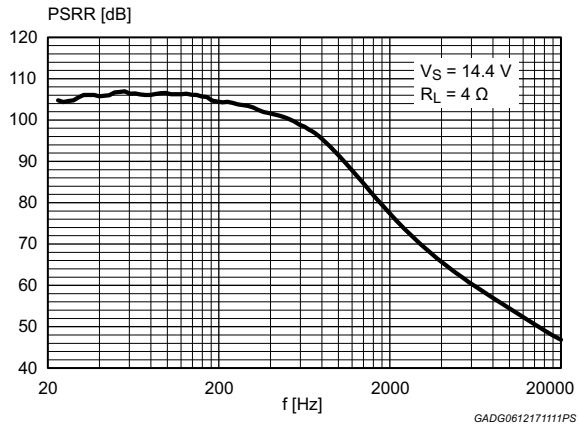


Figure 35. Quiescent current vs. supply voltage

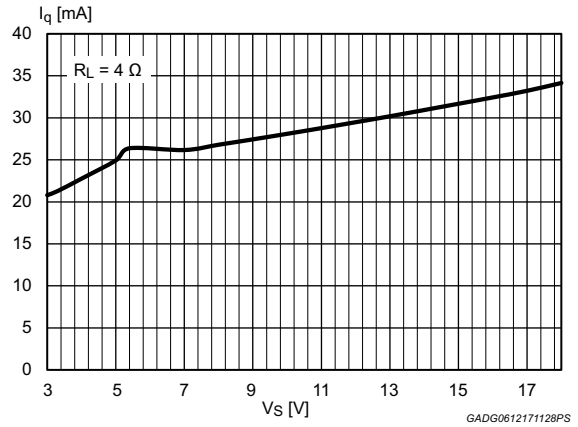


Figure 36. Dynamic range

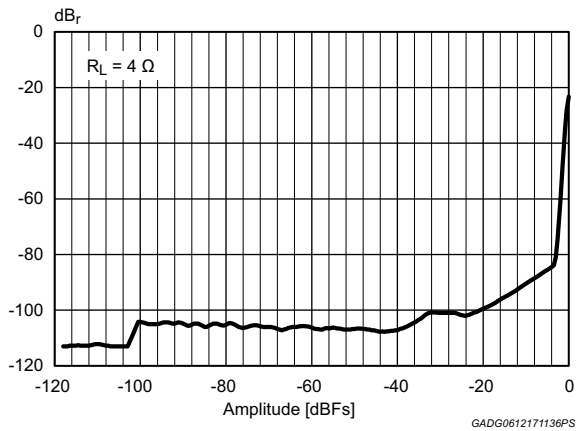
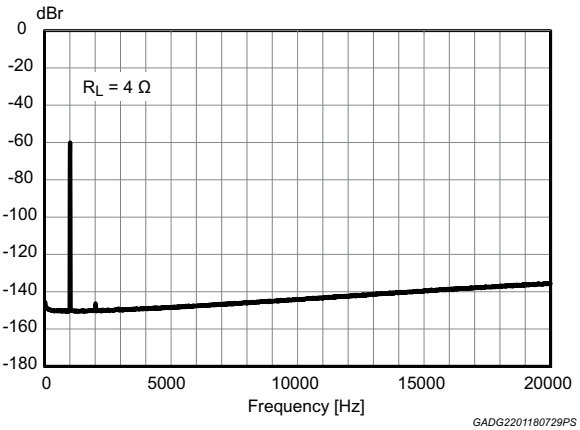


Figure 37. FFT - Output spectrum (-60 dBFS input signal)



6 General information

6.1 LC filter design

The audio performance of a Class D amplifier are heavily influenced by the characteristics of the output LC filter. The choice of its components is quite critical because a lot of constraints have to be fulfilled at the same time: size, cost, filter for EMI suppression, efficiency. In particular, both the inductor and the capacitor exhibit a non linear behavior: the value of the inductance is a function of the instantaneous current in it and similarly the value of the capacitor is a function of the voltage across it.

In the classical approach, where the feedback loop is closed right at the output of the power stage, the LC filter is placed outside the loop and these nonlinearities cause the Total Harmonic Distortion (THD) to increase. The only way to avoid this phenomenon would be to use components which are highly linear, but this means they are also bigger and/or more expensive.

Furthermore, when the LC filter is outside the loop, its frequency response heavily depends on the impedance of the loudspeaker; this is one of the most critical aspects of Class-D amplifiers. In standard class D this can be mitigated, but not solved, by means of additional damping networks, increasing cost, space and power dissipation. FDA803D, instead, provides a very flat frequency response over audio-band which can not be achieved by standard class D without feedback after LC filter.

Since the demodulator group is now in the feedback path, some constraints regarding the inductor and capacitor choice are still present but of course less stringent than in the case of a typical switching application.

Moreover FDA803D can be used with the 'classical' configuration of feedback on output (before LC filter), through I^2C configuration, allowing the maximum flexibility. The choice depends mainly on EMI target /requirements and could slightly affect other performances (like damping factor, or THD).

6.2 Load possibilities

FDA803D supports several load possibilities, driving 2 Ω, 4 Ω and higher ohmic loads.

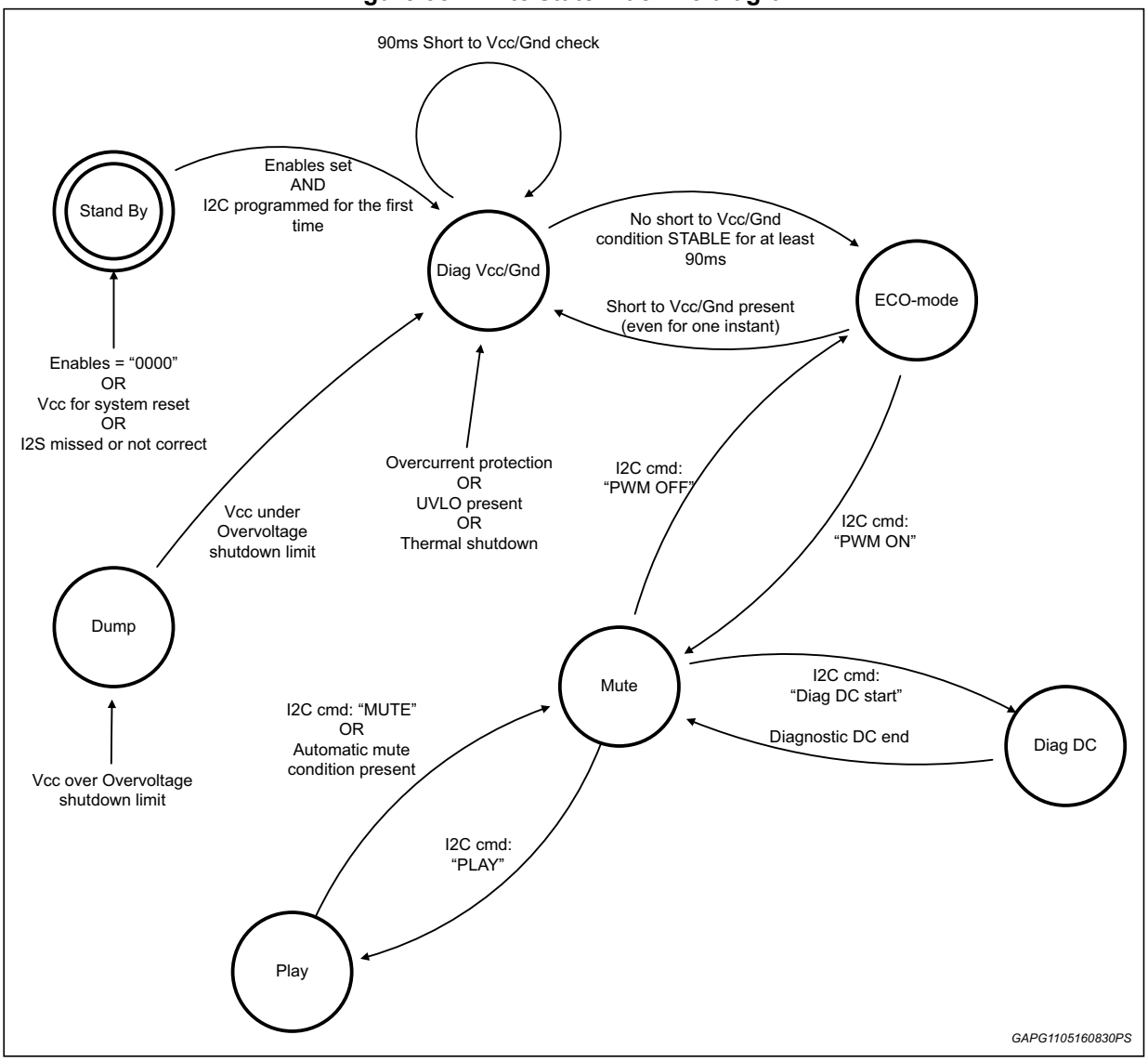
Possible channel configurations are:

- 1 x 4 ohm (or higher) (up to 18 V)
- 1 x 2 ohm (up to 16 V)

7 Finite state machine

FDA803D has a finite state machine which manages amplifier functionality, reacting to user and system inputs

Figure 38. Finite state machine diagram



7.1 Device state and address selection

Through Enable pins configuration it is possible to select different I^2C addresses (up to 8) or to configure the device in 4 different legacy ('no I^2C' modes) according to table 6.

Table 6. Operation mode

	Enable 1	Enable 2	Enable 3	Enable 4
Stand By	0	0	0	0
Amplifier ON address 1 = ‘1110000’	0	1	0	0
Amplifier ON address 2 = ‘1110001’	1	1	0	0
Amplifier ON address 3 = ‘1110010’	0	0	1	0
Amplifier ON address 4 = ‘1110011’	0	1	1	0
Amplifier ON address 5 = ‘1110100’	0	1	0	1
Amplifier ON address 6 = ‘1110101’	1	1	0	1
Amplifier ON address 7 = ‘1110110’	0	0	1	1
Amplifier ON address 8 = ‘1110111’	0	1	1	1
Legacy mode: low voltage mode; in-phase	1	1	1	0
Legacy mode: low voltage mode; out-phase	1	1	1	1
Legacy mode: standard voltage mode; in-phase	1	0	0	0
Legacy mode: standard voltage mode; out-phase	1	0	0	1

In this way, up to 8 devices can be easily used in the same application with a single I^2C bus.

Moreover it is possible to work without I^2C configuring the voltage range and switching mode to be used.

When a valid combination of Enable 1/2/3/4 is recognized the device turns on all the internal supply voltages and outputs are biased to Vcc/2.

The internal I^2C registers are pre-settled in "default condition", waiting for the I^2C next instruction.

The return in the Standby condition, (all enable pins at 0), will cause the reset of the amplifier. As defined in the finite state machine, The same event will happen if PLL is not locked, I^2S is missing or not correct, Vcc for system reset.

FDA803D can work only in I^2C slave mode.