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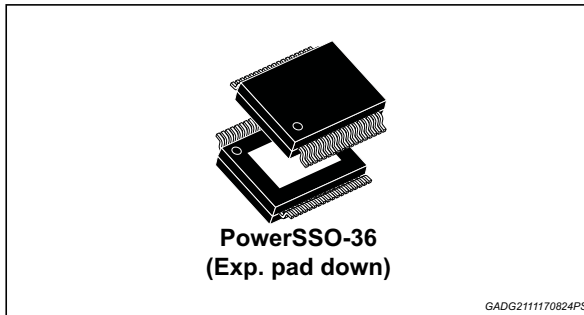
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## 1 x 45 W class D digital input automotive power amplifier with diagnostics, wide voltage operation range for car audio and telematic

Datasheet - production data



### Features



- AEC-Q100 qualified
- Integrated 108 dB D/A conversion
- I<sup>2</sup>S and TDM digital input (4/8/16CH TDM)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Full I<sup>2</sup>C bus driving (3.3/1.8 V)
- CISPR 25 - Class V (Fourth edition)
- Very low quiescent current
- Output lowpass filter included in the feedback allowing outstanding audio performances
- Wide operating supply range from 3.3 to 18 V, suitable for car radio, telematics and e-call
- MOSFET power outputs allowing high output power capability
  - 1 x 25 W /4 Ω @ 14.4 V, 1 kHz THD = 1%
  - 1 x 30 W /4 Ω @ 14.4 V, 1 kHz THD = 10%

- 2 Ω loads driving
- Power limiting function (configurable through I<sup>2</sup>C)
- I<sup>2</sup>C bus diagnostics:
  - Short to V<sub>CC</sub>/GND
  - Short load and open load detection (also in play mode)
  - Four thermal warnings
- DC offset detector (also in play) and 'hot spot' detection
- Clipping detector
- Integrated thermal protection
- Legacy mode ('no I<sup>2</sup>C' mode), 4 configurable settings
- Short circuit and ESD integrated protections
- Package: PowerSSO-36 exposed pad down

**Table 1. Device summary**

| Order code  | Package            | Packing     |
|-------------|--------------------|-------------|
| FDA803D-EHT | PowerSSO-36        | Tape & reel |
| FDA803D-EHX | (exposed pad down) | Tube        |

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# 1 Description

The FDA803D is a single bridge class D amplifier, designed in the most advanced BCD technology, intended for any automotive audio application (car radio, telematics and e-call, noise and tone generators, etc).

The FDA803D integrates a high performance D/A converter together with powerful MOSFET outputs in class D, so it is very compact and powerful, moreover reaches outstanding efficiency performances (90%).

It has a very wide operating range: it can be operated both with standard car battery levels (5.5-18 V operating, compatible to load dump pulse) and with external step-down generated voltages or emergency battery (since it is compatible to minimum 3.3 V operative).

The feedback loop is including the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion.

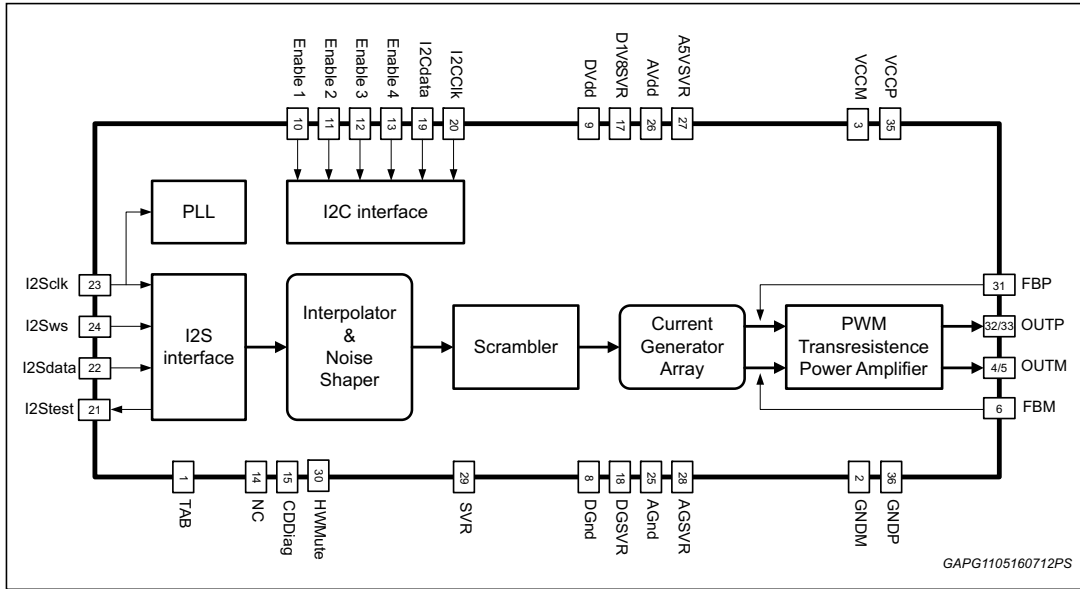
FDA803D is configurable through I<sup>2</sup>C bus interface and is integrating a complete diagnostics array specially intended for automotive applications including innovative open load and DC offset detection in play mode.

Thanks to the solutions implemented to solve the EMI problems, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover FDA803D features a configurable power limiting function, and can be optionally operated under no I<sup>2</sup>C mode ('legacy mode').

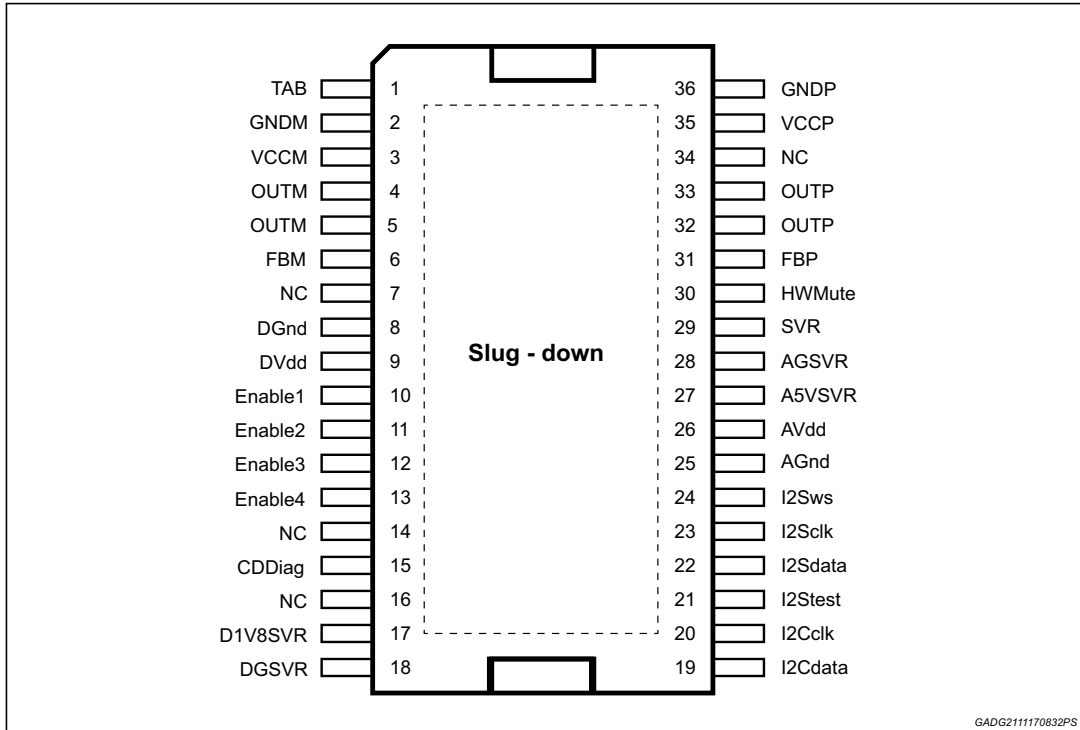
## 2 Block diagram

Figure 1. Block diagram



### 3 Pins description

Figure 2. Pins connection diagram



GADG211170832PS

Table 2. Pins list function

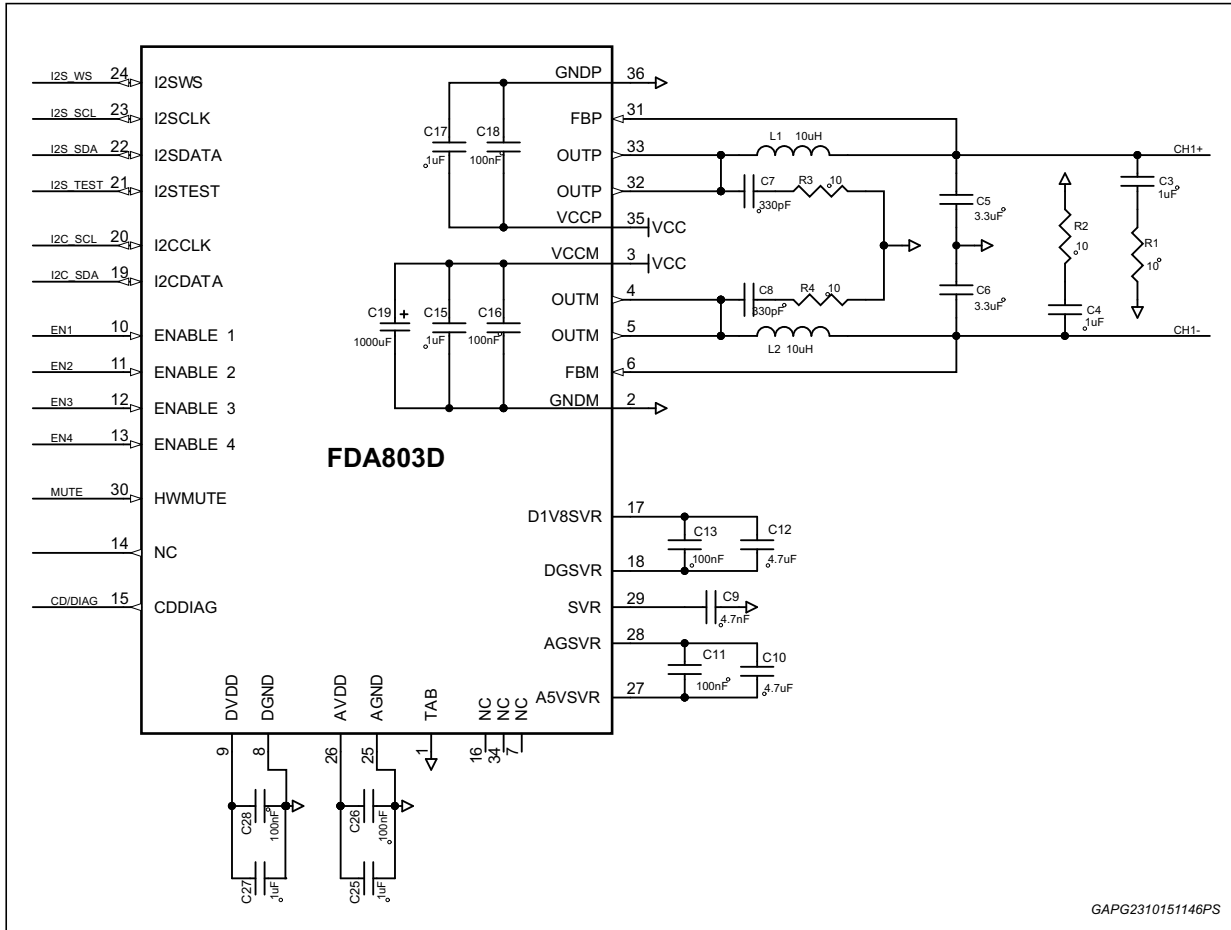
| Pin # | Pin name | Function                                    |
|-------|----------|---|
| 1     | TAB      | Device slug connection                      |
| 2     | GNDM     | Channel half bridge minus, Power Ground     |
| 3     | VCCM     | Channel half bridge minus, Power Supply     |
| 4     | OUTM     | Channel half bridge minus, Output           |
| 5     | OUTM     | Channel half bridge minus, Output           |
| 6     | FBM      | Channel half bridge minus, Feedback         |
| 7     | NC       | Not connected                               |
| 8     | DGnd     | Digital ground                              |
| 9     | DVdd     | Digital supply                              |
| 10    | Enable1  | Enable 1                                    |
| 11    | Enable2  | Enable 2                                    |
| 12    | Enable3  | Enable 3                                    |
| 13    | Enable4  | Enable 4                                    |
| 14    | NC       | Not connected                               |
| 15    | CDDiag   | Clipping detector and diagnostic output pin |

Table 2. Pins list function

| Pin # | Pin name | Function   |
|-------|----------|--|
| 16    | NC       | Not connected  |
| 17    | D1V8SVR  | Positive digital supply V(SVR)+0.9V (Internally generated) |
| 18    | DGSVR    | Negative digital supply V(SVR)-0.9V (Internally generated) |
| 19    | I2Cdata  | I2C Data   |
| 20    | I2Cclk   | I2C Clock  |
| 21    | I2Stest  | test pin, left open  |
| 22    | I2Sdata  | I2S/TDM data   |
| 23    | I2Sclk   | I2S/TDM Clock input  |
| 24    | I2Sws    | I2S/TDM Sync input /Word Select input                      |
| 25    | AGnd     | Analog ground  |
| 26    | AVdd     | Analog supply  |
| 27    | A5VSVR   | Positive Analog Supply V(SVR)+2.5V (Internally generated)  |
| 28    | AGSVR    | Negative Analog Supply V(SVR)-2.5V (Internally generated)  |
| 29    | SVR      | Supply Voltage Ripple Rejection Capacitor                  |
| 30    | HWMute   | Hardware mute pin  |
| 31    | FBP      | Channel half bridge plus, Feedback                         |
| 32    | OUTP     | Channel half bridge plus, Output                           |
| 33    | OUTP     | Channel half bridge plus, Output                           |
| 34    | NC       | Not connected  |
| 35    | VCCP     | Channel half bridge plus, Power Supply                     |
| 36    | GNDP     | Channel half bridge plus, Power Ground                     |

# 4 Application diagram

Figure 3. Application diagram



GAPG2310151146PS

## 5 Electrical specifications

### 5.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol   | Parameter   | Value              | Unit |
|--|---|--------------------|------|
| $V_{CC}$ [ $V_{CCP}$ , $V_{CCM}$ , $A_{VDD}$ , $D_{VDD}$ ] | DC supply voltage                                       | -0.3 to 28         | V    |
|  | Transient supply voltage for $t = 100 \text{ ms}^{(1)}$ | -0.3 to 40         | V    |
| $GND_{max}$ [ $D_{GND}$ , $A_{GND}$ , $GNDP$ , $GNDM$ ]    | Ground pin voltage difference                           | -0.3 to 0.3        | V    |
| $I^2C_{data}$ , $I^2C_{clk}$                               | I <sup>2</sup> C bus pins voltage                       | -0.3 to 5.5        | V    |
| $I^2S_{test}$ , $I^2S_{data}$ , $I^2S_{clk}$ , $I^2S_{ws}$ | I <sup>2</sup> S bus pins voltage                       | -0.3 to 5.5        | V    |
| Enable <sub>1,2,3,4</sub>                                  | Enables   | -0.3 to 5.5        | V    |
| HWMute   | Hardware mute   | -0.3 to 7          | V    |
| CDDiag   | Clip detection  | -0.3 to 5.5        | V    |
| $I_o$  | Output current (repetitive $f > 10 \text{ Hz}$ )        | Internally limited | A    |
| $T_{amb}$  | Ambient operating temperature                           | -40 to 125         | °C   |
| $T_{stg}$ , $T_j$  | Storage and junction temperature                        | -55 to 150         | °C   |
| ESDHBM   | ESD protection HBM                                      | 2000               | V    |
| ESDCDM   | ESD protection CDM                                      | 500                | V    |

1.  $V_{CC} = 35 \text{ V}$  for  $t < 400 \text{ ms}$  as per ISO16750-2 load dump with centralized load dump suppression.

### 5.2 Thermal data

Table 4. Thermal data - PowerSS036 slug-down package

| Symbol                     | Parameter   | Value | Unit |
|----------------------------|---|-------|------|
| $R_{th \text{ j-a-2s}}$    | Thermal resistance junction-to-ambient (2s board)   | 56    | °C/W |
| $R_{th \text{ j-a-2s2p}}$  | Thermal resistance junction-to-ambient (2s2p board) | 31    | °C/W |
| $R_{th \text{ j-a-2s2pv}}$ | Thermal resistance junction-to-ambient (2s2p+vias)  | 26    | °C/W |

### 5.3 Electrical characteristics

$V_{CC} = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ;  $f = 1\text{ kHz}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; I<sup>2</sup>C defaults, unless otherwise specified. LC filter:  $L = 10\ \mu\text{H}$ ,  $C = 3.3\ \mu\text{F}$ . PWM in In-phase modulation, feedback connected after the filter.

**Table 5. Electrical characteristics**

| Symbol       | Parameter   | Test condition                                    | Min  | Typ    | Max  | Unit             |
|--------------|---|---|------|--------|------|------------------|
| $V_{CC}$     | Supply voltage range                                | $R_L = 4\ \Omega$                                 | 3.3  | -      | 18   | V                |
|              |   | $R_L = 2\ \Omega$ <sup>(1)</sup>                  | 3.3  | -      | 16   |                  |
| $I_{VCC}$    | Quiescent current                                   | Device in Standby                                 | -    | 1      | 5    | $\mu\text{A}$    |
|              |   | Device on (MUTE state)                            | -    | 35     | -    | mA               |
|              |   | ECO MODE  | -    | 22     | -    | mA               |
| $V_{OS}$     | Offset voltage                                      | Mute & Play                                       | -10  | -      | +10  | mV               |
| $D_{VDD}$    | Digital supply voltage range                        | -   | 3.3  | -      | 18   | V                |
| $A_{VDD}$    | Analog supply voltage range                         | -   | 3.3  | -      | 18   | V                |
| $I_{OP}$     | Overcurrent protection                              | IB11 D5-4 = 00                                    | 9.5  | 11     | 12.5 | A                |
|              |   | IB11 D5-4 = 01                                    | 6.7  | 8      | 9.3  | A                |
|              |   | IB11 D5-4 = 10                                    | 5    | 6      | 7    | A                |
|              |   | IB11 D5-4 = 11                                    | 3    | 4      | 5    | A                |
| $I_{AVDD}$   | Analog current                                      | Device on (MUTE state)                            | -    | 9      | 20   | mA               |
| $I_{DVDD}$   | Digital current                                     | Device on (MUTE state)                            | -    | 13     | 20   | mA               |
| -            | Overvoltage shutdown                                | Attenuation = 0.5 dB <sup>(2)</sup>               | 18.5 | 19.5   | 20.5 | V                |
| $V_{lowM}$   | $V_{CC}$ low supply mute threshold                  | Attenuation <0.5 dB<br>Low voltage mode (IB0D0=1) | 2.7  | 2.9    | 3.3  | V                |
|              |   | Attenuation <0.5 dB<br>Standard mode (IB0D0=0)    | 4.5  | 4.7    | 5    | V                |
| $V_{highM}$  | $V_{CC}$ high voltage mute <sup>(2)</sup>           | -   | 18   | 18.9   | 20.3 | V                |
| $UVLO_{VCC}$ | $V_{CC}$ supply UVLO threshold                      | Standard mode (IB0D0=0)                           | 4.4  | 4.6    | 4.8  | V                |
|              |   | Low voltage mode (IB0D0=1)                        | 2.55 | 2.7    | 2.85 | V                |
| $T_{sh}$     | Thermal shutdown                                    | -   | 165  | 175    | 185  | $^\circ\text{C}$ |
| $T_{pl}$     | Thermal protection junction temperature             | Attenuation = 0.5 dB                              | 150  | 160    | 170  | $^\circ\text{C}$ |
| $T_{w1}$     | Thermal warning junction temperature <sup>(3)</sup> | -   | -    | Tpl-5  | -    | $^\circ\text{C}$ |
| $T_{w2}$     |   | -   | -    | Tpl-15 | -    | $^\circ\text{C}$ |
| $T_{w3}$     |   | -   | -    | Tpl-35 | -    | $^\circ\text{C}$ |
| $T_{w4}$     |   | -   | -    | Tpl-50 | -    | $^\circ\text{C}$ |

Table 5. Electrical characteristics (continued)

| Symbol                              | Parameter   | Test condition   | Min  | Typ   | Max  | Unit |
|-------------------------------------|---|--|------|-------|------|------|
| <b>Audio performances</b>           |   |  |      |       |      |      |
| P <sub>O</sub>                      | Output power  | THD = 10 %   | -    | 30    | -    | W    |
|                                     |   | THD = 1 %  | -    | 25    | -    | W    |
|                                     |   | Max power; V <sub>CC</sub> = 15.2 V  | -    | 50    | -    | W    |
|                                     |   | R <sub>L</sub> = 2 Ω THD = 10% <sup>(1)</sup>                                | -    | 55    | -    | W    |
|                                     |   | R <sub>L</sub> = 2 Ω THD = 1% <sup>(1)</sup>                                 | -    | 45    | -    | W    |
|                                     |   | R <sub>L</sub> = 2 Ω, max power <sup>(1)</sup>                               | -    | 80    | -    | W    |
| P <sub>O</sub>                      | Output power  | THD = 10% V <sub>CC</sub> = 5 V  | -    | 3.8   | -    | W    |
|                                     |   | THD = 10% V <sub>CC</sub> = 3.3 V  | -    | 1.6   | -    | W    |
| PSRR                                | Power supply rejection ratio  | f = 1 kHz; Vr = 1Vpk;  | 70   | 80    | -    | -    |
| THD                                 | Total harmonic distortion   | P <sub>O</sub> = 1 W, f = 1 kHz  | -    | 0.01  | 0.05 | %    |
| Gain                                | Standard gain   | at Amplitude = -10 dBFs  | 5.5  | 5.9   | 6.3  | Vp   |
|                                     | Low gain <sup>(4)</sup>   |  | 3.3  | 3.6   | 3.9  | Vp   |
| DR                                  | Dynamic range   | A-wtd and brickwall 20 kHz filter  | 102  | 107.5 | -    | dB   |
| SNR                                 | Signal to noise ratio   | A-wtd and brickwall 20 kHz filter  | 107  | 112   | -    | dB   |
| Eout1                               | Output noise  | A-wtd and brickwall 20 kHz filter used, no output signal;                    | -    | 35    | 55   | μV   |
| Eout2                               | Output noise  | CCIR 468 filtered  | -    | 84    | 130  | μV   |
| ΔV <sub>OITU</sub>                  | ITU Pop filter output voltage   | Standby to Mute and Mute to Standby transition                               | -7.5 | -     | +7.5 | mV   |
| <b>Mute</b>                         |   |  |      |       |      |      |
| V <sub>Mth</sub> <sup>(5)</sup>     | Mute pin voltage threshold  | Attenuation <0.5 dB, and digital mute disabled                               | 2.3  | -     | -    | V    |
|                                     |   | Attenuation ≥60 dB, and digital mute disabled                                | -    | -     | 1    |      |
| I <sub>M</sub>                      | Mute pin source current   | -  | 9    | 11    | 13   | μA   |
| V <sub>Mcl</sub>                    | Mute pin internal clamp voltage   | -  | 5.5  | 6     | 6.5  | V    |
| I <sub>feed</sub>                   | Peak current flowing in the feedback pins                                 | Standby condition, all feedbacks forced to V <sub>CC</sub> , output floating | -    | 110   | 130  | μA   |
| <b>I<sup>2</sup>C bus interface</b> |   |  |      |       |      |      |
| f <sub>SCL</sub>                    | Clock frequency   | -  | -    | -     | 400  | kHz  |
| V <sub>IL</sub>                     | I2C pins low voltage  | -  | -    | -     | 0.8  | V    |
| V <sub>IH</sub>                     | I2C pins high voltage   | -  | 1.3  | -     | -    | V    |
| V <sub>OLMAX</sub>                  | Maximum I2C data pin low voltage when current I <sub>sink</sub> is sinked | I <sub>sink</sub> = 4 mA   | -    | 0.12  | 0.5  | V    |
| I <sub>LIMAX</sub>                  | Maximum input leakage current   | V = 3.6 V  | -    | -     | 1    | μA   |

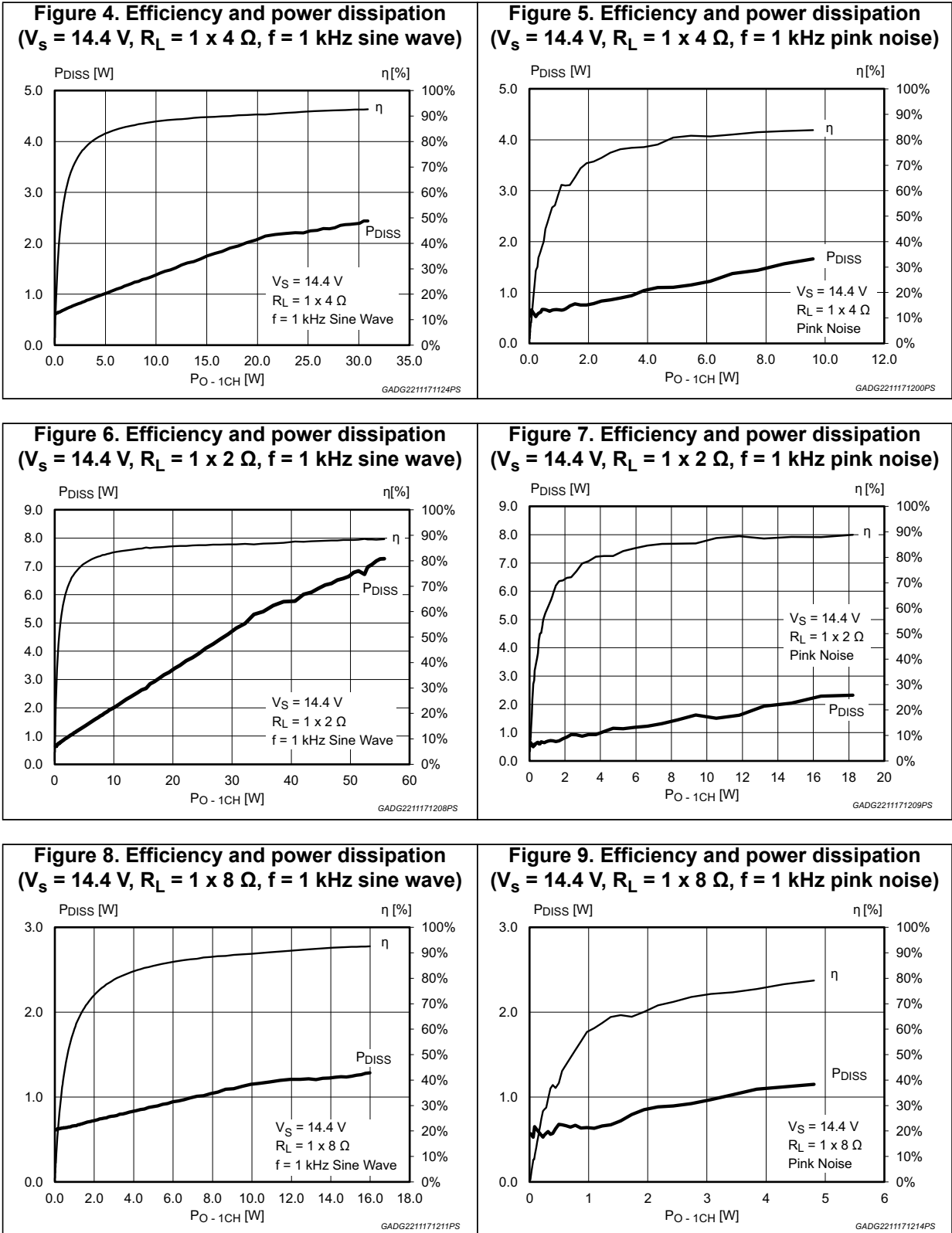


**Table 5. Electrical characteristics (continued)**

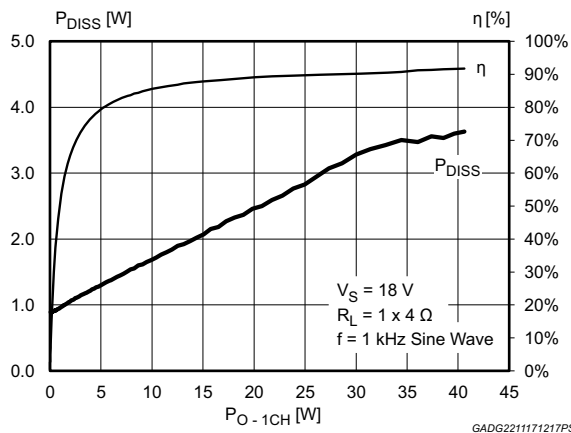
| Symbol                              | Parameter   | Test condition  | Min  | Typ | Max  | Unit |
|-------------------------------------|---|---|------|-----|------|------|
| <b>I<sup>2</sup>S bus interface</b> |   |   |      |     |      |      |
| V <sub>IL-I2S</sub>                 | I2S pins low voltage                                | -   | -    | -   | 0.8  | V    |
| I <sub>L</sub>                      | Input logic current, low                            | V <sub>I</sub> = 0 V                                      | -    | -   | 500  | nA   |
| V <sub>IH-I2S</sub>                 | I2S pins high voltage                               | -   | 1.3  | -   | -    | V    |
| I <sub>H</sub>                      | Input logic current, high                           | V <sub>I</sub> = TBD                                      | -    | -   | 500  | nA   |
| <b>Control pins characteristics</b> |   |   |      |     |      |      |
| V <sub>ENL</sub>                    | Enable pins low voltage                             | -   | -    | -   | 0.9  | V    |
| V <sub>ENH</sub>                    | Enable pins high voltage                            | -   | 2.4  | -   | -    | V    |
| <b>Clipping and offset detector</b> |   |   |      |     |      |      |
| CD <sub>THD</sub>                   | Clip det THD <sup>(6)</sup>                         | THD @ 100 Hz with average<br>V <sub>clipdet</sub> = 2 V   | 5    | 7   | 9    | %    |
| CDSAT                               | Clip det sat. voltage                               | CD on; I <sub>CD</sub> = 1 mA                             | -    | 150 | 300  | mV   |
| CD <sub>LK</sub>                    | Clip det leakage current                            | CD pin at 3.6 V   | -    | -   | 15   | μA   |
| V <sub>offin</sub>                  | Input DC offset detection threshold                 | Theshold at which an offset present at inputs is detected | -    | -18 | -    | dB   |
| V <sub>offout</sub>                 | Output DC offset detection threshold <sup>(7)</sup> | Input high pass filter disable                            | ±1.4 | ±2  | ±2.6 | V    |

1. If outphase modulation selected, slow slope configuration must be used (IB11,D3)
2. Parameter values based on bench measurements (guaranteed by correlation with overvoltage shutdown).
3. The thermal warnings are always in tracking.
4. When selecting the low gain, also the thresholds for "DC diagnostic" function and "Open load in play detector" function scale of the same factor with respect to standard gain configuration.
5. See [Chapter 8: Muting function architecture](#) for more details.
6. Guaranteed by correlation.
7. Measured at bench during product validation.

### 5.4 Typical curves of the main electrical parameters

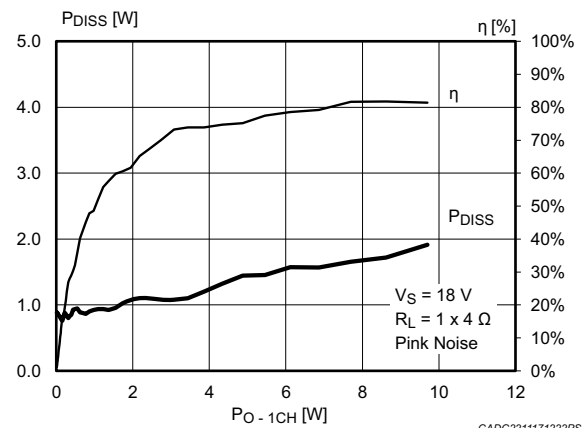


**Figure 10. Efficiency and power dissipation ( $V_S = 18\text{ V}$ ,  $R_L = 1 \times 4\ \Omega$ ,  $f = 1\text{ kHz}$  sine wave)**



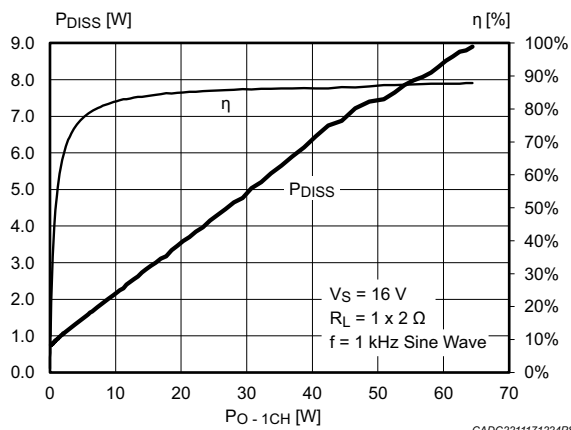
GADG2211171217PS

**Figure 11. Efficiency and power dissipation ( $V_S = 18\text{ V}$ ,  $R_L = 1 \times 4\ \Omega$ ,  $f = 1\text{ kHz}$  pink noise)**



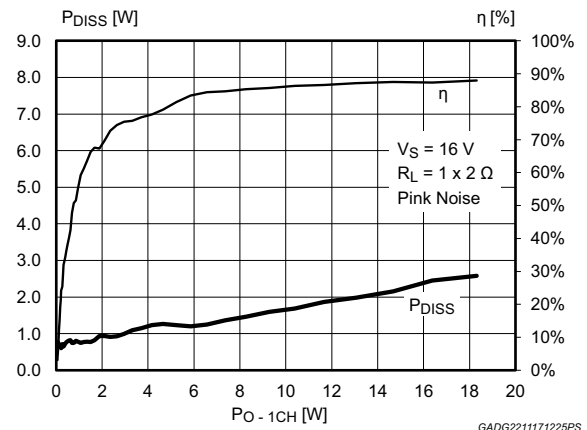
GADG2211171222PS

**Figure 12. Efficiency and power dissipation ( $V_S = 16\text{ V}$ ,  $R_L = 1 \times 2\ \Omega$ ,  $f = 1\text{ kHz}$  sine wave)**



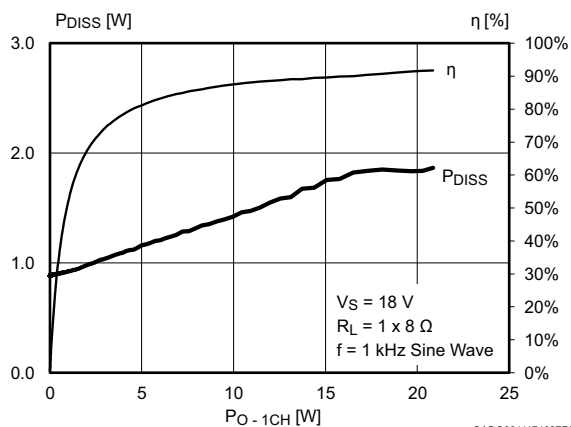
GADG2211171224PS

**Figure 13. Efficiency and power dissipation ( $V_S = 16\text{ V}$ ,  $R_L = 1 \times 2\ \Omega$ ,  $f = 1\text{ kHz}$  pink noise)**



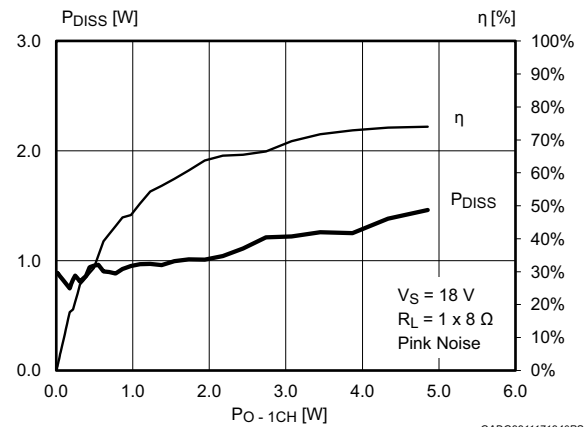
GADG2211171225PS

**Figure 14. Efficiency and power dissipation ( $V_S = 18\text{ V}$ ,  $R_L = 1 \times 8\ \Omega$ ,  $f = 1\text{ kHz}$  sine wave)**



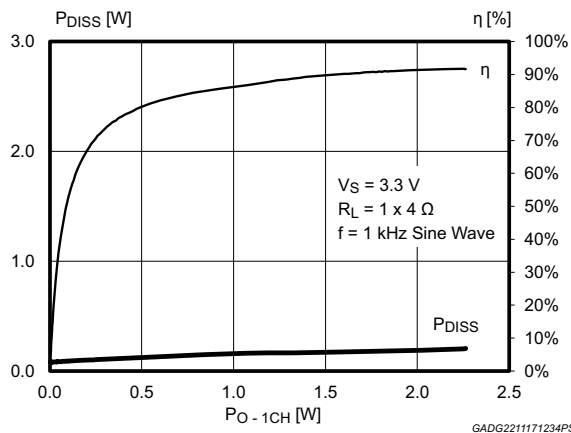
GADG2211171227PS

**Figure 15. Efficiency and power dissipation ( $V_S = 18\text{ V}$ ,  $R_L = 1 \times 8\ \Omega$ ,  $f = 1\text{ kHz}$  pink noise)**



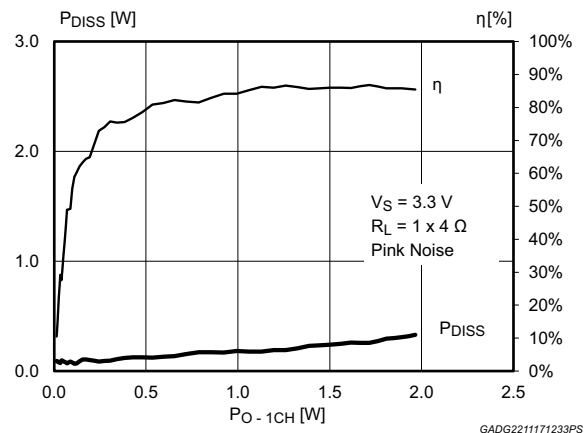
GADG2211171240PS

**Figure 16. Efficiency and power dissipation ( $V_S = 3.3\text{ V}$ ,  $R_L = 1 \times 4\ \Omega$ ,  $f = 1\text{ kHz}$  sine wave)**



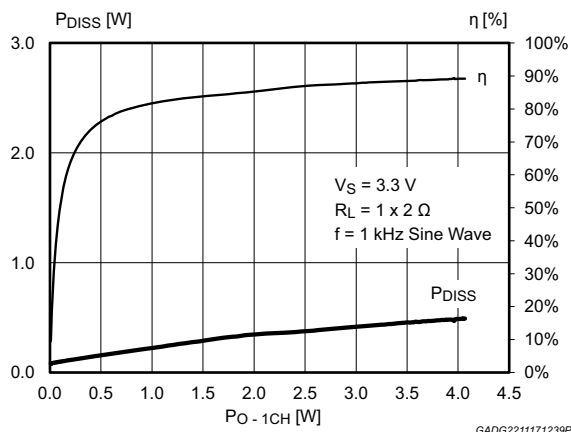
GADG2211171234PS

**Figure 17. Efficiency and power dissipation ( $V_S = 3.3\text{ V}$ ,  $R_L = 1 \times 4\ \Omega$ ,  $f = 1\text{ kHz}$  pink noise)**



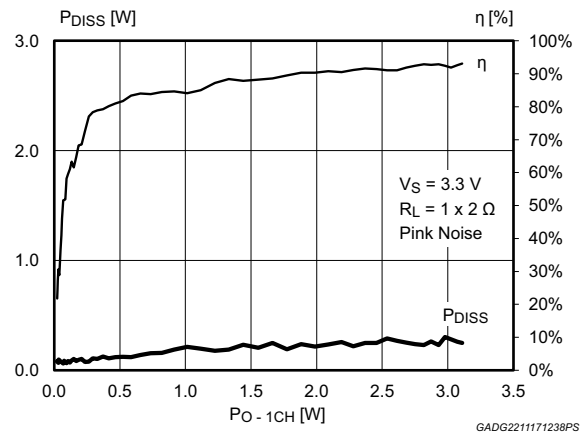
GADG2211171233PS

**Figure 18. Efficiency and power dissipation ( $V_S = 3.3\text{ V}$ ,  $R_L = 1 \times 2\ \Omega$ ,  $f = 1\text{ kHz}$  sine wave)**



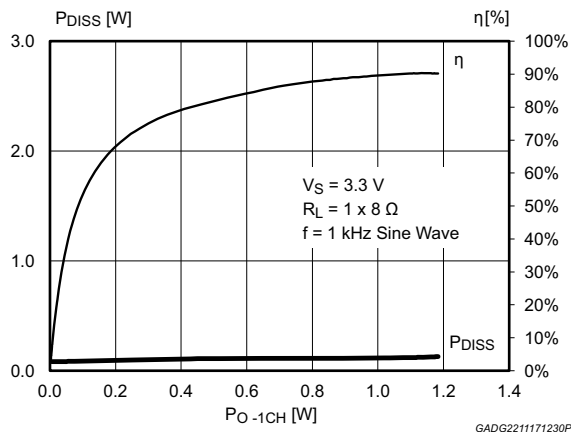
GADG2211171239PS

**Figure 19. Efficiency and power dissipation ( $V_S = 3.3\text{ V}$ ,  $R_L = 1 \times 2\ \Omega$ ,  $f = 1\text{ kHz}$  pink noise)**



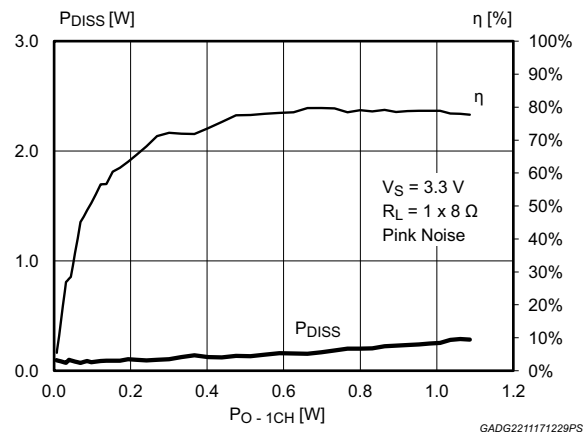
GADG2211171238PS

**Figure 20. Efficiency and power dissipation ( $V_S = 3.3\text{ V}$ ,  $R_L = 1 \times 8\ \Omega$ ,  $f = 1\text{ kHz}$  sine wave)**



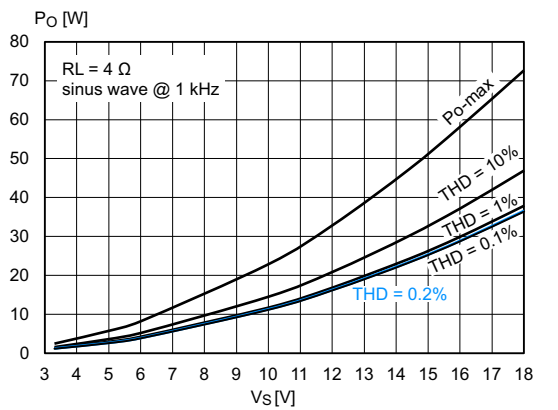
GADG2211171230PS

**Figure 21. Efficiency and power dissipation ( $V_S = 3.3\text{ V}$ ,  $R_L = 1 \times 8\ \Omega$ ,  $f = 1\text{ kHz}$  pink noise)**



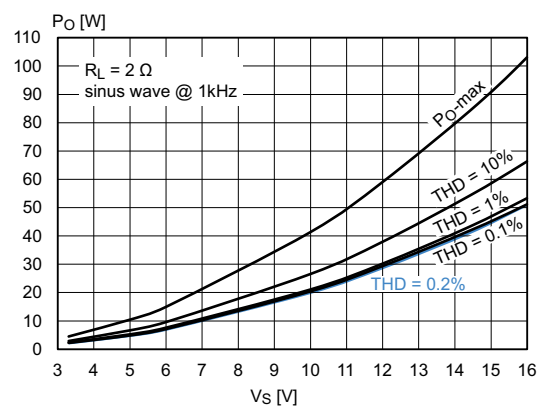
GADG2211171229PS

**Figure 22. Output power vs. supply voltage**  
( $R_L = 4 \Omega$ , sine wave)



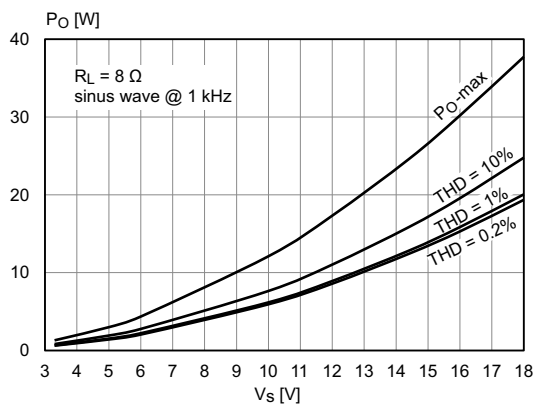
GADG2311171333PS

**Figure 23. Output power vs. supply voltage**  
( $R_L = 2 \Omega$ , sine wave)



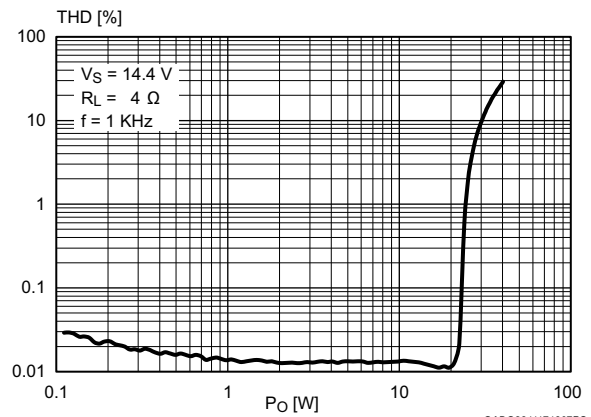
GADG2311171519PS

**Figure 24. Output power vs. supply voltage**  
( $R_L = 8 \Omega$ , sine wave)



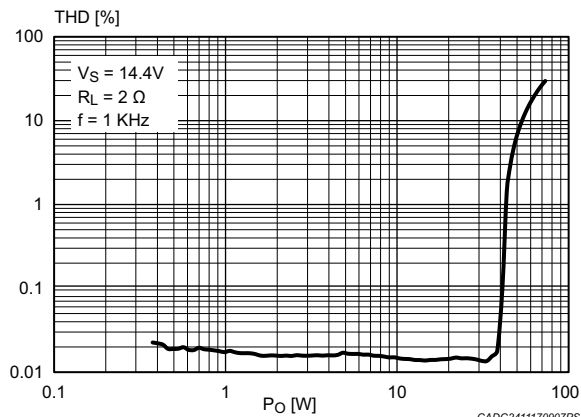
GADG2311171306PS

**Figure 25. THD vs. output power**  
( $V_S = 14.4 V$ ,  $R_L = 4 \Omega$ )



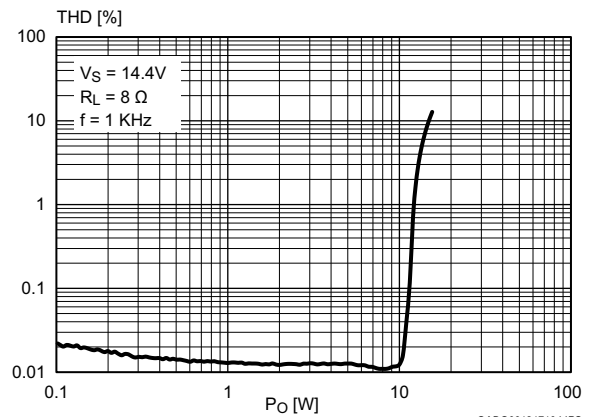
GADG2311171307PS

**Figure 26. THD vs. output power**  
( $V_S = 14.4 V$ ,  $R_L = 2 \Omega$ )



GADG2411170907PS

**Figure 27. THD vs. output power**  
( $V_S = 14.4 V$ ,  $R_L = 8 \Omega$ )



GADG0612171044PS

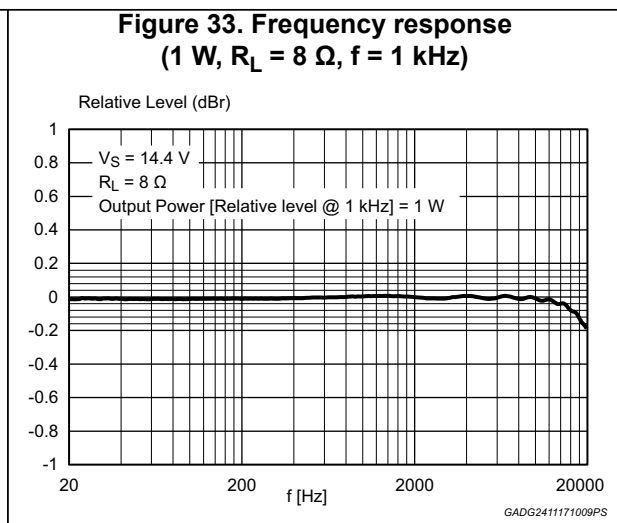
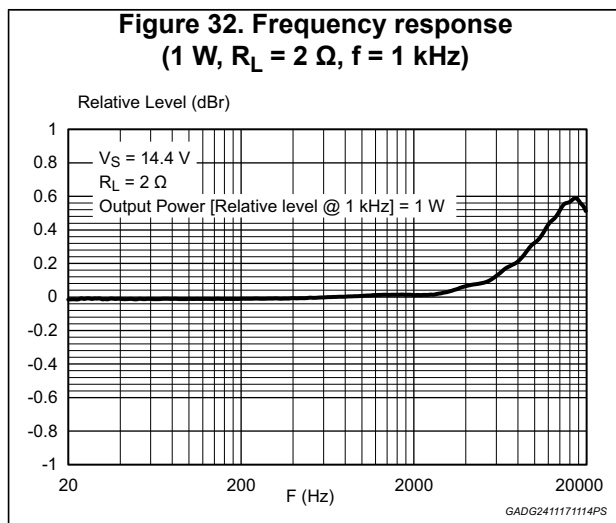
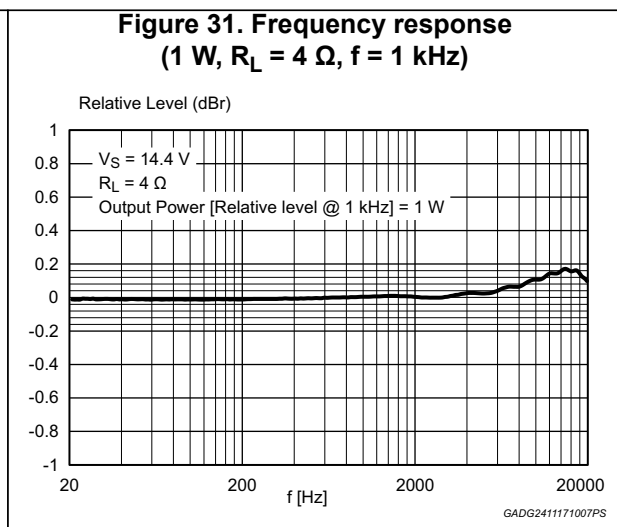
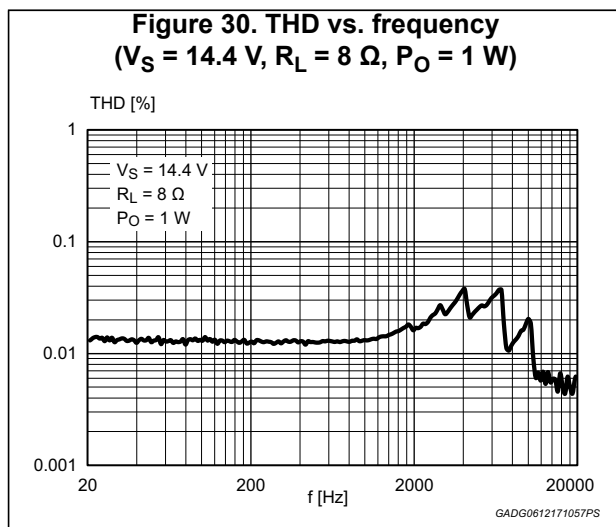
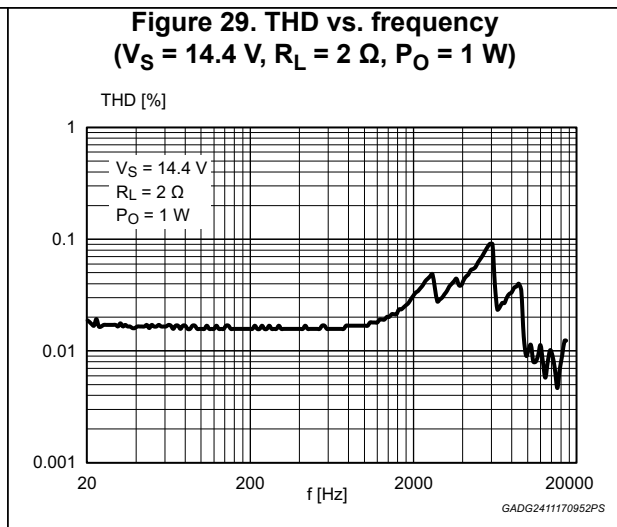
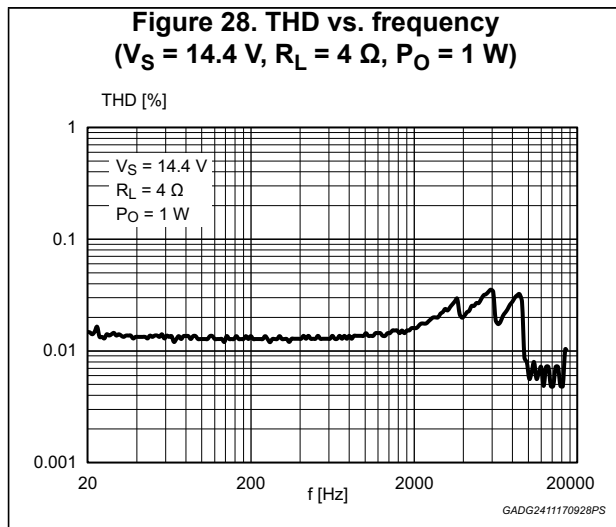


Figure 34. PSRR vs. frequency

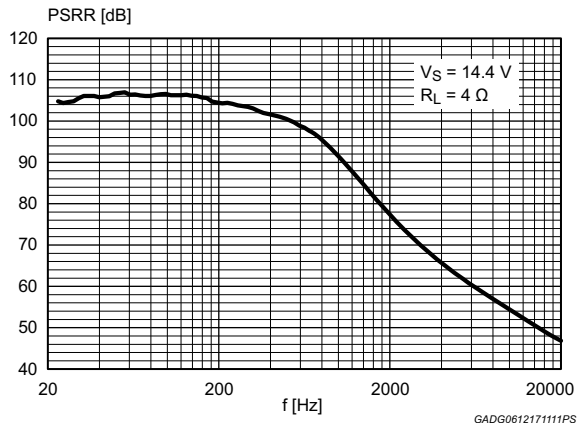


Figure 35. Quiescent current vs. supply voltage

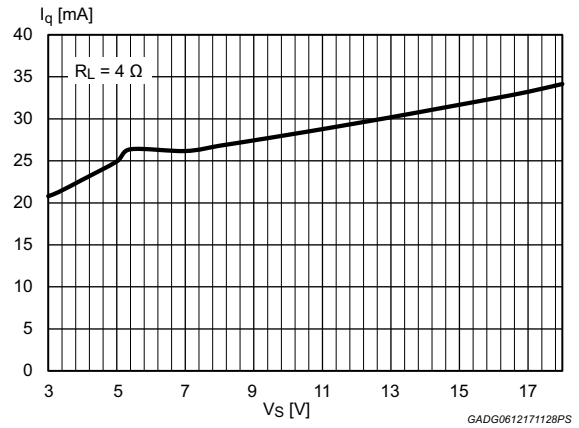


Figure 36. Dynamic range

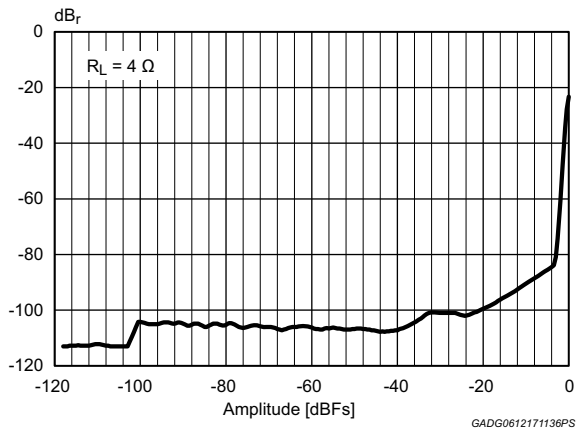
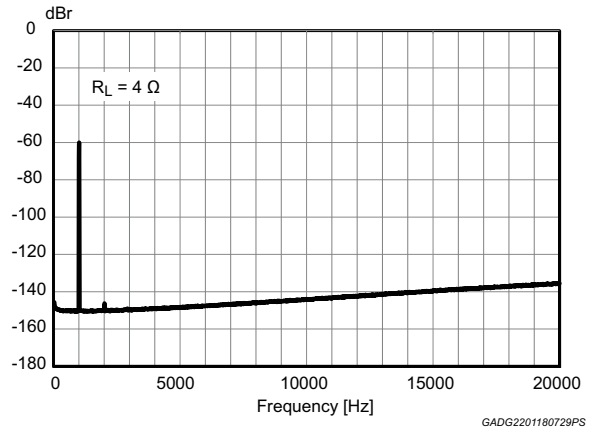


Figure 37. FFT - Output spectrum (-60 dBFS input signal)



## 6 General information

### 6.1 LC filter design

The audio performance of a Class D amplifier are heavily influenced by the characteristics of the output LC filter. The choice of its components is quite critical because a lot of constraints have to be fulfilled at the same time: size, cost, filter for EMI suppression, efficiency. In particular, both the inductor and the capacitor exhibit a non linear behavior: the value of the inductance is a function of the instantaneous current in it and similarly the value of the capacitor is a function of the voltage across it.

In the classical approach, where the feedback loop is closed right at the output of the power stage, the LC filter is placed outside the loop and these nonlinearities cause the Total Harmonic Distortion (THD) to increase. The only way to avoid this phenomenon would be to use components which are highly linear, but this means they are also bigger and/or more expensive.

Furthermore, when the LC filter is outside the loop, its frequency response heavily depends on the impedance of the loudspeaker; this is one of the most critical aspects of Class-D amplifiers. In standard class D this can be mitigated, but not solved, by means of additional damping networks, increasing cost, space and power dissipation. FDA803D, instead, provides a very flat frequency response over audio-band which can not be achieved by standard class D without feedback after LC filter.

Since the demodulator group is now in the feedback path, some constraints regarding the inductor and capacitor choice are still present but of course less stringent than in the case of a typical switching application.

Moreover FDA803D can be used with the 'classical' configuration of feedback on output (before LC filter), through I<sup>2</sup>C configuration, allowing the maximum flexibility. The choice depends mainly on EMI target /requirements and could slightly affect other performances (like damping factor, or THD).

### 6.2 Load possibilities

FDA803D supports several load possibilities, driving 2 Ω, 4 Ω and higher ohmic loads.

Possible channel configurations are:

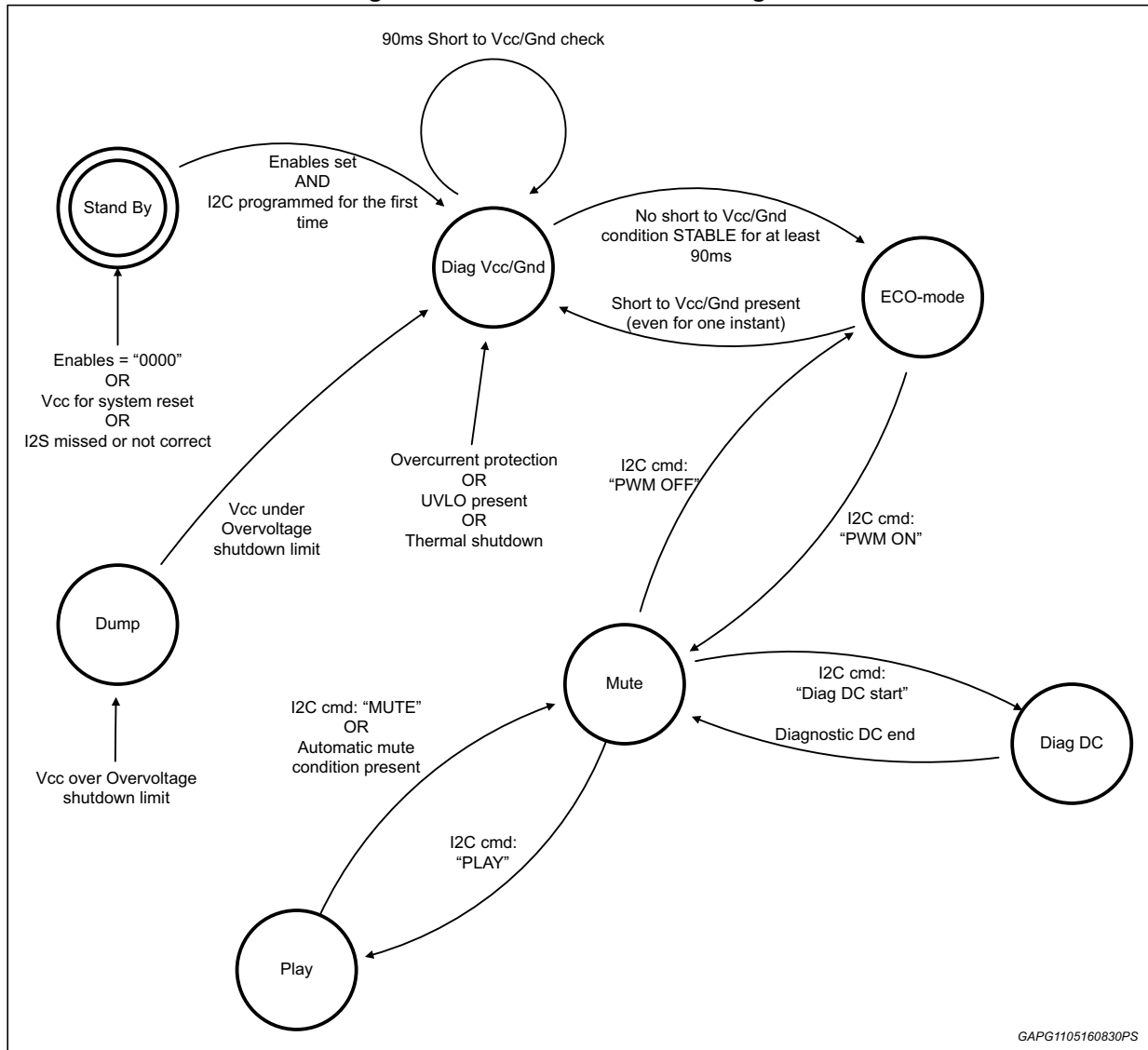
- 1 x 4 ohm (or higher) (up to 18 V)
- 1 x 2 ohm (up to 16 V)



# 7 Finite state machine

FDA803D has a finite state machine which manages amplifier functionality, reacting to user and system inputs

Figure 38. Finite state machine diagram



GAPG1105160830PS

## 7.1 Device state and address selection

Through Enable pins configuration it is possible to select different I<sup>2</sup>C addresses (up to 8) or to configure the device in 4 different legacy ('no I<sup>2</sup>C' modes) according to table 6.

**Table 6. Operation mode**

|   | Enable 1 | Enable 2 | Enable 3 | Enable 4 |
|---|----------|----------|----------|----------|
| Stand By                                      | 0        | 0        | 0        | 0        |
| Amplifier ON address 1 = '1110000'            | 0        | 1        | 0        | 0        |
| Amplifier ON address 2 = '1110001'            | 1        | 1        | 0        | 0        |
| Amplifier ON address 3 = '1110010'            | 0        | 0        | 1        | 0        |
| Amplifier ON address 4 = '1110011'            | 0        | 1        | 1        | 0        |
| Amplifier ON address 5 = '1110100'            | 0        | 1        | 0        | 1        |
| Amplifier ON address 6 = '1110101'            | 1        | 1        | 0        | 1        |
| Amplifier ON address 7 = '1110110'            | 0        | 0        | 1        | 1        |
| Amplifier ON address 8 = '1110111'            | 0        | 1        | 1        | 1        |
| Legacy mode: low voltage mode; in-phase       | 1        | 1        | 1        | 0        |
| Legacy mode: low voltage mode; out-phase      | 1        | 1        | 1        | 1        |
| Legacy mode: standard voltage mode; in-phase  | 1        | 0        | 0        | 0        |
| Legacy mode: standard voltage mode; out-phase | 1        | 0        | 0        | 1        |

In this way, up to 8 devices can be easily used in the same application with a single I<sup>2</sup>C bus. Moreover it is possible to work without I<sup>2</sup>C configuring the voltage range and switching mode to be used.

When a valid combination of Enable 1/2/3/4 is recognized the device turns on all the internal supply voltages and outputs are biased to V<sub>cc</sub>/2.

The internal I<sup>2</sup>C registers are pre-settled in "default condition", waiting for the I<sup>2</sup>C next instruction.

The return in the Standby condition, (all enable pins at 0), will cause the reset of the amplifier. As defined in the finite state machine, The same event will happen if PLL is not locked, I<sup>2</sup>S is missing or not correct, V<sub>cc</sub> for system reset.

FDA803D can work only in I<sup>2</sup>C slave mode.