



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

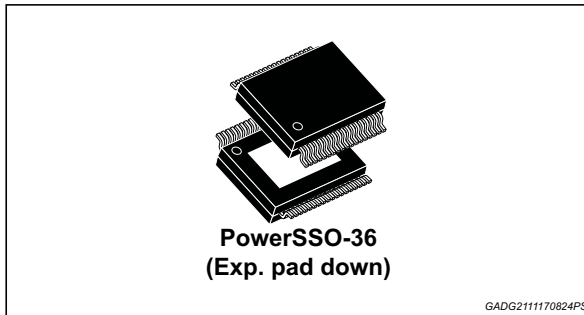
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



1 x 45 W class D digital input automotive power amplifier with I_{Load} current monitoring, wide voltage operation range for car audio and telematic

Datasheet - production data



Features



- AEC-Q100 qualified
- Integrated 108 dB D/A conversion
- I²S and TDM digital input (4/8/16CH TDM)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Full I²C bus driving (3.3/1.8 V)
- CISPR 25 - Class V (Fourth edition)
- Very low quiescent current
- Output lowpass filter included in the feedback allowing outstanding audio performances
- Wide operating supply range from 3.3 to 18 V, suitable for car radio, telematics and e-call
- MOSFET power outputs allowing high output power capability
 - 1 x 25 W /4 Ω @ 14.4 V, 1 kHz THD = 1%
 - 1 x 30 W /4 Ω @ 14.4 V, 1 kHz THD = 10%

- 2 Ω loads driving
- Power limiting function (configurable through I²C)
- I²C bus diagnostics:
 - Short to V_{CC}/GND
 - Short load and open load detection (also in play mode)
 - Four thermal warnings
- DC offset detector (also in play) and 'hot spot' detection
- Clipping detector
- Integrated thermal protection
- Legacy mode ('no I²C' mode), 4 configurable settings
- Short circuit and ESD integrated protections
- Package: PowerSSO-36 exposed pad down

Table 1. Device summary

Order code	Package	Packing
FDA903D-EHT	PowerSSO-36	Tape & reel
FDA903D-EHX	(exposed pad down)	Tube

Contents

1	Description	8
2	Block diagram	9
3	Pins description	10
4	Application diagram	12
5	Electrical specifications	13
	5.1 Absolute maximum ratings	13
	5.2 Thermal data	13
	5.3 Electrical characteristics	14
	5.4 Typical curves of the main electrical parameters	17
6	General information	23
	6.1 LC filter design	23
	6.2 Load possibilities	23
7	Finite state machine	24
	7.1 Device state and address selection	25
	7.2 Standby state	26
	7.3 Diagnostic Vcc-Gnd state	26
	7.4 ECO-mode state	26
	7.5 MUTE-PLAY and diagnostic states	27
	7.6 Operation compatibility vs battery	28
8	Muting function architecture	29
	8.1 Command dependence	29
	8.2 Analog-Mute	30
	8.3 Digital-Mute	30
	8.4 Mixed mute advantages	31
9	Hardware mute pin	33
10	Power limiter function	34

10.1	Power limiter control	35
11	Diagnostic	36
11.1	DC diagnostic	36
11.1.1	Diagnostic control	36
11.1.2	Relation with short circuit protection activation	37
11.1.3	Load range	37
11.2	Short to Vcc / GND diagnostic	38
11.3	Diagnostic time-line diagrams	38
11.4	Open load in play detector	41
11.4.1	Open load in play detector operation overview	41
11.4.2	Processing bandwidth range	41
11.4.3	Audio signal evaluation	42
11.4.4	Impedance threshold	42
11.4.5	I ² C control and timing	43
11.5	Input offset detector	43
11.6	Output voltage offset detector	44
11.7	Output current offset detector	45
11.7.1	Output current offset detector operation principle	45
11.7.2	Result communication and I ² C control	45
11.7.3	Hot spot detection	45
11.8	PWM pulse skipping detector	46
11.9	Thermal protection	47
11.10	Watch-dog	48
11.11	Error frame check	48
12	Additional features	49
12.1	AM operation mode	49
12.2	Noise gating	50
12.3	Dither PWM	50
12.4	Real time load current monitoring	51
12.4.1	Result communication and I ² C control	51
12.4.2	Current sensing limitations	52
13	I²S bus interface	53
13.1	I ² S standard mode description	54

13.2	TDM 4CH mode description	54
13.3	TDM 8CH mode description	55
13.4	TDM 16CH mode description	56
13.5	Timing requirements	57
13.6	Group delay	58
14	I²C bus interface	59
14.1	Writing procedure	60
14.2	Reading procedure	60
14.3	Data validity	61
14.4	Start and stop conditions	61
14.5	Byte format	61
14.6	Acknowledge	61
14.7	I ² C timing	62
14.8	I ² S, I ² C and Enable relationship	63
15	I²C register	64
15.1	Instruction bytes- "100xxxxx"	64
15.2	Data bytes - "101xxxxx"	73
16	Package information	77
16.1	PowerSSO-36 (exposed pad) package information	77
16.2	Package marking information	80
17	Revision history	81

List of tables

Table 1.	Device summary	1
Table 2.	Pins list function	10
Table 3.	Absolute maximum ratings	13
Table 4.	Thermal data - PowerSSO36 slug-down package	13
Table 5.	Electrical characteristics	14
Table 6.	Operation mode	25
Table 7.	Command dependence.	29
Table 8.	Power limiter function	34
Table 9.	Open load in play detector impedance and validity thresholds.	42
Table 10.	I ² S Interface timings	57
Table 11.	Group delay dependency from input sampling frequency.	58
Table 12.	I ² C bus interface timing.	62
Table 13.	IB0-ADDR: "I0000000"	64
Table 14.	IB1-ADDR: "I0000001"	65
Table 15.	IB2-ADDR: "I0000010"	66
Table 16.	IB3-ADDR: "I0000011"	67
Table 17.	IB4-ADDR: "I0000100" - CDDiag pin configuration.	67
Table 18.	IB5-ADDR: "I0000101" - CDDiag pin configuration.	68
Table 19.	IB6-ADDR: "I0000110"	68
Table 20.	IB7-ADDR: "I0000111"	69
Table 21.	IB8-ADDR: "I0001000" - CHANNEL CONTROLS	70
Table 22.	IB9-ADDR: "I0001001"	70
Table 23.	IB10-ADDR: "I0001010"	71
Table 24.	IB11-ADDR: "I0001011"	71
Table 25.	IB12-ADDR: "I0001100"	71
Table 26.	IB13-ADDR: "I0001101"	72
Table 27.	IB14-ADDR: "I0001110"	72
Table 28.	DB0-ADDR: "I0100000"	73
Table 29.	DB1-ADDR: "I0100001"	74
Table 30.	DB2-ADDR: "I0100010"	74
Table 31.	DB3-ADDR: "I0100011" DC Diagnostic Error code	75
Table 32.	DB4-ADDR: "I0100100" - Current Sensing data (10-8)	75
Table 33.	DB5-ADDR: "I0100101" - Current Sensing data (7-0)	75
Table 34.	DB6-ADDR: "I0100110"	76
Table 35.	PowerSSO-36 exposed pad (D1 and E2 use the option variation B) package mechanical data	78
Table 36.	Document revision history.	81

List of figures

Figure 1.	Block diagram	9
Figure 2.	Pins connection diagram	10
Figure 3.	Application diagram	12
Figure 4.	Efficiency and power dissipation ($V_S = 14.4\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ sine wave)	17
Figure 5.	Efficiency and power dissipation ($V_S = 14.4\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ pink noise)	17
Figure 6.	Efficiency and power dissipation ($V_S = 14.4\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ sine wave)	17
Figure 7.	Efficiency and power dissipation ($V_S = 14.4\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ pink noise)	17
Figure 8.	Efficiency and power dissipation ($V_S = 14.4\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ sine wave)	17
Figure 9.	Efficiency and power dissipation ($V_S = 14.4\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ pink noise)	17
Figure 10.	Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ sine wave)	18
Figure 11.	Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ pink noise)	18
Figure 12.	Efficiency and power dissipation ($V_S = 16\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ sine wave)	18
Figure 13.	Efficiency and power dissipation ($V_S = 16\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ pink noise)	18
Figure 14.	Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ sine wave)	18
Figure 15.	Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ pink noise)	18
Figure 16.	Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ sine wave)	19
Figure 17.	Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ pink noise)	19
Figure 18.	Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ sine wave)	19
Figure 19.	Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ pink noise)	19
Figure 20.	Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ sine wave)	19
Figure 21.	Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ pink noise)	19
Figure 22.	Output power vs. supply voltage ($R_L = 4\ \Omega$, sine wave)	20
Figure 23.	Output power vs. supply voltage ($R_L = 2\ \Omega$, sine wave)	20
Figure 24.	Output power vs. supply voltage ($R_L = 8\ \Omega$, sine wave)	20
Figure 25.	THD vs. output power ($V_S = 14.4\text{ V}$, $R_L = 4\ \Omega$)	20
Figure 26.	THD vs. output power ($V_S = 14.4\text{ V}$, $R_L = 2\ \Omega$)	20
Figure 27.	THD vs. output power ($V_S = 14.4\text{ V}$, $R_L = 8\ \Omega$)	20
Figure 28.	THD vs. frequency ($V_S = 14.4\text{ V}$, $R_L = 4\ \Omega$, $P_O = 1\text{ W}$)	21
Figure 29.	THD vs. frequency ($V_S = 14.4\text{ V}$, $R_L = 2\ \Omega$, $P_O = 1\text{ W}$)	21
Figure 30.	THD vs. frequency ($V_S = 14.4\text{ V}$, $R_L = 8\ \Omega$, $P_O = 1\text{ W}$)	21
Figure 31.	Frequency response (1 W, $R_L = 4\ \Omega$, $f = 1\text{ kHz}$)	21
Figure 32.	Frequency response (1 W, $R_L = 2\ \Omega$, $f = 1\text{ kHz}$)	21
Figure 33.	Frequency response (1 W, $R_L = 8\ \Omega$, $f = 1\text{ kHz}$)	21
Figure 34.	PSRR vs. frequency	22
Figure 35.	Quiescent current vs. supply voltage	22
Figure 36.	Dynamic range	22
Figure 37.	FFT - Output spectrum (-60 dBFS input signal)	22
Figure 38.	Finite state machine diagram	24
Figure 39.	Operation vs. battery charge	28
Figure 40.	Analog-Mute diagram	30
Figure 41.	Digital-Mute diagram	31
Figure 42.	Mixed mute diagram	31
Figure 43.	Analog-Mute vs. Mixed-Mute	32
Figure 44.	HWMute pin schematic	33
Figure 45.	Response obtained with a limitation corresponding to 80% of the full-scale	35
Figure 46.	Load range detection configured properly setting IB5 d7-d6	37
Figure 47.	DC diagnostic before turn on	38
Figure 48.	Short to VCC at device turn on	39

Figure 49.	DC Diagnostic in Mute	39
Figure 50.	Short circuit protection activation - Short to VCC	40
Figure 51.	Short Circuit Protection activation due to short across load, short to Vcc/Gnd not present	40
Figure 52.	Open load in play detector guaranteed thresholds with standard gain setting	42
Figure 53.	Open load in play detector guaranteed thresholds with low gain setting	42
Figure 54.	Open load in play detector timing	43
Figure 55.	Output voltage offset detector operation	44
Figure 56.	Current offset measurement	45
Figure 57.	Hot spot detection	46
Figure 58.	PWM pulse skipping detector operation	46
Figure 59.	Thermal attenuation curve	47
Figure 60.	PWM switching frequency selection	49
Figure 61.	LRF effect on PWM output	49
Figure 62.	Dither PWM effect on output PWM	50
Figure 63.	Current sensing path	51
Figure 64.	I ² S standard mode	54
Figure 65.	TDM4 mode	54
Figure 66.	TDM8 mode	55
Figure 67.	TDM16 mode	56
Figure 68.	I ² S Interface timings	57
Figure 69.	I ² S clock transition timings	57
Figure 70.	I ² C bus protocol description	59
Figure 71.	Reading procedure	60
Figure 72.	Without/with auto-increment reading procedure	61
Figure 73.	I ² C bus interface timing	62
Figure 74.	PowerSSO-36 (exposed pad) package outline	77
Figure 75.	PowerSSO-36 (exp. pad) marking information	80

1 Description

The FDA903D is a single bridge class D amplifier, designed in the most advanced BCD technology, intended for any automotive audio application (car radio, telematics and e-call, noise and tone generators, etc).

The FDA903D integrates a high performance D/A converter together with powerful MOSFET outputs in class D, so it is very compact and powerful, moreover reaches outstanding efficiency performances (90%).

It has a very wide operating range: it can be operated both with standard car battery levels (5.5-18 V operating, compatible to load dump pulse) and with external step-down generated voltages or emergency battery (since it is compatible to minimum 3.3 V operative).

The feedback loop is including the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion.

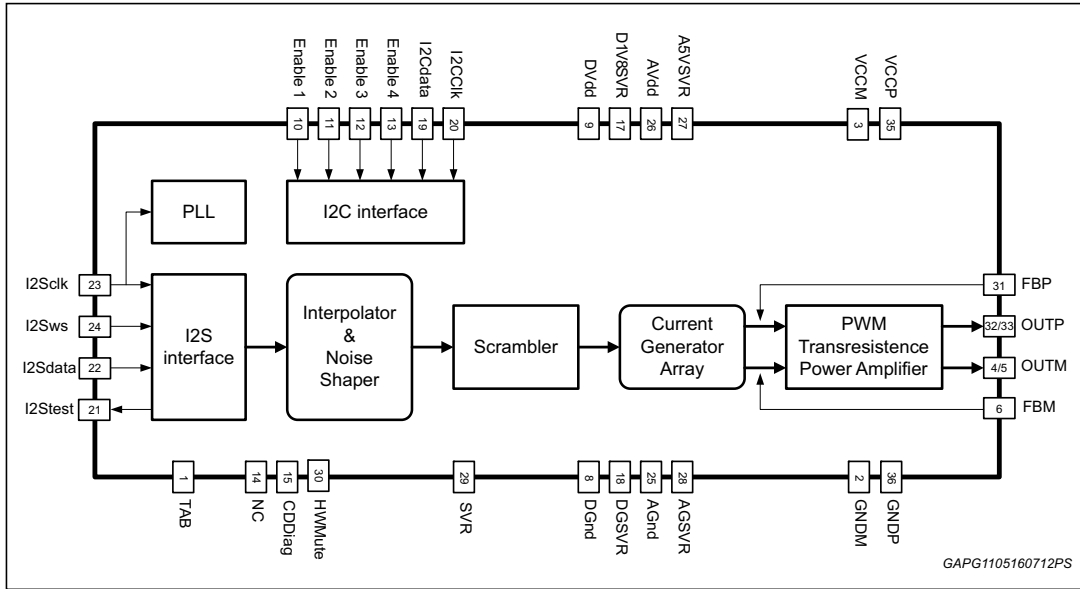
FDA903D is configurable through I²C bus interface and is integrating a complete diagnostics array specially intended for automotive applications including innovative open load and DC offset detection in play mode.

Thanks to the solutions implemented to solve the EMI problems, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover FDA903D features a configurable power limiting function, and can be optionally operated under no I²C mode ('legacy mode').

2 Block diagram

Figure 1. Block diagram



3 Pins description

Figure 2. Pins connection diagram

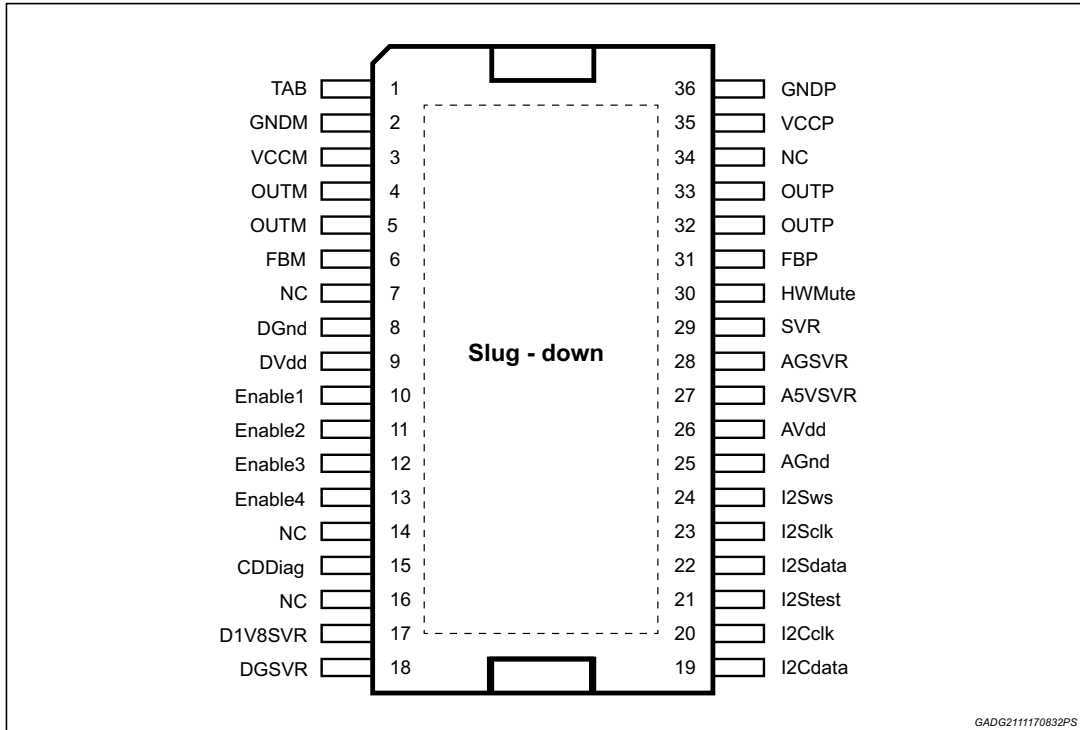


Table 2. Pins list function

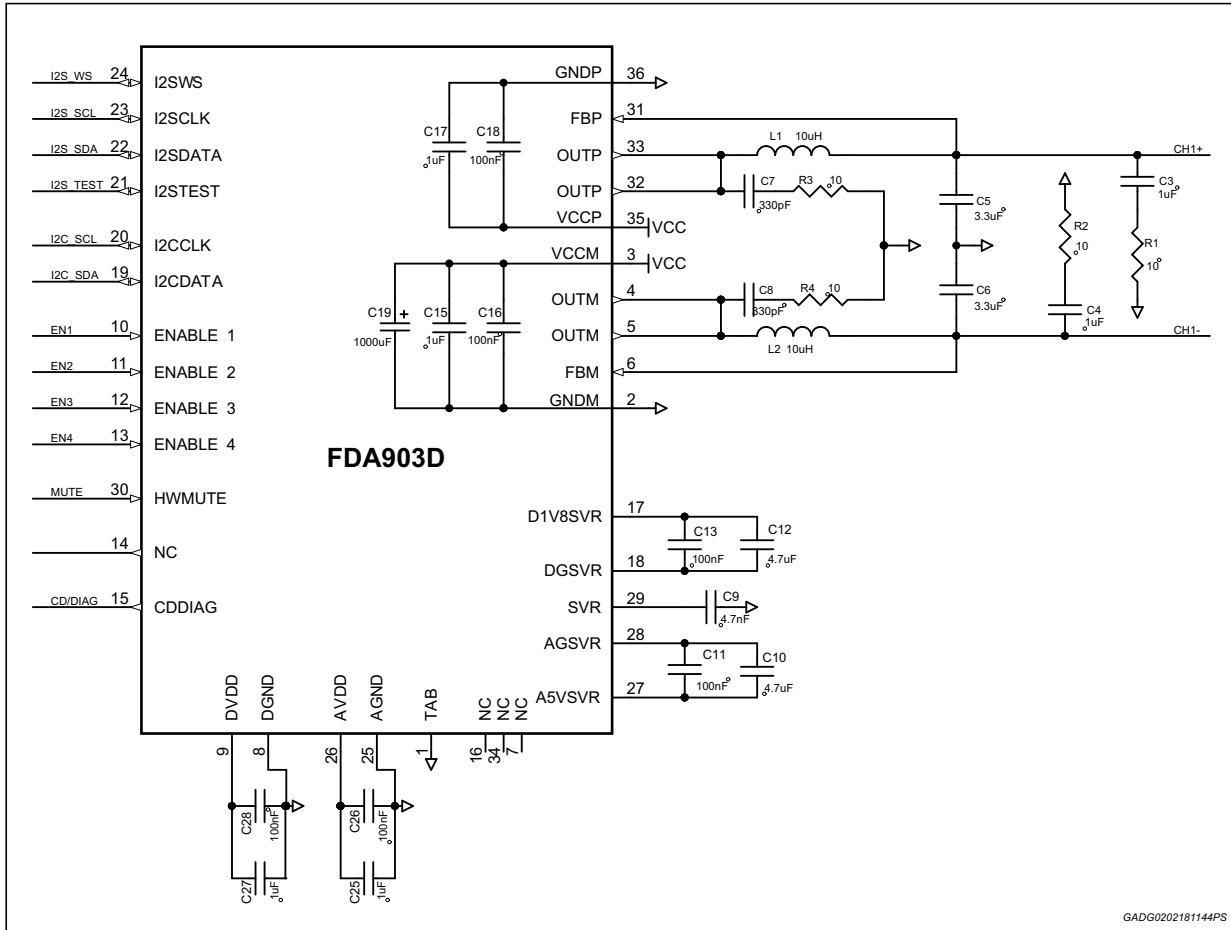
Pin #	Pin name	Function
1	TAB	Device slug connection
2	GNDM	Channel half bridge minus, Power Ground
3	VCCM	Channel half bridge minus, Power Supply
4	OUTM	Channel half bridge minus, Output
5	OUTM	Channel half bridge minus, Output
6	FBM	Channel half bridge minus, Feedback
7	NC	Not connected
8	DGnd	Digital ground
9	DVdd	Digital supply
10	Enable1	Enable 1
11	Enable2	Enable 2
12	Enable3	Enable 3
13	Enable4	Enable 4
14	NC	Not connected
15	CDDiag	Clipping detector and diagnostic output pin

Table 2. Pins list function

Pin #	Pin name	Function
16	NC	Not connected
17	D1V8SVR	Positive digital supply V(SVR)+0.9V (Internally generated)
18	DGSVR	Negative digital supply V(SVR)-0.9V (Internally generated)
19	I2Cdata	I2C Data
20	I2Cclk	I2C Clock
21	I2Stest	test pin, left open
22	I2Sdata	I2S/TDM data
23	I2Sclk	I2S/TDM Clock input
24	I2Sws	I2S/TDM Sync input /Word Select input
25	AGnd	Analog ground
26	AVdd	Analog supply
27	A5VSVR	Positive Analog Supply V(SVR)+2.5V (Internally generated)
28	AGSVR	Negative Analog Supply V(SVR)-2.5V (Internally generated)
29	SVR	Supply Voltage Ripple Rejection Capacitor
30	HWMute	Hardware mute pin
31	FBP	Channel half bridge plus, Feedback
32	OUTP	Channel half bridge plus, Output
33	OUTP	Channel half bridge plus, Output
34	NC	Not connected
35	VCCP	Channel half bridge plus, Power Supply
36	GNDP	Channel half bridge plus, Power Ground

4 Application diagram

Figure 3. Application diagram



GADG0202181144PS

5 Electrical specifications

5.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC} [V_{CCP} , V_{CCM} , A_{VDD} , D_{VDD}]	DC supply voltage	-0.3 to 28	V
	Transient supply voltage for $t = 100 \text{ ms}^{(1)}$	-0.3 to 40	V
GND_{max} [D_{GND} , A_{GND} , $GNDP$, $GNDM$]	Ground pin voltage difference	-0.3 to 0.3	V
I^2C_{data} , I^2C_{clk}	I^2C bus pins voltage	-0.3 to 5.5	V
I^2S_{test} , I^2S_{data} , I^2S_{clk} , I^2S_{ws}	I^2S bus pins voltage	-0.3 to 5.5	V
Enable _{1,2,3,4}	Enables	-0.3 to 5.5	V
HWMute	Hardware mute	-0.3 to 7	V
CDDiag	Clip detection	-0.3 to 5.5	V
I_o	Output current (repetitive $f > 10 \text{ Hz}$)	Internally limited	A
T_{amb}	Ambient operating temperature	-40 to 125	°C
T_{stg} , T_j	Storage and junction temperature	-55 to 150	°C
ESDHBM	ESD protection HBM	2000	V
ESDCDM	ESD protection CDM	500	V

1. $V_{CC} = 35 \text{ V}$ for $t < 400 \text{ ms}$ as per ISO16750-2 load dump with centralized load dump suppression.

5.2 Thermal data

Table 4. Thermal data - PowerSSO36 slug-down package

Symbol	Parameter	Value	Unit
$R_{th \text{ j-a-2s}}$	Thermal resistance junction-to-ambient (2s board)	56	°C/W
$R_{th \text{ j-a-2s2p}}$	Thermal resistance junction-to-ambient (2s2p board)	31	°C/W
$R_{th \text{ j-a-2s2pv}}$	Thermal resistance junction-to-ambient (2s2p+vias)	26	°C/W

5.3 Electrical characteristics

$V_{CC} = 14.4\text{ V}$; $R_L = 4\ \Omega$; $f = 1\text{ kHz}$; $T_{amb} = 25\text{ }^\circ\text{C}$; I²C defaults, unless otherwise specified. LC filter: $L = 10\ \mu\text{H}$, $C = 3.3\ \mu\text{F}$. PWM in In-phase modulation, feedback connected after the filter.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage range	$R_L = 4\ \Omega$	3.3	-	18	V
		$R_L = 2\ \Omega$ ⁽¹⁾	3.3	-	16	
I_{VCC}	Quiescent current	Device in Standby	-	1	5	μA
		Device on (MUTE state)	-	35	-	mA
		ECO MODE	-	22	-	mA
V_{os}	Offset voltage	Mute & Play	-10	-	+10	mV
D_{VDD}	Digital supply voltage range	-	3.3	-	18	V
A_{VDD}	Analog supply voltage range	-	3.3	-	18	V
I_{op}	Overcurrent protection	IB11 D5-4 = 00	9.5	11	12.5	A
		IB11 D5-4 = 01	6.7	8	9.3	A
		IB11 D5-4 = 10	5	6	7	A
		IB11 D5-4 = 11	3	4	5	A
I_{AVDD}	Analog current	Device on (MUTE state)	-	9	20	mA
I_{DVDD}	Digital current	Device on (MUTE state)	-	13	20	mA
-	Overvoltage shutdown	Attenuation = 0.5 dB ⁽²⁾	18.5	19.5	20.5	V
V_{lowM}	V_{CC} low supply mute threshold	Attenuation <0.5 dB Low voltage mode (IB0D0=1)	2.7	2.9	3.3	V
		Attenuation <0.5 dB Standard mode (IB0D0=0)	4.5	4.7	5	V
V_{highM}	V_{CC} high voltage mute ⁽²⁾	-	18	18.9	20.3	V
$UVLO_{VCC}$	V_{CC} supply UVLO threshold	Standard mode (IB0D0=0)	4.4	4.6	4.8	V
		Low voltage mode (IB0D0=1)	2.55	2.7	2.85	V
T_{sh}	Thermal shutdown	-	165	175	185	$^\circ\text{C}$
T_{pl}	Thermal protection junction temperature	Attenuation = 0.5 dB	150	160	170	$^\circ\text{C}$
T_{w1}	Thermal warning junction temperature ⁽³⁾	-	-	Tpl-5	-	$^\circ\text{C}$
T_{w2}		-	-	Tpl-15	-	$^\circ\text{C}$
T_{w3}		-	-	Tpl-35	-	$^\circ\text{C}$
T_{w4}		-	-	Tpl-50	-	$^\circ\text{C}$

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Audio performances						
P _O	Output power	THD = 10 %	-	30	-	W
		THD = 1 %	-	25	-	W
		Max power; V _{CC} = 15.2 V	-	50	-	W
		R _L = 2 Ω THD = 10% ⁽¹⁾	-	55	-	W
		R _L = 2 Ω THD = 1% ⁽¹⁾	-	45	-	W
		R _L = 2 Ω, max power ⁽¹⁾	-	80	-	W
P _O	Output power	THD = 10% V _{CC} = 5 V	-	3.8	-	W
		THD = 10% V _{CC} = 3.3 V	-	1.6	-	W
PSRR	Power supply rejection ratio	f = 1 kHz; Vr = 1Vpk;	70	80	-	-
THD	Total harmonic distortion	P _O = 1 W, f = 1 kHz	-	0.01	0.05	%
Gain	Standard gain	at Amplitude = -10 dBFs	5.5	5.9	6.3	Vp
	Low gain ⁽⁴⁾		3.3	3.6	3.9	Vp
DR	Dynamic range	A-wtd and brickwall 20 kHz filter	102	107.5	-	dB
SNR	Signal to noise ratio	A-wtd and brickwall 20 kHz filter	107	112	-	dB
Eout1	Output noise	A-wtd and brickwall 20 kHz filter used, no output signal;	-	35	55	μV
Eout2	Output noise	CCIR 468 filtered	-	84	130	μV
ΔV _{OITU}	ITU Pop filter output voltage	Standby to Mute and Mute to Standby transition	-7.5	-	+7.5	mV
Mute						
V _{Mth} ⁽⁵⁾	Mute pin voltage threshold	Attenuation <0.5 dB, and digital mute disabled	2.3	-	-	V
		Attenuation ≥60 dB, and digital mute disabled	-	-	1	
I _M	Mute pin source current	-	9	11	13	μA
V _{Mcl}	Mute pin internal clamp voltage	-	5.5	6	6.5	V
I _{feed}	Peak current flowing in the feedback pins	Standby condition, all feedbacks forced to V _{CC} , output floating	-	110	130	μA
I²C bus interface						
f _{SCL}	Clock frequency	-	-	-	400	kHz
V _{IL}	I2C pins low voltage	-	-	-	0.8	V
V _{IH}	I2C pins high voltage	-	1.3	-	-	V
V _{OLMAX}	Maximum I2C data pin low voltage when current I _{sink} is sinked	I _{sink} = 4 mA	-	0.12	0.5	V
I _{LIMAX}	Maximum input leakage current	V = 3.6 V	-	-	1	μA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I²S bus interface						
V _{IL-I2S}	I2S pins low voltage	-	-	-	0.8	V
I _L	Input logic current, low	V _I = 0 V	-	-	500	nA
V _{IH-I2S}	I2S pins high voltage	-	1.3	-	-	V
I _H	Input logic current, high	V _I = TBD	-	-	500	nA
Control pins characteristics						
V _{ENL}	Enable pins low voltage	-	-	-	0.9	V
V _{ENH}	Enable pins high voltage	-	2.4	-	-	V
Clipping and offset detector						
CD _{THD}	Clip det THD ⁽⁶⁾	THD @ 100 Hz with average V _{clipdet} = 2 V	5	7	9	%
CDSAT	Clip det sat. voltage	CD on; I _{CD} = 1 mA	-	150	300	mV
CD _{LK}	Clip det leakage current	CD pin at 3.6 V	-	-	15	μA
V _{offin}	Input DC offset detection threshold	Theshold at which an offset present at inputs is detected	-	-18	-	dB
V _{offout}	Output DC offset detection threshold ⁽⁷⁾	Input high pass filter disable	±1.4	±2	±2.6	V

1. If outphase modulation selected, slow slope configuration must be used (IB11,D3)
2. Parameter values based on bench measurements (guaranteed by correlation with overvoltage shutdown).
3. The thermal warnings are always in tracking.
4. When selecting the low gain, also the thresholds for "DC diagnostic" function and "Open load in play detector" function scale of the same factor with respect to standard gain configuration.
5. See [Chapter 8: Muting function architecture](#) for more details.
6. Guaranteed by correlation.
7. Measured at bench during product validation.

5.4 Typical curves of the main electrical parameters

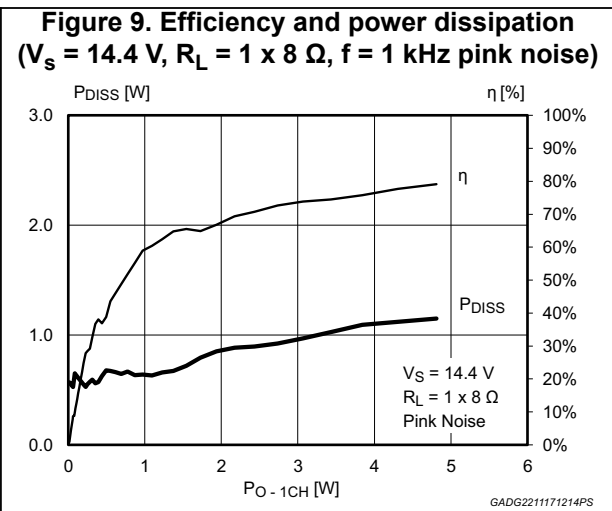
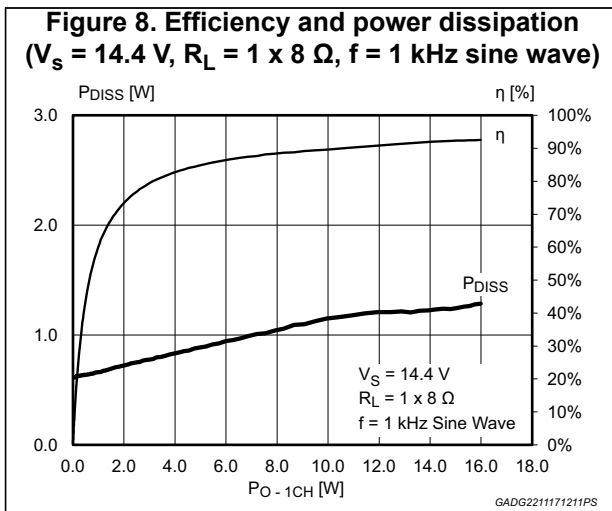
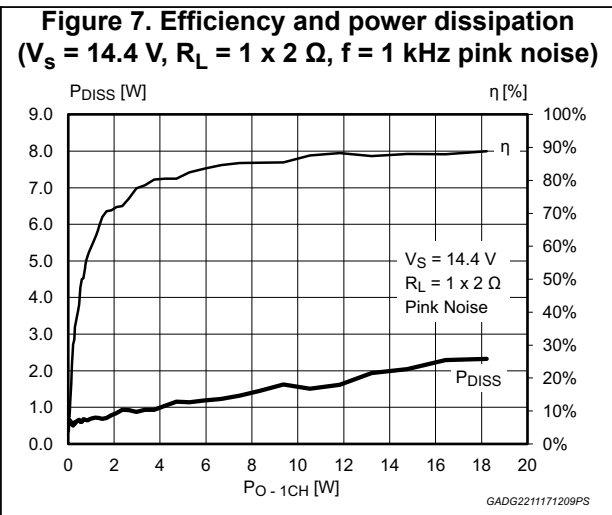
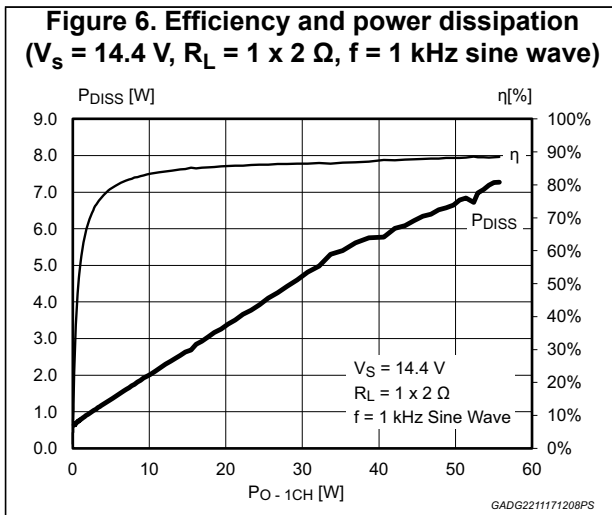
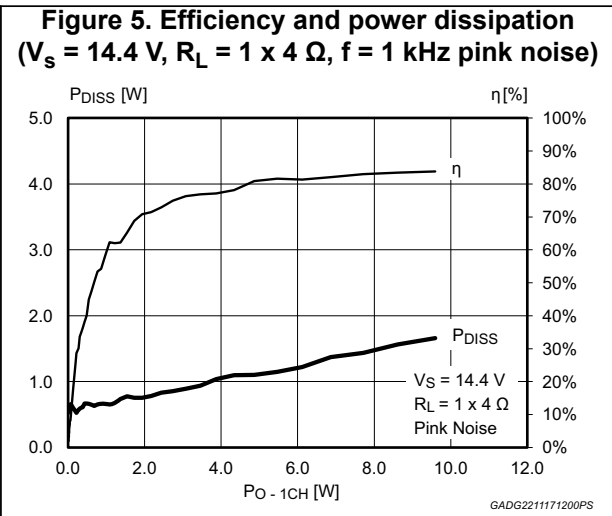
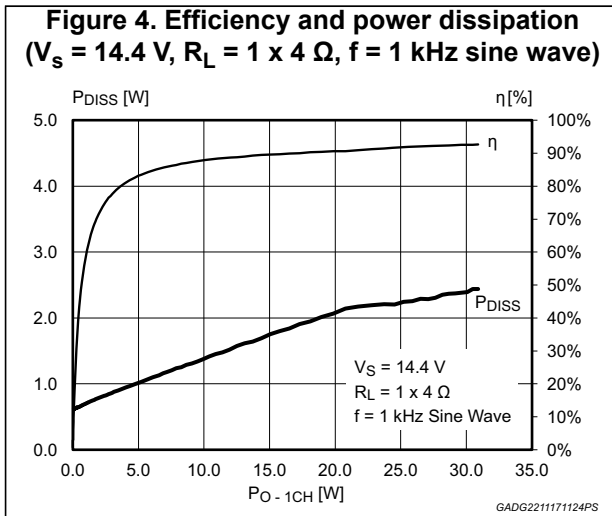
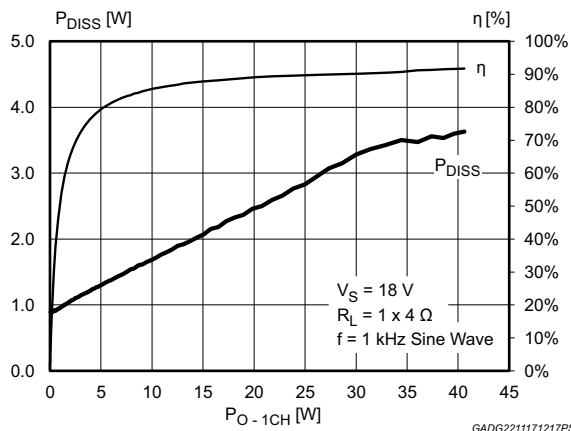
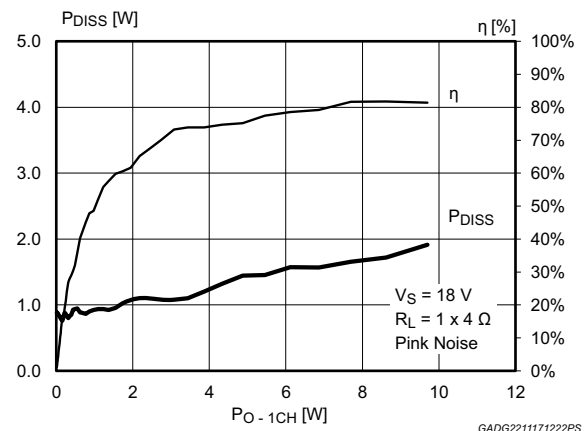


Figure 10. Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ sine wave)



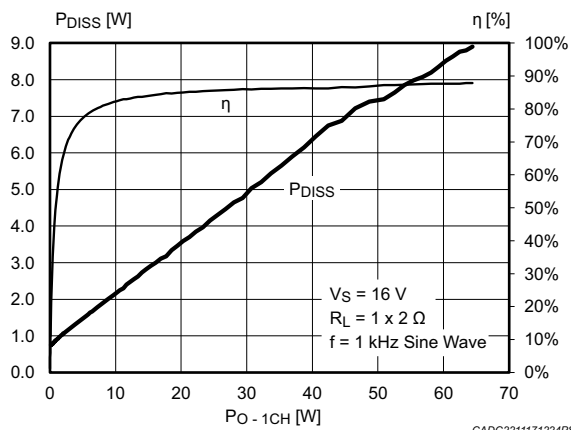
GADG2211171217PS

Figure 11. Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ pink noise)



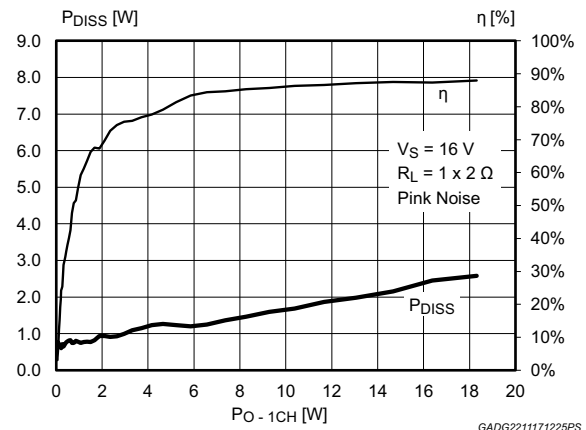
GADG2211171222PS

Figure 12. Efficiency and power dissipation ($V_S = 16\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ sine wave)



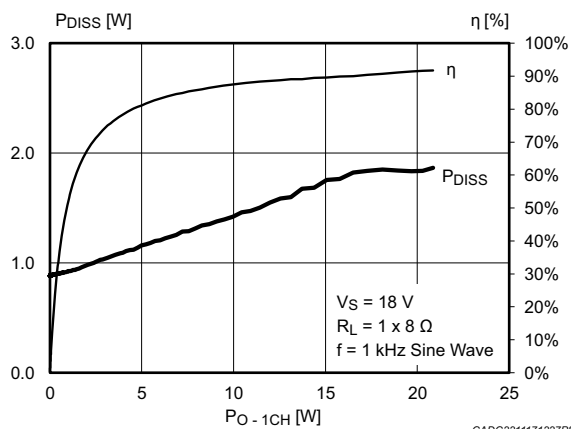
GADG2211171224PS

Figure 13. Efficiency and power dissipation ($V_S = 16\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ pink noise)



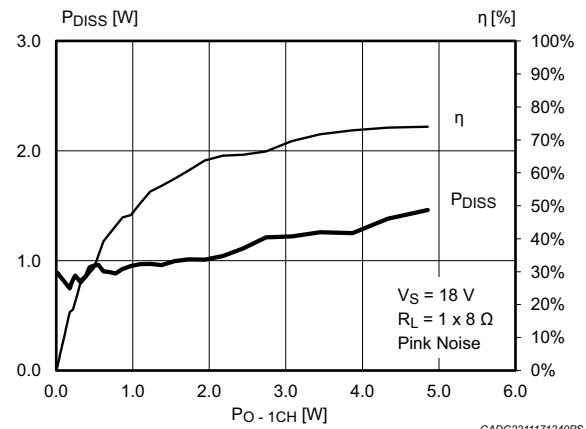
GADG2211171225PS

Figure 14. Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ sine wave)



GADG2211171227PS

Figure 15. Efficiency and power dissipation ($V_S = 18\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ pink noise)



GADG2211171240PS

Figure 16. Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ sine wave)

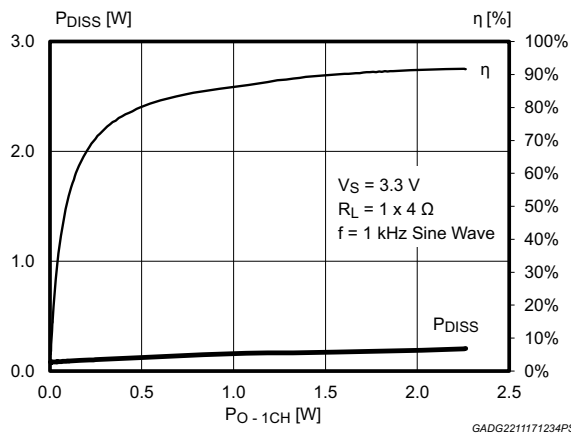


Figure 17. Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 4\ \Omega$, $f = 1\text{ kHz}$ pink noise)

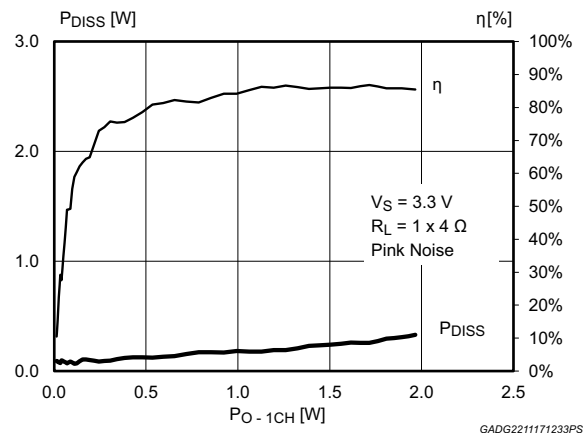


Figure 18. Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ sine wave)

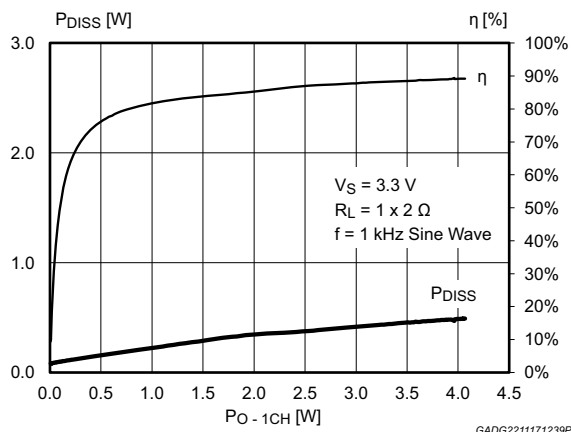


Figure 19. Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 2\ \Omega$, $f = 1\text{ kHz}$ pink noise)

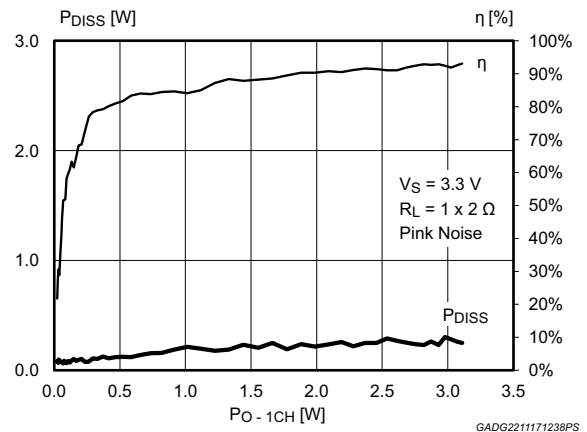


Figure 20. Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ sine wave)

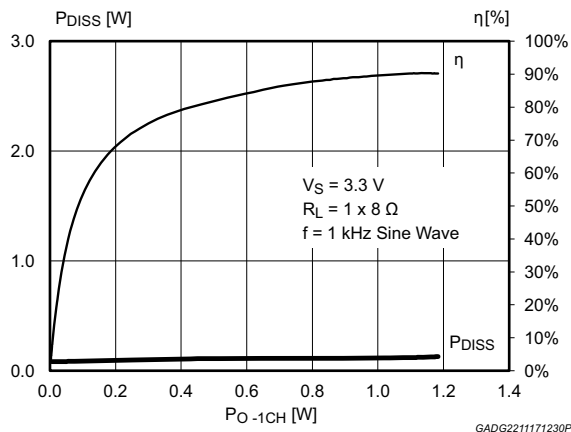


Figure 21. Efficiency and power dissipation ($V_S = 3.3\text{ V}$, $R_L = 1 \times 8\ \Omega$, $f = 1\text{ kHz}$ pink noise)

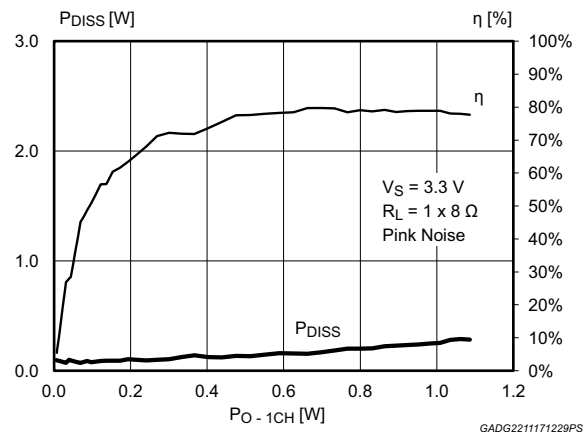
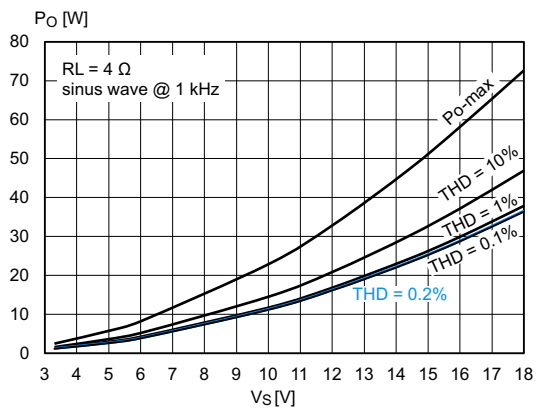
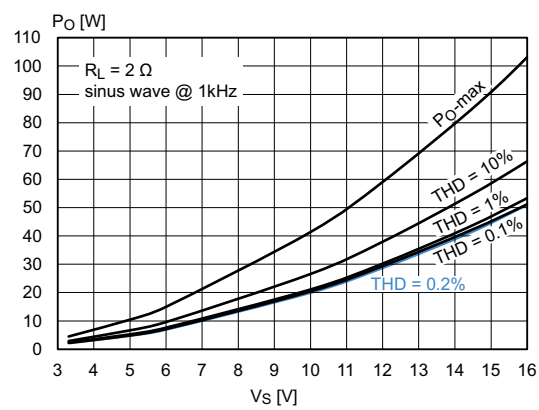


Figure 22. Output power vs. supply voltage
($R_L = 4 \Omega$, sine wave)



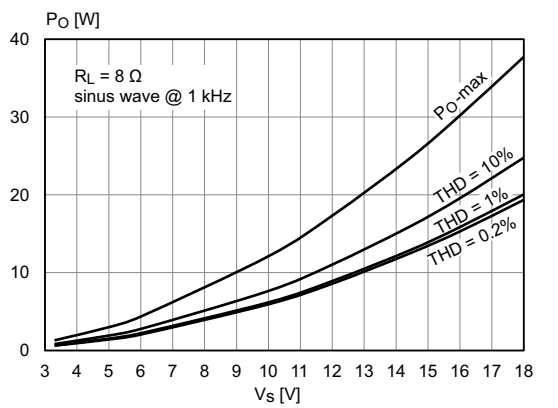
GADG2311171333PS

Figure 23. Output power vs. supply voltage
($R_L = 2 \Omega$, sine wave)



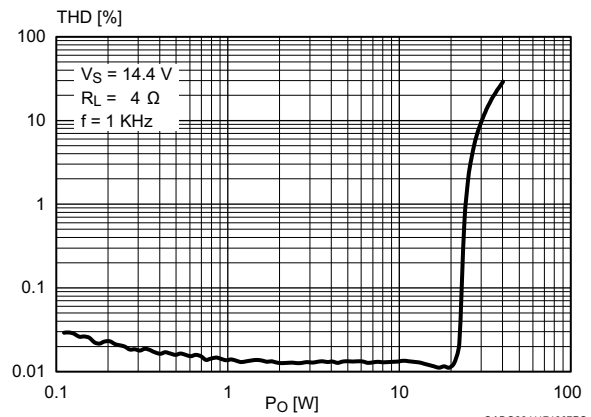
GADG2311171519PS

Figure 24. Output power vs. supply voltage
($R_L = 8 \Omega$, sine wave)



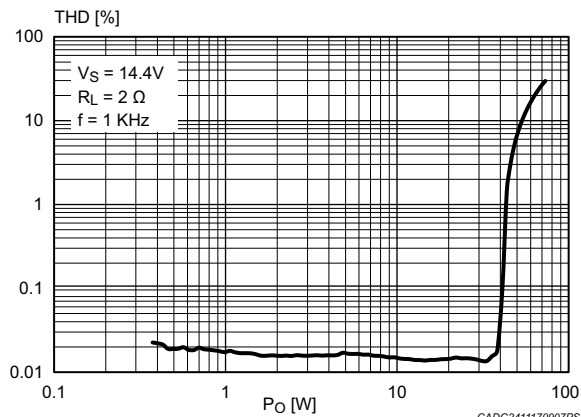
GADG2311171306PS

Figure 25. THD vs. output power
($V_S = 14.4 V$, $R_L = 4 \Omega$)



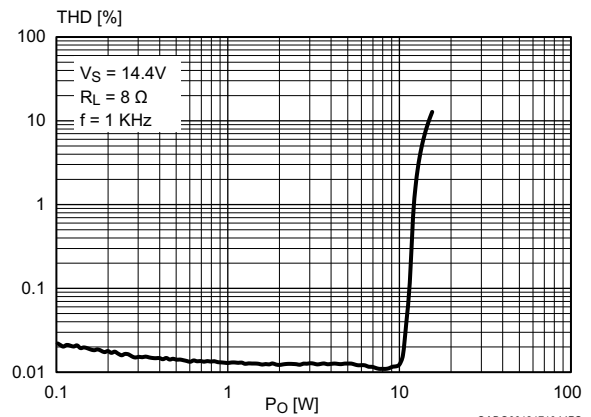
GADG2311171307PS

Figure 26. THD vs. output power
($V_S = 14.4 V$, $R_L = 2 \Omega$)

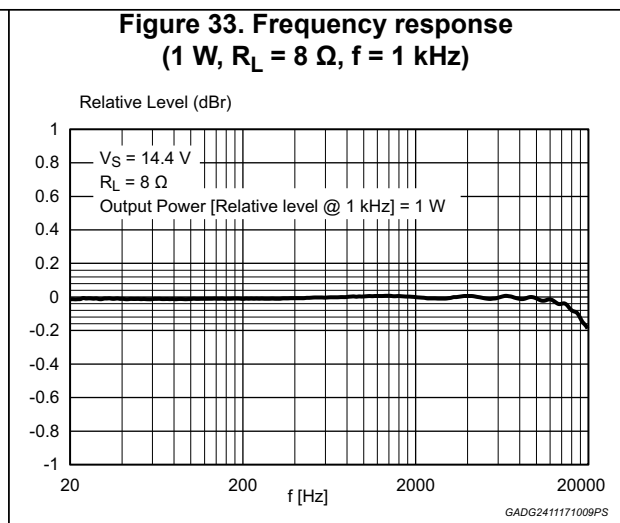
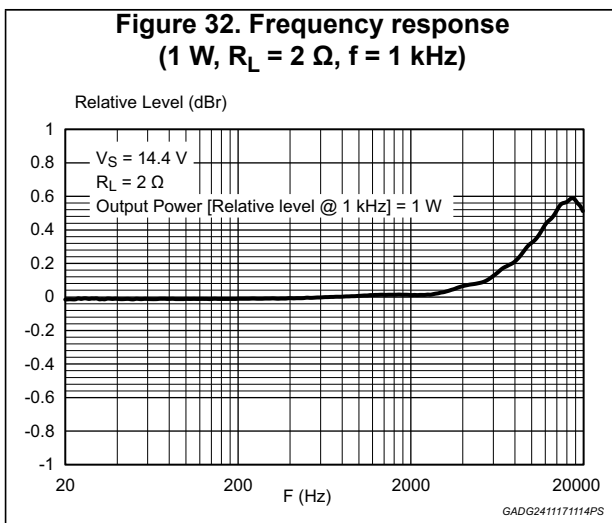
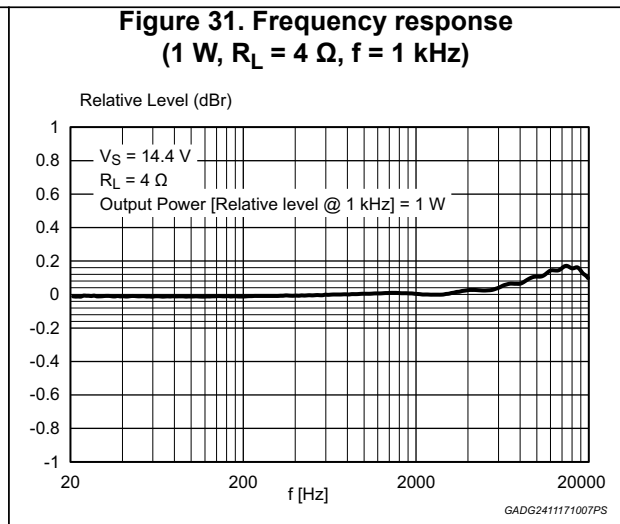
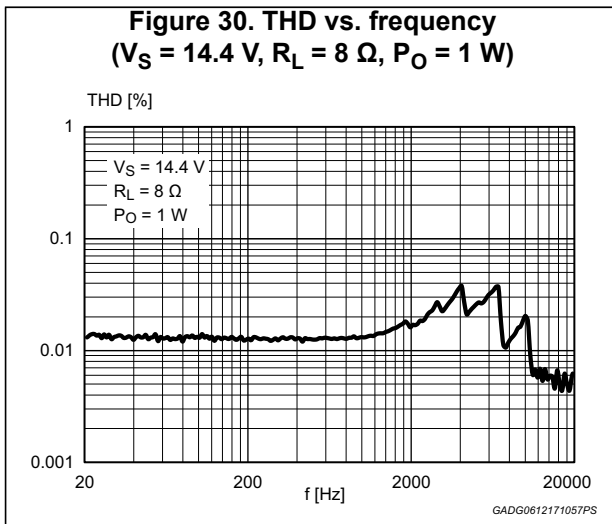
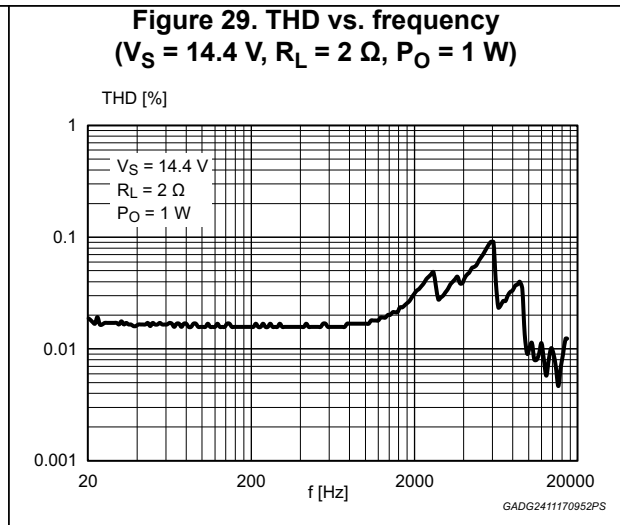
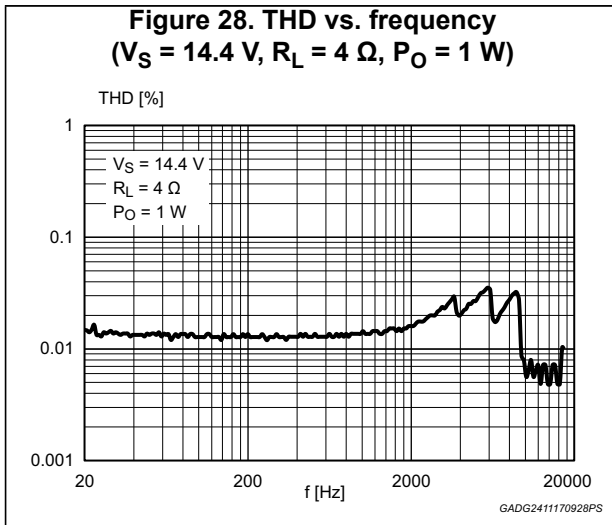


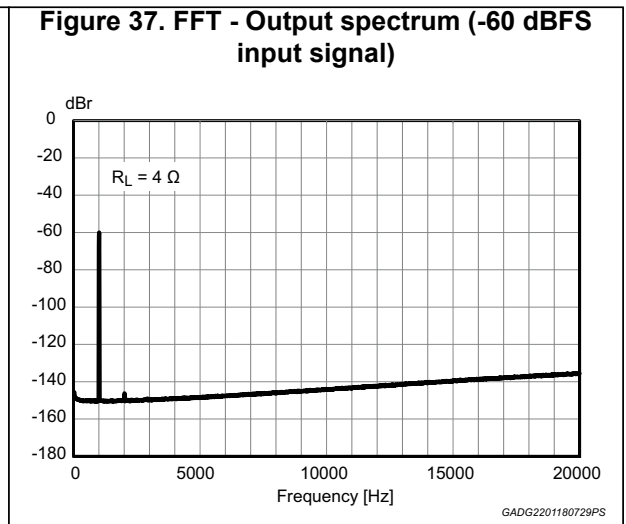
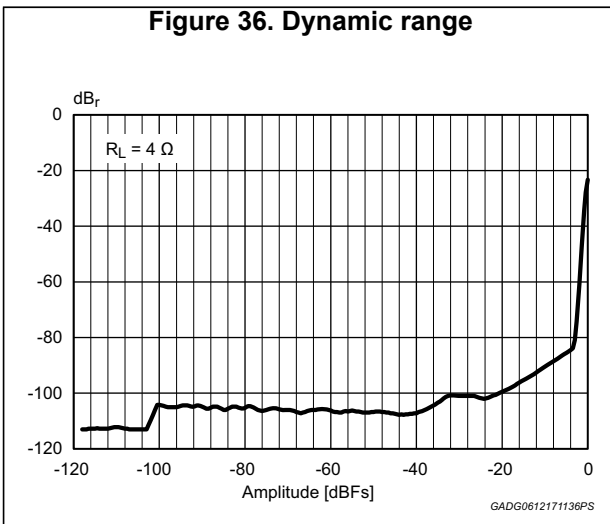
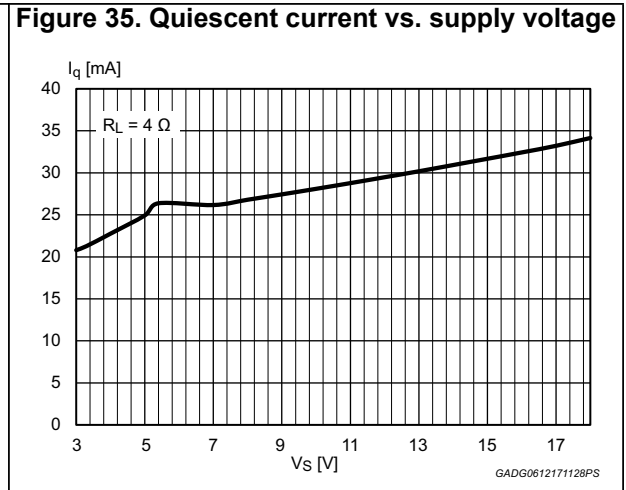
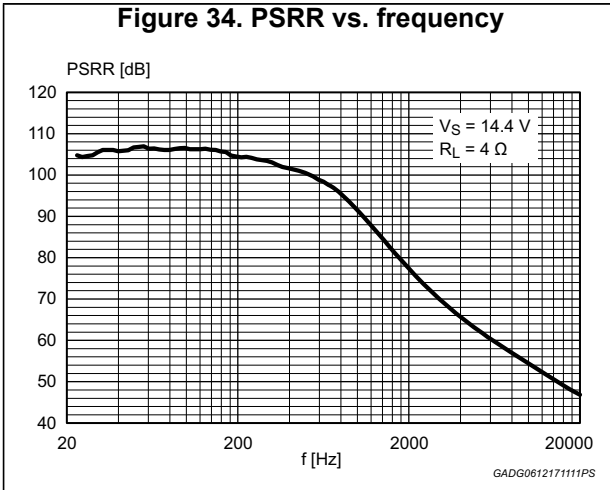
GADG2411170907PS

Figure 27. THD vs. output power
($V_S = 14.4 V$, $R_L = 8 \Omega$)



GADG0612171044PS





6 General information

6.1 LC filter design

The audio performance of a Class D amplifier are heavily influenced by the characteristics of the output LC filter. The choice of its components is quite critical because a lot of constraints have to be fulfilled at the same time: size, cost, filter for EMI suppression, efficiency. In particular, both the inductor and the capacitor exhibit a non linear behavior: the value of the inductance is a function of the instantaneous current in it and similarly the value of the capacitor is a function of the voltage across it.

In the classical approach, where the feedback loop is closed right at the output of the power stage, the LC filter is placed outside the loop and these nonlinearities cause the Total Harmonic Distortion (THD) to increase. The only way to avoid this phenomenon would be to use components which are highly linear, but this means they are also bigger and/or more expensive.

Furthermore, when the LC filter is outside the loop, its frequency response heavily depends on the impedance of the loudspeaker; this is one of the most critical aspects of Class-D amplifiers. In standard class D this can be mitigated, but not solved, by means of additional damping networks, increasing cost, space and power dissipation. FDA903D, instead, provides a very flat frequency response over audio-band which can not be achieved by standard class D without feedback after LC filter.

Since the demodulator group is now in the feedback path, some constraints regarding the inductor and capacitor choice are still present but of course less stringent than in the case of a typical switching application.

Moreover FDA903D can be used with the 'classical' configuration of feedback on output (before LC filter), through I²C configuration, allowing the maximum flexibility. The choice depends mainly on EMI target /requirements and could slightly affect other performances (like damping factor, or THD).

6.2 Load possibilities

FDA903D supports several load possibilities, driving 2 Ω , 4 Ω and higher ohmic loads.

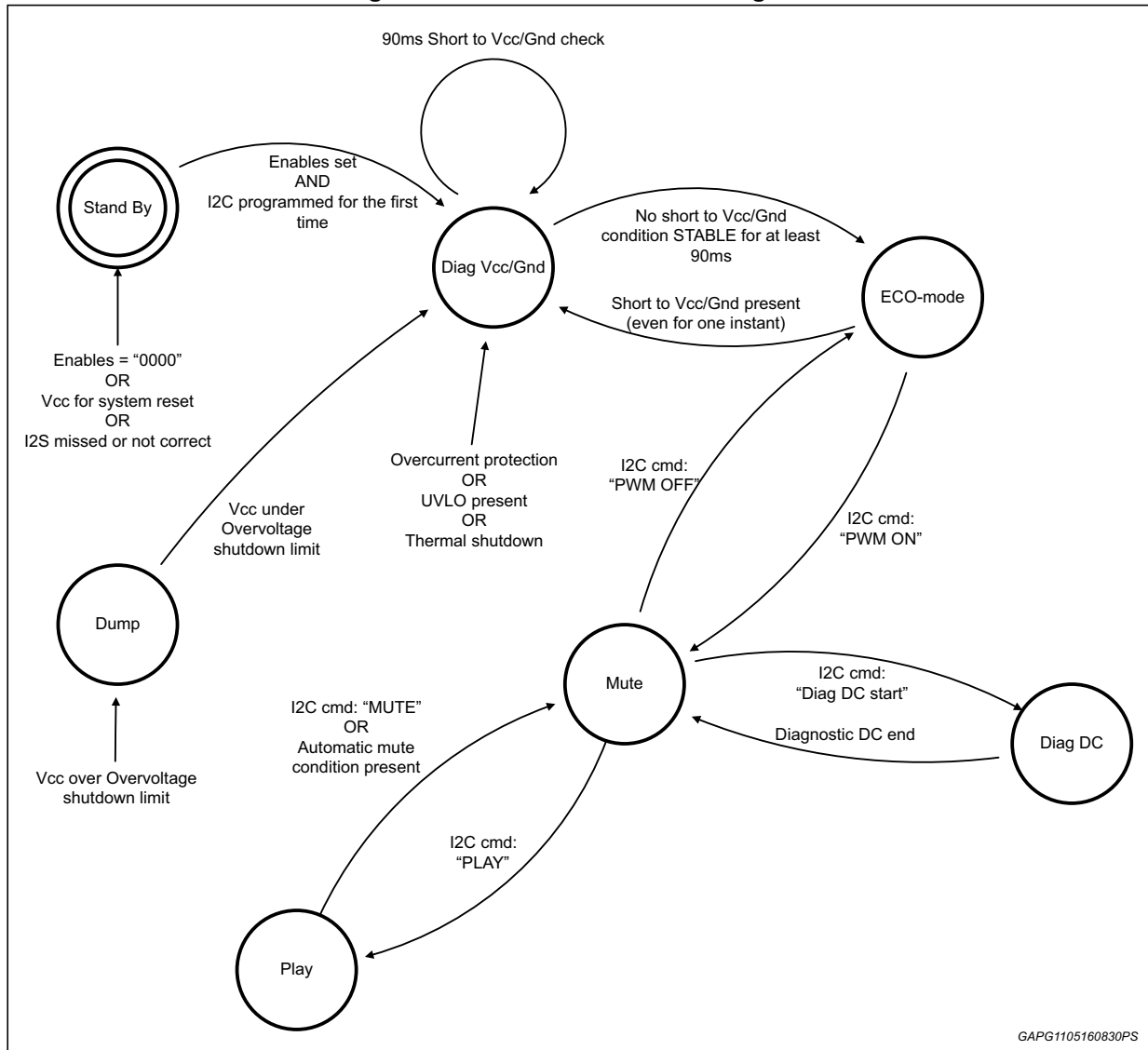
Possible channel configurations are:

- 1 x 4 ohm (or higher) (up to 18 V)
- 1 x 2 ohm (up to 16 V)

7 Finite state machine

FDA903D has a finite state machine which manages amplifier functionality, reacting to user and system inputs

Figure 38. Finite state machine diagram



7.1 Device state and address selection

Through Enable pins configuration it is possible to select different I²C addresses (up to 8) or to configure the device in 4 different legacy ('no I²C' modes) according to table 6.

Table 6. Operation mode

	Enable 1	Enable 2	Enable 3	Enable 4
Stand By	0	0	0	0
Amplifier ON address 1 = '1110000'	0	1	0	0
Amplifier ON address 2 = '1110001'	1	1	0	0
Amplifier ON address 3 = '1110010'	0	0	1	0
Amplifier ON address 4 = '1110011'	0	1	1	0
Amplifier ON address 5 = '1110100'	0	1	0	1
Amplifier ON address 6 = '1110101'	1	1	0	1
Amplifier ON address 7 = '1110110'	0	0	1	1
Amplifier ON address 8 = '1110111'	0	1	1	1
Legacy mode: low voltage mode; in-phase	1	1	1	0
Legacy mode: low voltage mode; out-phase	1	1	1	1
Legacy mode: standard voltage mode; in-phase	1	0	0	0
Legacy mode: standard voltage mode; out-phase	1	0	0	1

In this way, up to 8 devices can be easily used in the same application with a single I²C bus. Moreover it is possible to work without I²C configuring the voltage range and switching mode to be used.

When a valid combination of Enable 1/2/3/4 is recognized the device turns on all the internal supply voltages and outputs are biased to V_{cc}/2.

The internal I²C registers are pre-settled in "default condition", waiting for the I²C next instruction.

The return in the Standby condition, (all enable pins at 0), will cause the reset of the amplifier. As defined in the finite state machine, The same event will happen if PLL is not locked, I²S is missing or not correct, V_{cc} for system reset.

FDA903D can work only in I²C slave mode.