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FDAF59N30

300V N-Channel MOSFET

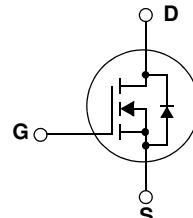
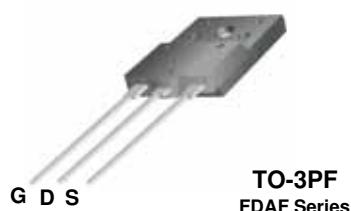
Features

- 34A, 300V, $R_{DS(on)} = 0.056\Omega$ @ $V_{GS} = 10\text{ V}$
- Low gate charge (typical 77 nC)
- Low C_{rss} (typical 80 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



Absolute Maximum Ratings

Symbol	Parameter	FDAF59N30	Unit
V_{DSS}	Drain-Source Voltage	300	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	34 20	A A
I_{DM}	Drain Current - Pulsed	(Note 1)	A
V_{GSS}	Gate-Source voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	161 1.3	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.77	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDAF59N30	FDAF59N30	TO-3PF	-	-	30

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units		
Off Characteristics								
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	300	--	--	V		
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	--	0.3	--	$\text{V}/^\circ\text{C}$		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 300\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = 240\text{V}$, $T_C = 125^\circ\text{C}$	-- --	-- --	1 10	μA μA		
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{V}$, $V_{DS} = 0\text{V}$	--	--	100	nA		
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{V}$, $V_{DS} = 0\text{V}$	--	--	-100	nA		
On Characteristics								
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	3.0	--	5.0	V		
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{V}$, $I_D = 17\text{A}$	--	0.047	0.056	Ω		
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}$, $I_D = 17\text{A}$	(Note 4)	52	--	S		
Dynamic Characteristics								
C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$		--	3590	pF		
C_{oss}	Output Capacitance			--	710	pF		
C_{rss}	Reverse Transfer Capacitance			--	80	pF		
Switching Characteristics								
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 150\text{V}$, $I_D = 59\text{A}$ $R_G = 25\Omega$	(Note 4, 5)	--	140	290	ns	
t_r	Turn-On Rise Time			--	575	1160	ns	
$t_{d(off)}$	Turn-Off Delay Time			--	120	250	ns	
t_f	Turn-Off Fall Time			--	200	410	ns	
Q_g	Total Gate Charge	$V_{DS} = 240\text{V}$, $I_D = 59\text{A}$ $V_{GS} = 10\text{V}$		--	77	100	nC	
Q_{gs}	Gate-Source Charge			--	22	--	nC	
Q_{gd}	Gate-Drain Charge			--	40	--	nC	
Drain-Source Diode Characteristics and Maximum Ratings								
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	34	A		
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	136	A		
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = 34\text{A}$	--	--	1.4	V		
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}$, $I_S = 59\text{A}$ $dI_F/dt = 100\text{A}/\mu\text{s}$	(Note 4)	--	246	--	ns	
Q_{rr}	Reverse Recovery Charge			--	6.9	--	μC	

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 2.5\text{mH}$, $I_{AS} = 34\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 34\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

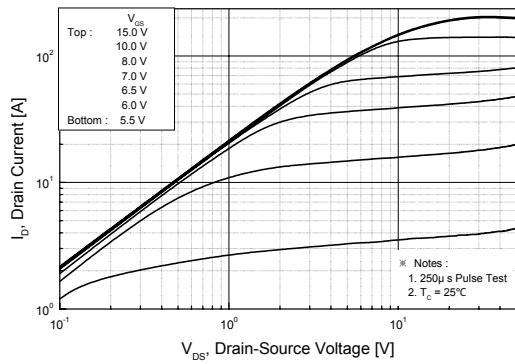


Figure 2. Transfer Characteristics

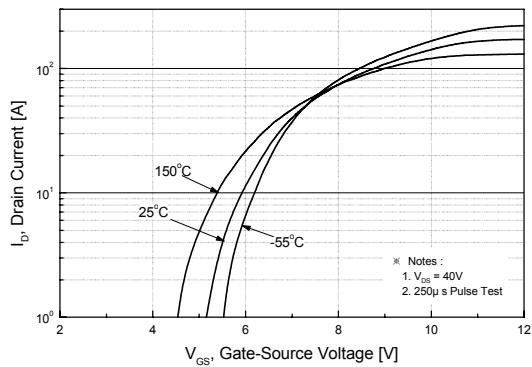


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

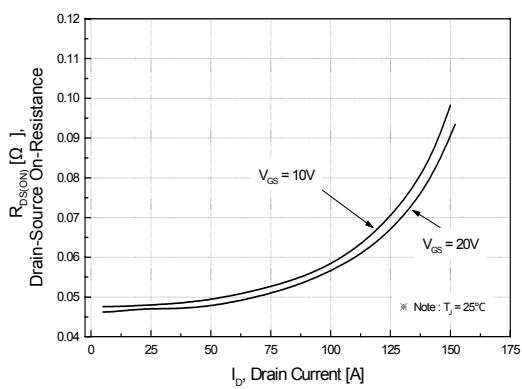


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

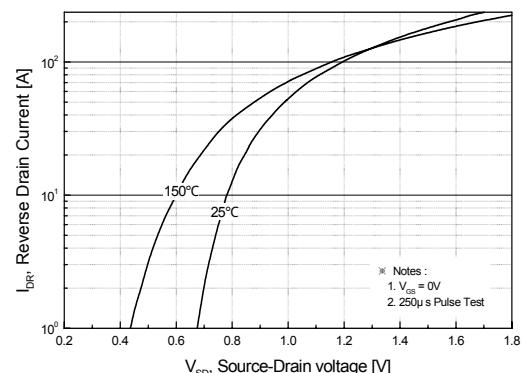


Figure 5. Capacitance Characteristics

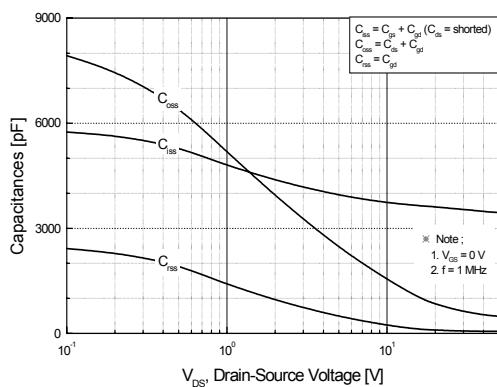
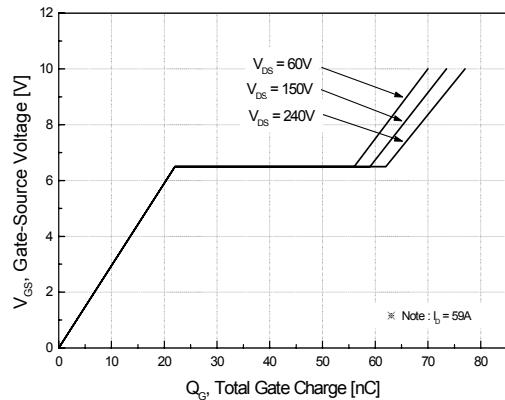


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

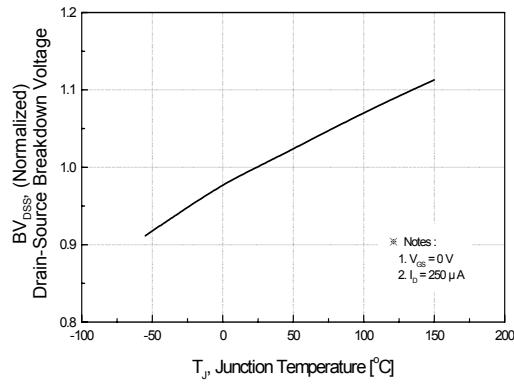


Figure 8. On-Resistance Variation vs. Temperature

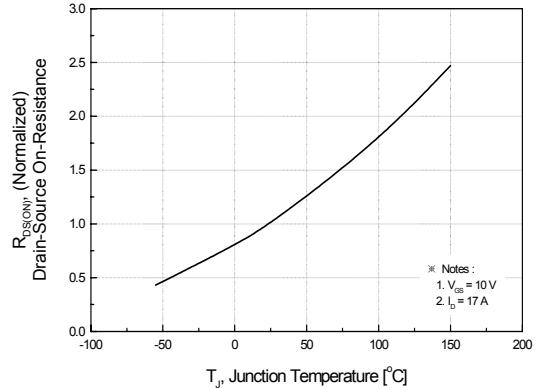


Figure 9. Maximum Safe Operating Area

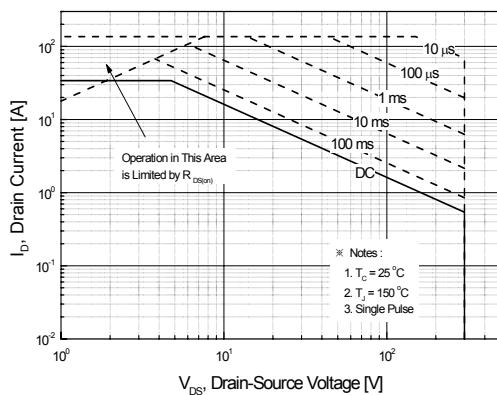


Figure 10. Maximum Drain Current vs. Case Temperature

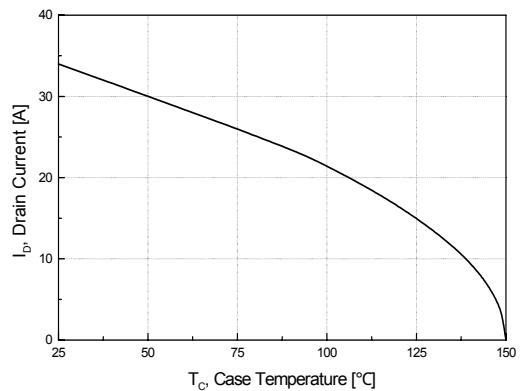
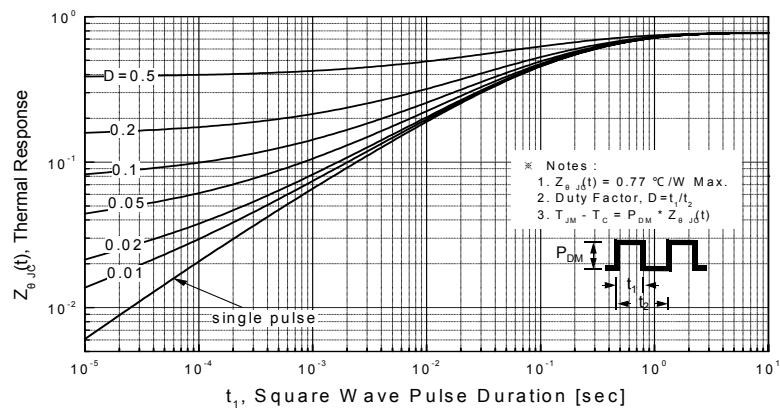
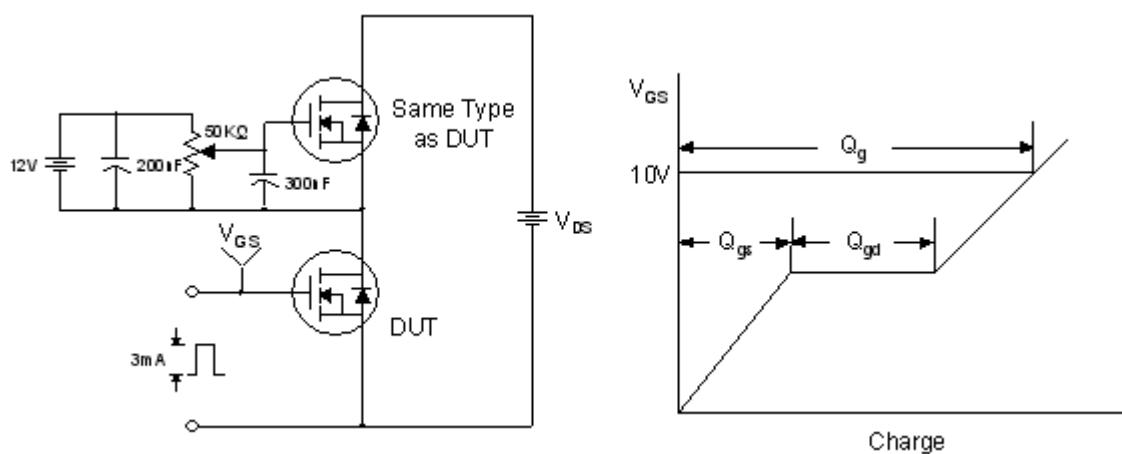


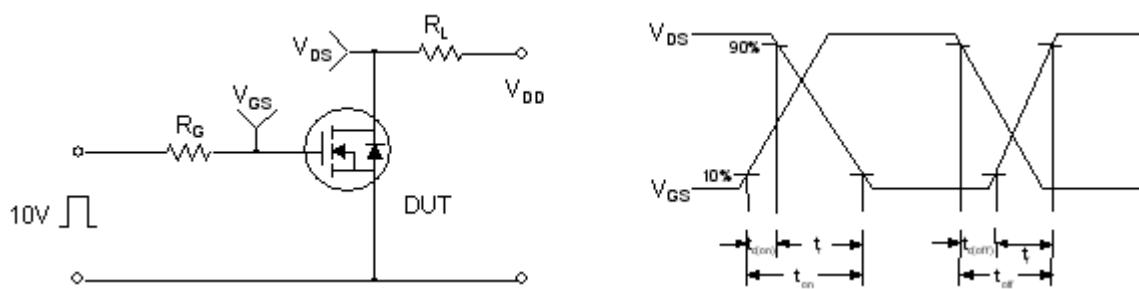
Figure 11. Transient Thermal Response Curve



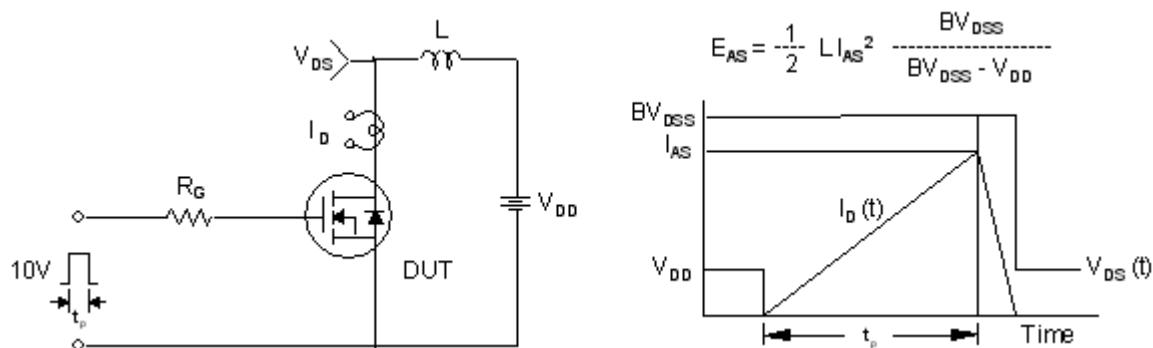
Gate Charge Test Circuit & Waveform



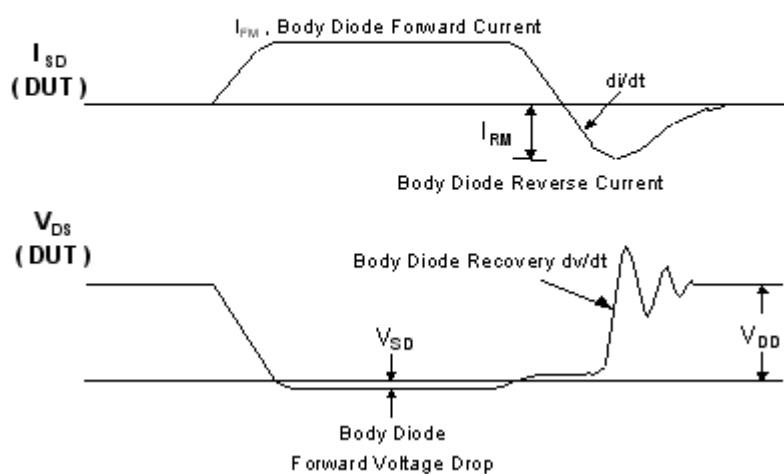
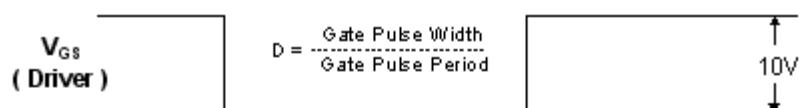
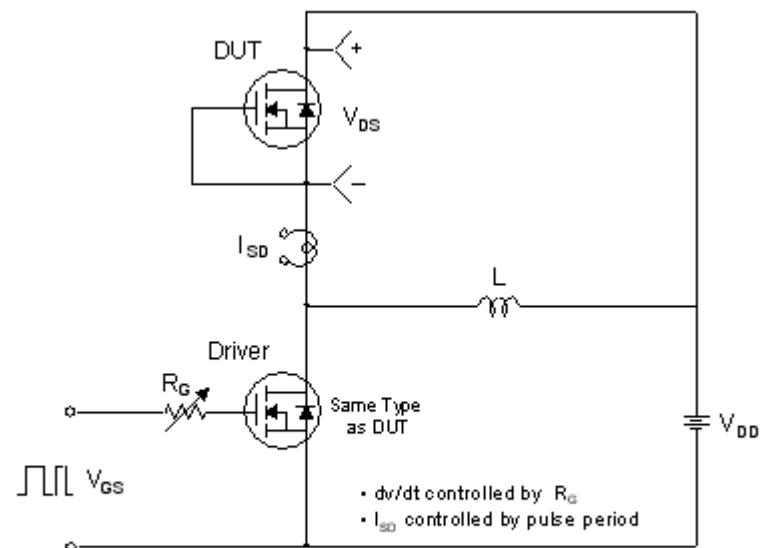
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

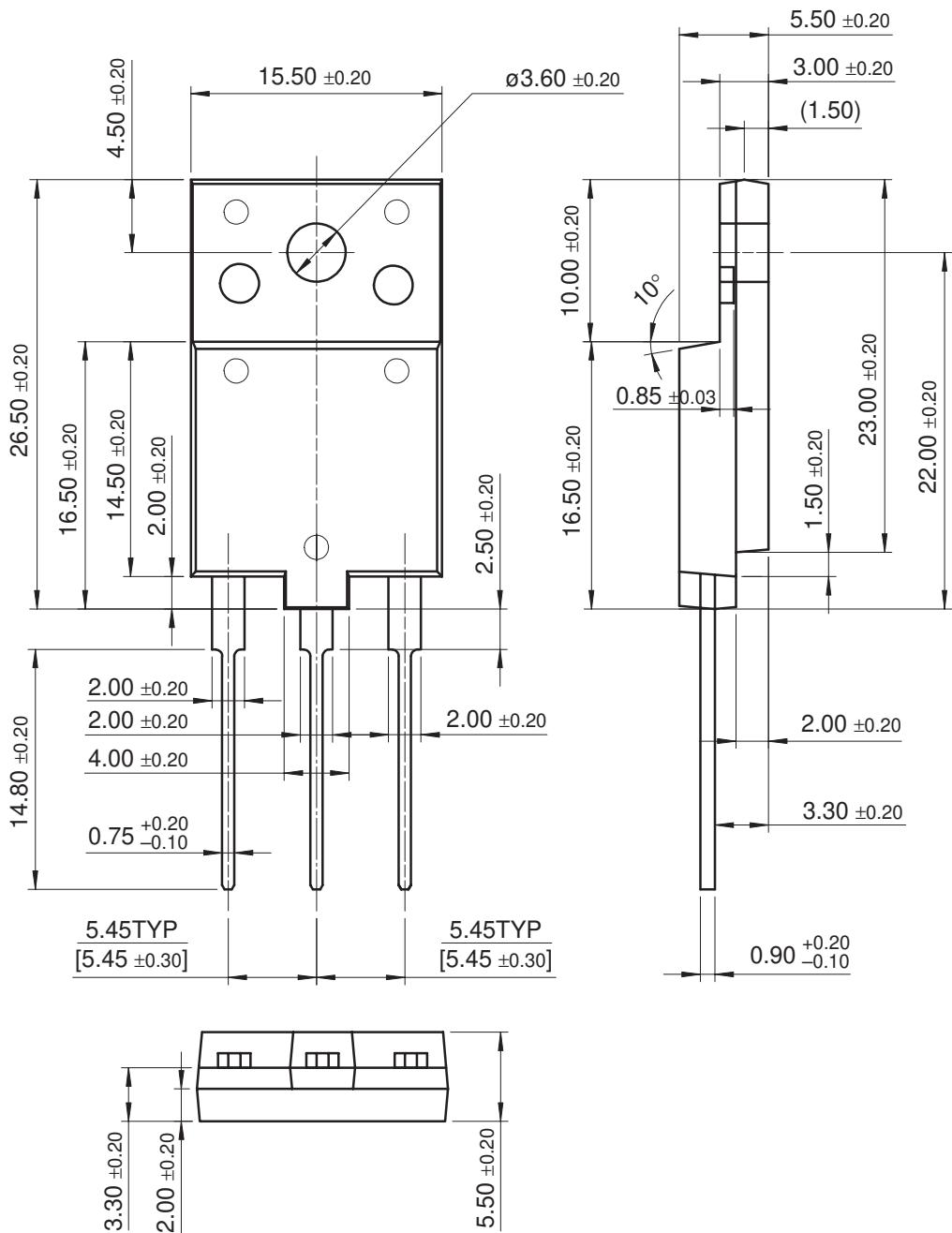


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-3PF



Dimensions in Millimeters

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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