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Super I/O Controller with ACPI Support, Real Time Clock and Consumer IR

FEATURES

- 5 Volt Operation
- PC98/99 and ACPI 1.0 Compliant
- Battery Back-up for Wake-Events
- ISA Plug-and-Play Compatible Register Set
  - 12 IRQ Options
  - 15 Serial IRQ Options
  - 16 Bit Address Qualification
  - Four DMA Options
  - 12mA AT Bus Drivers
- BIOS Buffer
- 20 GPI/O Pins
- 32KHz Standby Clock Output
- Soft Power Management
- ACPI/PME Support
- SCI/SMI Support
  - Watchdog timer
  - Power Button Override Event
  - Either Edge Triggered Interrupts
- Intelligent Auto Power Management
  - Shadowed Write-only Registers
  - Programmable Wake-up Event Interface
- 8042 Keyboard Controller
  - 2K Program ROM
  - 256 Bytes Data RAM
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Timer/Counter
  - Port 92 Support
  - Fast Gate A20 and Hardware Keyboard Reset
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  - Day of Month Alarm, Century Byte
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  - 128 Bytes of CMOS RAM Lockable in 4x32 Byte Blocks
  - 12 and 24 Hour Time Format
  - Binary and BCD Format
  - 5μA Standby Battery Current (max)[1]
- 2.88MB Super I/O Floppy Disk Controller
  - Relocatable to 480 Different Addresses
  - Licensed CMOS 765B Floppy Disk Controller
  - Advanced Digital Data Separator
  - SMSC's Proprietary 82077AA Compatible Core
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - Supports Two Floppy Drives Directly
  - Software Write Protect
  - FDC on Parallel Port
  - Low Power CMOS Design
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  - Low Cost Implementation
  - No Filter Components Required
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  - Relocatable to 480 Different Addresses
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - Programmable Baud Rate Generator
  - Modem Control Circuitry Including 230K and 460K Baud
  - IrDA 1.0, Consumer IR, HP-SIR, ASK-IR Support
  - Ring Wake Filter
- Multi-Mode Parallel Port with ChiProtect
  - Relocatable to 480 Different Addresses
  - Standard Mode
  - IBM PC/XT, PC/AT, and PS/2 Compatible Bidirectional ParallelPort
  - Enhanced Mode
  - Enhanced Parallel Port (EPP) Compatible
  - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - High Speed Mode
  - Microsoft and Hewlett Packard
  - Extended Capabilities Port (ECP) Compatible (IEEE 1284 Compliant)
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 14 mA Output Drivers
- 128 Pin QFP package, lead-free RoHS compliant package also available

Note 1: Please contact SMSC for the latest value.

ORDERING INFORMATION

Order Numbers:

FDC37B787QFP for 128 pin QFP package

FDC37B787-NS for 128 pin QFP lead-free RoHS compliant package

TABLE OF CONTENTS

GENERAL DESCRIPTION

The FDC37B78x with advanced Consumer IR and IrDA v1.0 support incorporates a keyboard interface, real-time clock, SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP support, on-chip 12 mA AT bus drivers, and two floppy direct drive support, soft power management and SMI support and Intelligent Power Management including PME and SCI/ACPI support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550. The parallel port, the IDE interface, and the game port select logic are compatible with IBM PC/AT architecture, as well as EPP and ECP. The FDC37B78x incorporates sophisticated power control circuitry (PCC) which includes support for keyboard, mouse, modem ring, power button support and consumer infrared wake-up events. The PCC supports multiple low power down modes.

The FDC37B78x provides features for compliance with the “Advanced Configuration and Power Interface Specification” (ACPI).
These features include support of both legacy and ACPI power management models through the selection of SMI or SCI. It implements a power button override event (4 second button hold to turn off the system) and either edge triggered interrupts.

The FDC37B78x provides support for the ISA Plug-and-Play Standard (Version 1.0a) and provides for the recommended functionality to support Windows '95, PC97 and PC98. Through internal configuration registers, each of the FDC37B78x 's logical device's I/O address, DMA channel and IRQ channel may be programmed. There are 480 I/O address location options, 12 IRQ options or Serial IRQ option, and four DMA channel options for each logical device.

The FDC37B78x Floppy Disk Controller and data separator do not require any external filter components and are therefore easy to use, offer lower system cost and reduced board area. The FDC is software and register compatible with SMSC's proprietary 82077AA core.

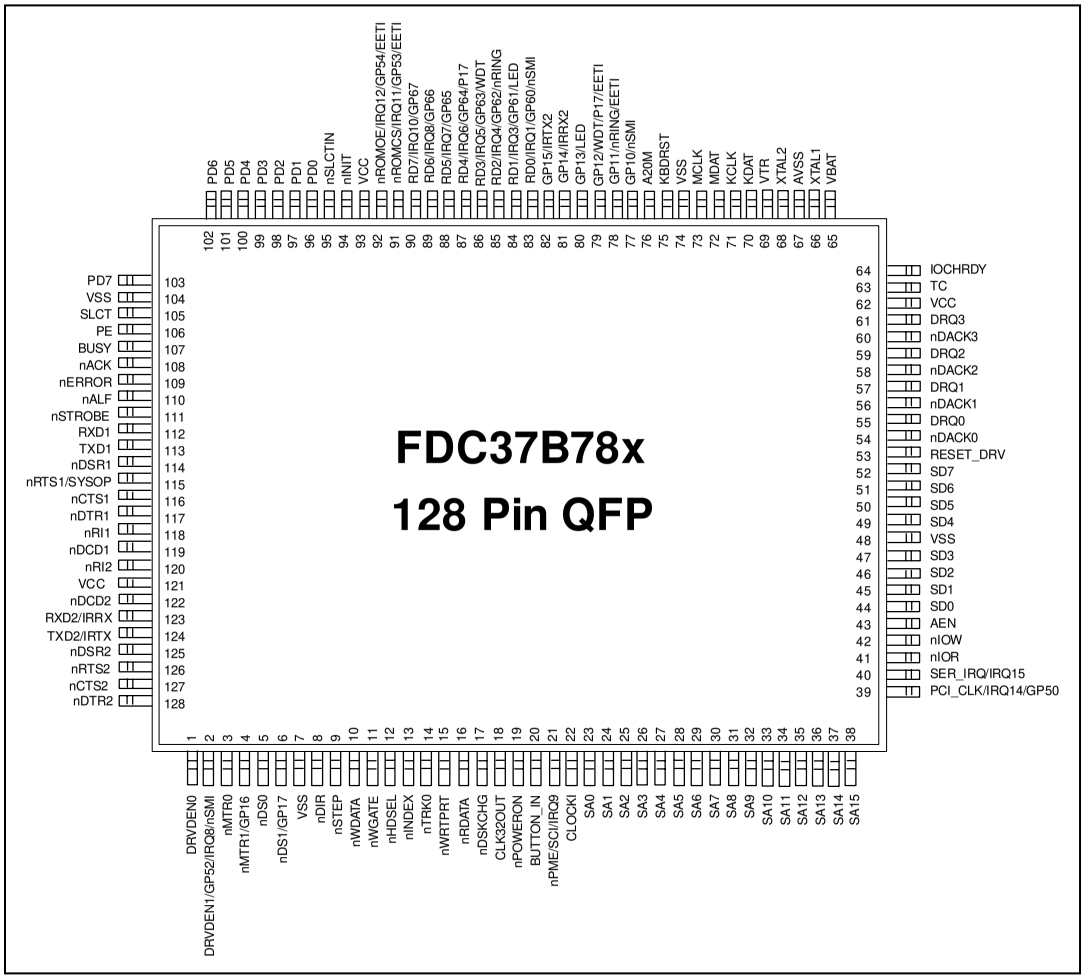

FIGURE 1 - FDC37B78x PIN CONFIGURATION

DESCRIPTION OF PIN FUNCTIONS

PIN No./QFP	NAME	TOTAL	SYMBOL	BUFFER TYPE
PROCESSOR/HOST INTERFACE (40)				
44-47, 49-52	System Data Bus	8	SD[0:7]	IO12
23-38	16-bit System Address Bus	16	SA[0:15]	I
43	Address Enable	1	AEN	I
64	I/O Channel Ready	1	IOCHRDY	OD12
53	ISA Reset Drive	1	RESET_DRV	IS
40	Serial IRQ/IRQ15	1	SER_IRQ	IO12
39	PCI Clock/IRQ14/GP50	1	PCI_CLK	IO12
55	DMA Request 0	1	DRQ0	O12
57	DMA Request 1	1	DRQ1	O12
59	DMA Request 2	1	DRQ2	O12
61	DMA Request 3	1	DRQ3	O12
54	DMA Acknowledge 0	1	nDACK0	I
56	DMA Acknowledge 1	1	nDACK1	I
58	DMA Acknowledge 2	1	nDACK2	I
60	DMA Acknowledge 3	1	nDACK3	I
63	Terminal Count	1	TC	I
41	I/O Read	1	nIOR	I
42	I/O Write	1	nIOW	I
CLOCKS (4)				
22	14.318MHz Clock Input	1	CLOCKI	I
66	32.768kHz Crystal Input	1	XTAL1	ICLK
68	32.768kHz Crystal Driver	1	XTAL2	OCLK
18	32.768kHz Clock Out	1	CLK32OUT	O8
POWER PINS (10)				
62, 93, 121	+5V Supply Voltage	3	VCC	

PIN No./QFP	NAME	TOTAL	SYMBOL	BUFFER TYPE
7, 48, 74, 104	Digital Ground	4	VSS	
67	Analog Ground	1	AVSS	
69	Trickle Supply Voltage	1	VTR	
65	Battery Voltage	1	VBAT	
POWER MANAGEMENT (3)				
19	Power On	1	nPOWERON	OD24
20	Button In	1	BUTTON_IN	I
21	Power Management Event/SCI/IRQ9	1	nPME	O12
FDD INTERFACE (16)				
16	Read Disk Data	1	nRDATA	IS
11	Write Gate	1	nWGATE	O24
10	Write Disk Data	1	nWDATA	O24
12	Head Select	1	nHDSEL	O24
8	Step Direction	1	nDIR	O24
9	Step Pulse	1	nSTEP	O24
17	Disk Change	1	nDSKCHG	IS
5	Drive Select 0	1	nDS0	O24
6	Drive Select 1/GP17	1	nDS1	IO24
3	Motor On 0	1	nMTR0	O24
4	Motor On 1/GP16	1	nMTR1	IO24
15	Write Protected	1	nWRTPRT	IS
14	Track 0	1	nTRKO	IS
13	Index Pulse Input	1	nINDEX	IS
1	Drive Density Select 0	1	DRVDEN0	O24
2	Drive Density Select 1/GP52/IRQ8/nSMI	1	DRVDEN1	IO24
GENERAL PURPOSE I/O (6)				
77	General Purpose 10/nSMI	1	GP10	IO12
78	General Purpose 11/nRING/EETI	1	GP11	IO4

PIN No./QFP	NAME	TOTAL	SYMBOL	BUFFER TYPE
79	General Purpose 12/WDT/P17/EETI	1	GP12	IO4
80	General Purpose 13/LED Driver	1	GP13	IO24
81	General Purpose 14/Infrared Rx	1	GP14	IO4
82	General Purpose 15/Infrared Tx (Note 3)	1	GP15	IO24
BIOS INTERFACE (10)				
83	ROM Bus 0/IRQ1/GP60/nSMI	1	RD0	IO12
84	ROM Bus 1/IRQ3/GP61/LED	1	RD1	IO24
85	ROM Bus 2/IRQ4/GP62/nRING	1	RD2	IO12
86	ROM Bus 3/IRQ5/GP63/WDT	1	RD3	IO12
87	ROM Bus 4/IRQ6/GP64/P17	1	RD4	IO12
88	ROM Bus 5/IRQ7/GP65	1	RD5	IO12
89	ROM Bus 6/IRQ8/GP66	1	RD6	IO12
90	ROM Bus 7/IRQ10/GP67	1	RD7	IO12
91	nROMCS/IRQ11/GP53/EETI	1	nROMCS	IO12
92	nROMOE/IRQ12/GP54/EETI	1	nROMOE	IO12
SERIAL PORT 1 INTERFACE (8)				
112	Receive Serial Data 1	1	RXD1	I
113	Transmit Serial Data 1	1	TXD1	O4
115	Request to Send 1	1	nRTS1/ SYSOP	IO4
116	Clear to Send 1	1	nCTS1	I
117	Data Terminal Ready 1	1	nDTR1	O4
114	Data Set Ready 1	1	nDSR1	I
119	Data Carrier Detect 1	1	nDCD1	I
118	Ring Indicator 1	1	nRI1	I
SERIAL PORT 2 INTERFACE (8)				
123	Receive Serial Data 2/Infrared Rx	1	RXD2/IRRX	I
124	Transmit Serial Data 2/Infrared Tx (Note 3)	1	TXD2/IRTX	O24
126	Request to Send 2	1	nRTS2	O4

PIN No./QFP	NAME	TOTAL	SYMBOL	BUFFER TYPE
127	Clear to Send 2	1	nCTS2	I
128	Data Terminal Ready	1	nDTR2	O4
125	Data Set Ready 2	1	nDSR2	I
122	Data Carrier Detect 2	1	nDCD2	I
120	Ring Indicator 2	1	nRI2	I
PARALLEL PORT INTERFACE (17)				
96-103	Parallel Port Data Bus	8	PD[0:7]	IOP14
95	Printer Select	1	nSLCTIN	OP14
94	Initiate Output	1	nINIT	OP14
110	Auto Line Feed	1	nALF	OP14
111	Strobe Signal	1	nSTROBE	OP14
107	Busy Signal	1	BUSY	I
108	Acknowledge Handshake	1	nACK	I
106	Paper End	1	PE	I
105	Printer Selected	1	SLCT	I
109	Error at Printer	1	nERROR	I
KEYBOARD/MOUSE INTERFACE (6)				
70	Keyboard Data	1	KDAT	IOD16
71	Keyboard Clock	1	KCLK	IOD16
72	Mouse Data	1	MDAT	IOD16
73	Mouse Clock	1	MCLK	IOD16
75	Keyboard Reset	1	KBDRST (Note 2)	O4
76	Gate A20	1	A20M	O4

Note 1 The “n” as the first letter of a signal name indicates an “Active Low” signal.
Note 2 KBDRST is active low.
Note 3 This pin defaults to an output and low.

BUFFER TYPE DESCRIPTIONS

TABLE 1 - BUFFER TYPES

SYMBOL	DESCRIPTION
I	Input, TTL compatible.
IS	Input with Schmitt trigger.
ICLK	RTC 32.768 kHz crystal input.
OCLK	RTC 32.768 kHz crystal output.
IO4	Input/Output, 4mA sink, 2mA source.
O4	Output, 4mA sink, 2mA source.
O8	Output, 8mA sink, 4mA source.
IO12	Input/Output, 12mA sink, 6mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Output, Open Drain, 12 mA sink.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive Protected.
OD14	Output, Open Drain, 14mA sink.
OP14	Output, 14mA sink, 14mA source. Backdrive Protected.
IOD16	Input/Output, Open Drain, 16mA sink
O24	Output, 24mA sink, 12mA source.
OD24	Output, Open Drain, 24mA sink.
IO24	Input/Output, 24mA sink, 12mA source.

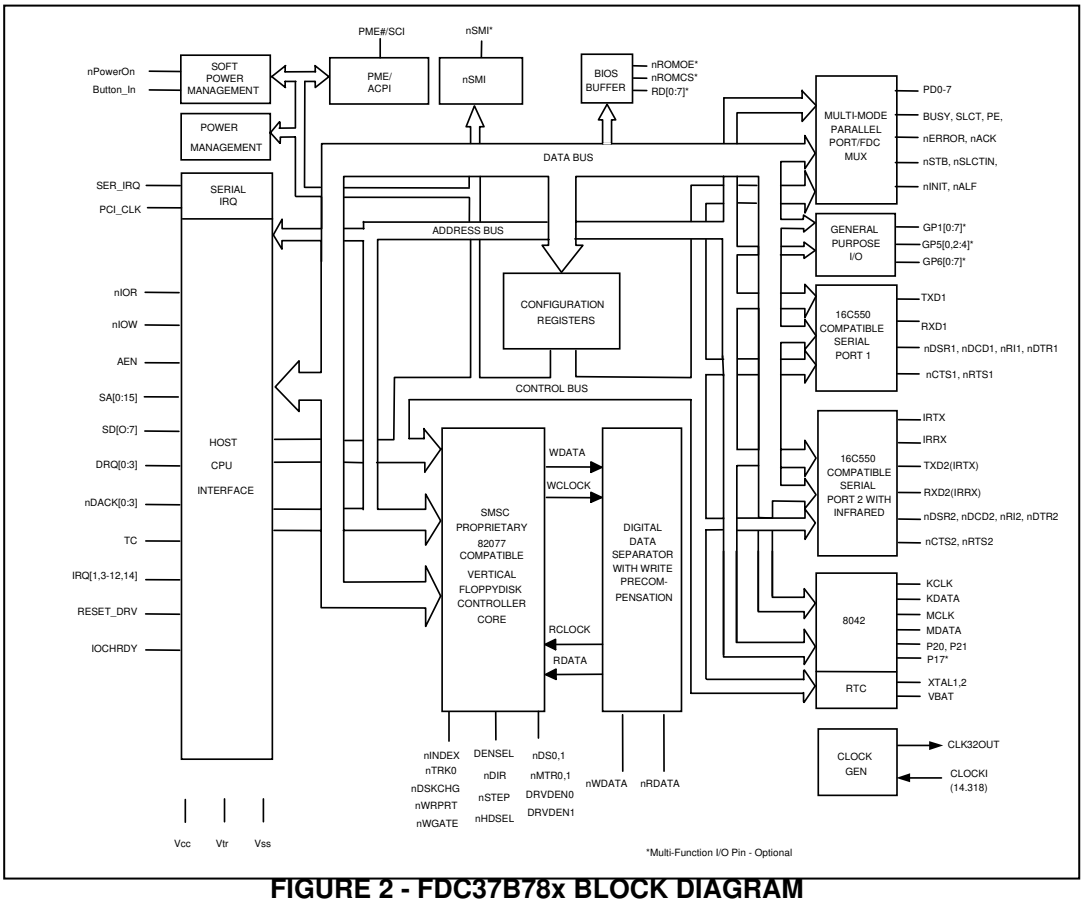

FIGURE 2 - FDC37B78x BLOCK DIAGRAM

GENERAL PURPOSE I/O PINS

TABLE 2 - GENERAL PURPOSE I/O PIN FUNCTIONS

PIN NO. QFP	DEFAULT FUNCT	ALT FUNCT 1	ALT FUNCT 2	ALT FUNCT 3	BUFFER TYPE	INDEX REGISTER	GPIO
77	GPIO	nSMI	-	-	IO12	GP1	GP10
78	GPIO	nRING	EETI[1]	-	IO4	GP1	GP11
79	GPIO	WDT	P17	EETI[1]	IO4	GP1	GP12
80	GPIO	LED	-	-	IO24	GP1	GP13
81	GPIO	IRRX2	-	-	IO4	GP1	GP14
82	GPIO	IRTX2	-	-	IO24	GP1	GP15
4	nMTR1	GPIO	-	-	IO24	GP1	GP16
6	nDS1	GPIO	-	-	IO24	GP1	GP17
39	PCI_CLK	IRQ14	GPIO	-	IO12	GP5	GP50
2	DRVDEN1	GPIO	IRQ8	nSMI	IO24	GP5	GP52
91	nROMCS[2]	IRQ11	GPIO	EETI[1]	IO12	GP5	GP53
92	nROMOE[2]	IRQ12	GPIO	EETI[1]	IO12	GP5	GP54
83	RD0[2,3]	IRQ1	GPIO	nSMI	IO12	GP6	GP60
84	RD1[2,3]	IRQ3	GPIO	LED	IO24	GP6	GP61
85	RD2[2,3]	IRQ4	GPIO	nRING	IO12	GP6	GP62
86	RD3[2,3]	IRQ5	GPIO	WDT	IO12	GP6	GP63
87	RD4[2,3]	IRQ6	GPIO	P17	IO12	GP6	GP64
88	RD5[2,3]	IRQ7	GPIO	-	IO12	GP6	GP65
89	RD6[2,3]	IRQ8	GPIO	-	IO12	GP6	GP66
90	RD7[2,3]	IRQ10	GPIO	-	IO12	GP6	GP67

Note 1 Either Edge Triggered Interrupt Inputs.

Note 2 At power-up, RD0-7, nROMCS and nROMOE function as the XD Bus. To use RD0-7 for alternate functions, nROMCS must stay high until those pins are finished being programmed.

Note 3 These pins cannot be programmed as open drain pins in their original function.

REFERENCE DOCUMENTS

- SMSC Consumer Infrared Communications Controller (CIrCC) V1.X
- IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993.
- Hardware Description of the 8042, Intel 8 bit Embedded Controller Handbook.
- PCI Bus Power Management Interface Specification, Rev. 1.0, Draft, March 18, 1997.

FUNCTIONAL DESCRIPTION

SUPER I/O REGISTERS

The address map, shown below in Table 4, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, serial and parallel ports can be moved via the configuration registers. Some addresses are used to access more than one register.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37B78x through a series of read/write registers. The port addresses for these registers are shown in Table 4. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide. All host interface output buffers are capable of sinking a minimum of 12 mA.

TABLE 3 - SUPER I/O BLOCK ADDRESSES

ADDRESS	BLOCK NAME	LOGICAL DEVICE	NOTES
Base+(0-5) and +(7)	Floppy Disk	0	
 Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	3	
Base+(0-7)	Serial Port Com 1	4	
Base1+(0-7) Base2+(0-7)	Serial Port Com 2	5	IR Support Consumer IR
70,71, Base, Base+(1)	RTC	6	
60, 64	KYBD	7	
Base + (0-17h)	ACPI, PME, SMI	A	
Base + (0-1)	Configuration		

Note 1: Refer to the configuration register descriptions for setting the base address.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

FDC INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers that facilitate the interfacing between the host microprocessor and the disk drive. TABLE 4 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

TABLE 4 - STATUS, DATA AND CONTROL REGISTERS

(Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TSR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

STATUS REGISTER A (SRA)

Address 3F0 READ ONLY
This register is read-only and monitors the state of the FINTR pin and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION
Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected. (See also Force Write Protect Function)

BIT 2 nINDEX
Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2
Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed. Note: **This function is not supported in this chip. (Always 1, indicating 1 drive)**

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected. (See also Force Write Protect Function)

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DRQ output pin.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

STATUS REGISTER B (SRB)

Address 3F1 READ ONLY
This register is read-only and monitors the state of several disk interface pins in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE
Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE
Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE
Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED
Always read as a logic "1".

BIT 7 RESERVED
Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2
The DS2 disk interface is not supported. (Always 1)

BIT 1 nDRIVE SELECT 3
The DS3 disk interface is not supported. (Always 1)

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0
Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1
Active low status of the DS1 disk interface output.

BIT 7 nDRV2
Active low status of the DRV2 disk interface input, this is not supported. (Always 1)

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE
The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET
A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN
PC/AT and Model 30 Mode:
Writing this bit to logic "1" will enable the DRQ, nDACK, TC and FINTR outputs. This bit being a logic "0" will disable the nDACK and TC inputs, and hold the DRQ and FINTR outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.
PS/2 Mode: In this mode the DRQ, nDACK, TC and FINTR pins are always enabled. During a reset, the DRQ, nDACK, TC, and FINTR pins will remain enabled, but this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0
This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1
This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2
The MTR2 disk interface output is not. (Always 0)

BIT 7 MOTOR ENABLE 3
The MTR3 disk interface output is not. (Always 0)

Table 6 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

TABLE 7 - TAPE SELECT BITS

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR

Tape Select bits TDR.[1:0] determine the tape drive number. TABLE 7 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

TABLE 8 - INTERNAL 2 DRIVE DECODE - NORMAL

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	1	0	nBIT 5	nBIT 4
X	X	1	X	0	1	0	1	nBIT 5	nBIT 4
X	1	X	X	1	0	1	1	nBIT 5	nBIT 4
1	X	X	X	1	1	1	1	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	nBIT 5	nBIT 4

TABLE 9 - INTERNAL 2 DRIVE DECODE - DRIVES 0 AND 1 SWAPPED

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	nBIT 4	nBIT 5
X	X	1	X	0	1	1	0	nBIT 4	nBIT 5
X	1	X	X	1	0	1	1	nBIT 4	nBIT 5
1	X	X	X	1	1	1	1	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	nBIT 4	nBIT 5

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are a high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

TABLE 10 - DRIVE TYPE ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 - B1	L0-CRF2 - B0
0	1	L0-CRF2 - B3	L0-CRF2 - B2
1	0	L0-CRF2 - B5	L0-CRF2 - B4
1	1	L0-CRF2 - B7	L0-CRF2 - B6

Note:L0-CRF2-Bx = Logical Device 0, Configuration Register F2, Bit x.

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 11 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT
These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 10 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. this starting track number can be changed by the configure command.

BIT 5 UNDEFINED
Should be written as a logic "0".

BIT 6 LOW POWER
A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET
This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Note: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, LD8:CRC2[7:0]. separator circuits will be turned off. The controller will come out of manual low power.