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SUCCESS BY DESIGN

# FDC37C665GT
# FDC37C666GT

# High-Performance Multi-Mode™ Parallel Port Super I/O Floppy Disk Controllers

## FEATURES

- 5 Volt Operation
- Floppy Disk Available on Parallel Port Pins
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible to the 82077AA Using SMSC's Proprietary Floppy Disk Controller Core
  - Supports Vertical Recording Format
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - 48 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA Option
  - FDC Primary/Secondary Address Selection
  - 16 Byte Data FIFO
  - Low Power CMOS 0.8µ Design
- Enhanced Digital Data Separator
  - Low Cost Implementation - 24 MHz Crystal
  - No Filter Components Required
  - Ease of Test and Use, Lower System Cost, and Reduced Board Area
  - 1 Mb/s, 500 Kb/s, 300 Kb/s, 250 Kb/s Data Rates
  - Supports Floppy Disk and Tape Drives
  - Programmable Precompensation Modes
- Multi-Mode Parallel Port with ChiProtect™ Circuitry
  - Standard Mode
    - IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bidirectional Parallel Port
  - Enhanced Mode
    - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - High Speed Mode
    - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) IEEE 1284 Compliant
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - Provides Backdrive Current Protection
  - 24 mA Output Drivers
  - Two Parallel Port Interrupt Pins
- Serial Ports
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - MIDI Compatible
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- ISA Host Interface
- IDE Interface
  - On-Chip Decode and Select Logic Compatible with IBM PC/XT and PC/AT Embedded Hard Disk Drives
  - IDE Primary/Secondary Address Selection

- Supports Four Floppy Drives Directly (Standard and Enhanced Modes)
- General Purpose 11 Bit Address Decoder
- Game Port Select Logic (FDC37C666GT Only)
- 100 Pin QFP Package

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## GENERAL DESCRIPTION

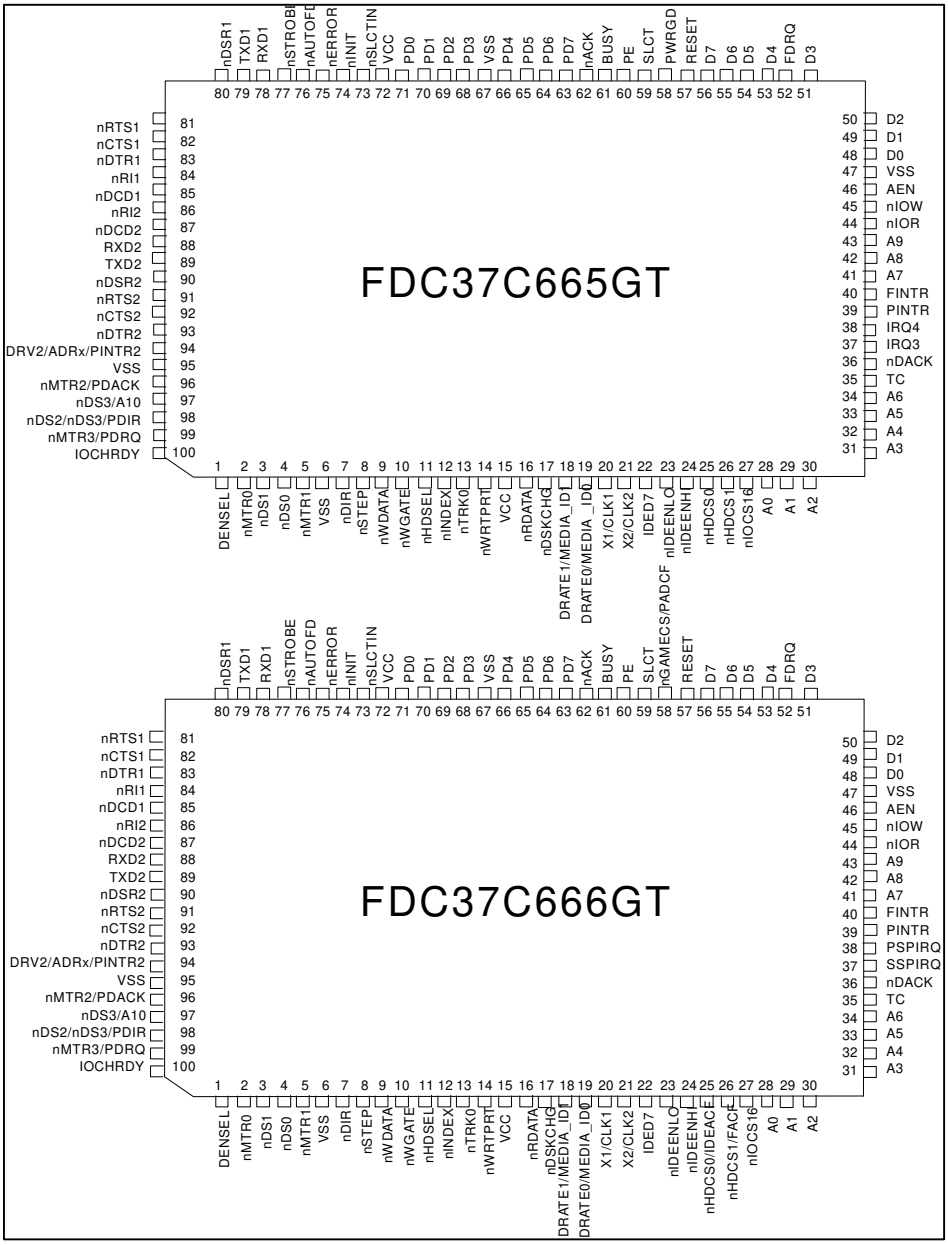
The SMSC FDC37C665GT and FDC37C666GT Advanced High Performance Multi-Mode Parallel Port Super I/O Floppy Disk Controller ICs utilize SMSC's proven SuperCell technology for increased product reliability and functionality. The FDC37C665GT is optimized for motherboard applications while the FDC37C666GT is oriented towards controller card applications. Both devices support 1 Mb/s data rates for vertical recording operation. The FDC37C665GT is hardware compatible with the FDC37C651 and FDC37C661 in the Standard and Enhanced Parallel Port Modes.

The FDC37C665GT and FDC37C666GT incorporate SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP support, IDE interface, on-chip 24 mA AT bus drivers, game port chip select (FDC37C666GT only), general purpose address decoder and four floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550. The parallel port, the IDE interface and the game port select logic are compatible with IBM PC/XT and PC/AT architectures, as well as EPP and ECP. The FDC37C665GT and FDC37C666GT incorporate sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C665GT Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. Use of the SCL feature allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs. The parallel port ChiProtect prevents damage caused by the printer being powered when the FDC37C665GT or FDC37C666GT is not powered. The parallel port backdrive current protection prevents the FDC37C665GT or FDC37C666GT from sinking current when the device is powered off and the printer is left powered on.

The FDC37C665GT and FDC37C666GT do not require any external filter components and are, therefore, easy to use and offer lower system cost and reduced board area. The FDC37C665GT and FDC37C666GT are software and register compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

## PIN CONFIGURATION



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| **HOST PROCESSOR INTERFACE** | | | | |
| 48-51<br>53-56 | Data Bus 0-7 | D0-D7 | I/O24 | The data bus connection used by the host microprocessor to transmit data to and from the FDC37C665GT. These pins are in a high-impedance state when not in the output mode. |
| 44 | nI/O Read | nIOR | I | This active low signal is issued by the host microprocessor to indicate a read operation. |
| 45 | nI/O Write | nIOW | I | This active low signal is issued by the host microprocessor to indicate a write operation. |
| 46 | Address Enable | AEN | I | Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes. |
| 28-34<br>41-43 | I/O Address | A0-A9 | I | These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW. |
| 52 | FDC DMA Request | FDRQ | O24 | This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode). |
| 36 | nDMA Acknowle-dge | nDACK | I | An active low input acknowledging the request for a DMA transfer of data. This input enables the DMA read or write internally. |
| 35 | Terminal Count | TC | I | This signal indicates to the FDC37C665GT that data transfer is complete. TC is only accepted when nDACK or nPDACK is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 38 | Serial Port Interrupt Request | IRQ4 | O24 | FDC37C665GT (Motherboard application): IRQ4 is the interrupt from the Primary Serial Port (PSP) or Secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM1 or COM3 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. |
| | Primary Serial Port Interrupt | PSPIRQ | O24 | FDC37C666GT (Adapter application): PSPIRQ is a source of PSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers. |
| 37 | Serial Port Interrupt Request | IRQ3 | O24 | FDC37C665GT (Motherboard application): IRQ3 is the interrupt from the Primary Serial Port (PSP) or secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM2 or COM4 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. |
| | Secondary Serial Port Interrupt | SSPIRQ | O24 | FDC37C666GT (Adapter application): SSPIRQ is a source of SSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers. |
| 40 | Floppy Controller Interrupt Request | FINTR | O24 | This interrupt from the Floppy Disk Controller is enabled/disabled via bit 3 of the Digital Output Register (DOR). |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 39 | Parallel Port Interrupt Request 1 | PINTR1 | O24<br><br><br><br><br>OD24 | This interrupt from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. Refer to configuration registers CR1 and CR3 for more information.<br><br>If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts. |
| 57 | Reset | RST | IS | This active high signal resets the FDC37C665GT and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset. In the FDC37C666GT, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge. |
| **FLOPPY DISK INTERFACE** | | | | |
| 16 | nRead Disk Data | nRDATA | IS | Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data. |
| 10 | nWrite Gate | nWGATE | OD48 | This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette. |
| 9 | nWrite Data | nWDATA | OD48 | This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media. |
| 11 | nHead Select | nHDSEL | OD48 | This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 7 | nDirection Control | nDIR | OD48 | This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion. |
| 8 | nStep Pulse | nSTEP | OD48 | This active low high current driver issues a low pulse for each track-to-track movement of the head. |
| 17 | nDisk Change | nDSKCHG | IS | This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H. |
| 4,3 | nDrive Select O,1 | nDS0,1 | OD48 | Active low open drain outputs select drives 0-1. Refer to Note 2. |
| 98 | nDrive Select 2 | nDS2 | OD48 | Active low open drain output selects drives 2. Refer to Note 2. |
| | nDrive Select 3 | nDS3 | OD48 | In non-ECP mode: Active low open drain output selects drive 3. Refer to Note 2. |
| | PDIR | PDIR | O4 | This bit is used to indicate the direction of the Parallel Port data bus. 0 = output/write 1 = input/read |
| 97 | nDrive Select 3 | nDS3 | 0D48 | In non-ECP mode: Active low open drain output selects drive 3. Refer to Note 2. |
| | I/O Address 10 | A10 | I | In ECP Mode, this pin is the A10 address input. |
| 2,5 | nMotor On 0,1 | nMTR0,1 | OD48 | These active low open drain outputs select motor drives 0-1. Refer to Note 1. |
| 96 | nMotor On 2 | nMTR2 | OD48 | Motor On 2: Refer to Note 1. |
| | | nPDACK | I | In ECP Mode, nMTR2 is the Parallel Port DMA Acknowledge input. Active Low. |
| 99 | nMotor On 3 | nMTR3 | OD48 | Motor On 3: Refer to Note 1. |
| | | PDRQ | O24 | In ECP Mode, MTR3 is the Parallel Port DMA Request output. Active High. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | Density Select | DENSEL | OD48 | Indicates whether a low (250/300 Kb/s) or high (500 Kb/s) data rate has been selected. This is determined by the IDENT bit in Configuration Register 3. |
| 14 | nWrite Protected | nWRTPRT | IS | This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored. |
| 13 | nTrack 00 | nTR0 | IS | This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track. |
| 12 | nIndex | nINDEX | IS | This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole. |
| 19,18 | Data Rate 0, Data Rate 1 | DRATE0, DRATE1 | O24 | These two outputs reflect bits 0 and 1 respectively of the Data Rate Register. At power on, these two outputs are in a high impedance state (refer to Table 50). |
| 19,18 | Media ID0, Media ID1 | | I | In Floppy Enhanced Mode 2 - These bits are the Media ID 0,1 inputs. The value of these bits can be read as bits 6 and 7 of the Floppy Tape register. |
| **SERIAL PORT INTERFACE** | | | | |
| 78,88 | Receive Data | RXD1, RXD2 | I | Receiver serial data input. |
| 79 | Transmit Data | TXD1 | O4 | Transmitter serial data output from Primary Serial Port. |
| | | PCF0 | I | FDC37C666GT (Adapter Mode): Parallel Port Configuration Control 0. During reset active this input is read and latched to define the address of the Parallel Port. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 81 | nRequest to Send | nRTS1 | O4 | Active low Request to Send output for Primary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). Forced inactive during loop mode operation. |
| | Parallel Port Configuration Control | PCF1 | I | FDC37C666GT (Adapter Mode): Parallel Port Configuration Control 1. During reset active this input is read and latched to define the address of the Parallel Port. |
| 91 | nRequest to Send | nRTS2 | O4 | Active low Request to Send output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). Forced inactive during loop mode operation. |
| | Secondary Serial Port Configuration Control | S2CF0 | I | FDC37C666GT (Adapter Mode): Secondary Serial Port Configuration Control 0. During Reset active this input is read and latched to define the address of the Secondary Serial Port. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 83 | nData Terminal Ready | nDTR1 | O4 | Active low Data Terminal Ready output for primary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). Forced inactive during loop mode operation. |
| | IDE Configuration Control | IDECF | I | FDC37C666GT (Adapter Mode): IDE Configuration Control. During reset active this input is read and latched to enable/disable the IDE. |
| 93 | nData Terminal Ready | nDTR2 | O4 | Active low Data Terminal Ready output for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR), The hardware reset will reset the nDTR signal to inactive mode (high). Forced inactive during loop mode operation. |
| | Secondary Serial Port Configuration Control 1 | S2CF1 | I | FDC37C666GT (Adapter Mode): Secondary Serial Port Configuration Control 1. During reset active this input is read and latched to define the address of the Secondary Serial Port. |
| 89 | Transmit Data 2 | TXD2 | O4 | Transmitter Serial Data output from Secondary Serial Port. |
| | | FDCCF | I | FDC37C666GT (Adapter Mode): Floppy Disk Configuration. This input is read and latched during Reset to enable/disable the Floppy Disk Controller. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 82,92 | nClear to Send | nCTS1, nCTS2 | I | Active low Clear to Send inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of nCTS. |
| 80,90 | nData Set Ready | nDSR1, nDSR2 | I | Active low Data Set Ready inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. Note: Bit 5 of MSR is the complement of nDSR. |
| 85,87 | nData Carrier Detect | nDCD1, nDCD2 | I | Active low Data Carrier Detect inputs for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. Note: Bit 7 of MSR is the complement of nDCD. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 84,86 | nRing Indicator | nRI1, nRI2 | I | Active low Ring Indicator input for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. Note: Bit 6 of MSR is the complement of nRI. |
| 94 | Drive 2 | DRV2 | I | In PS/2 mode, this input indicates whether a second drive is connected; DRV2 should be low if a second drive is connected. This status is reflected in a read of Status Register A. (Only available in FDC37C665GT. This pin must not be driven in the FDC37C666GT) |
| | nADRx | nADRx | O24 | Optional I/O port address decode output. Refer to Configuration registers CR3, CR8 and CR9 for more information. Active low. (Available in FDC37C665GT and FDC37C666GT.) Defaults to tri-state after power-up. This pin has a 30µa internal pull-up. |
| | Parallel Port Interrupt Request 2 | PINTR2 | O24 | This interrupt from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. Refer to configuration registers CR1 and CR3 for more information. |
| | | ECPEN | I | FDC37C666GT (Adapter Mode): Enhanced Parallel Port mode select. Refer to FDC37C666GT hardware configuration for more information. Read and latched during reset active. |
| **PARALLEL PORT INTERFACE** | | | | |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 73 | nPrinter Select Input | nSLCTIN | OD24 | This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. |
| | | | 0P24 | Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 74 | nInitiate Output | nINIT | OD24 | This output is bit 2 of the printer control register. This is used to initiate the printer when low. |
| | | | 0P24 | Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 76 | nAutofeed Output | nAUTOFD | OD24 | This output goes low to cause the printer to automatically feed one line after each line is printed. The nAUTOFD output is the complement of bit 1 of the Printer Control Register. |
| | | | 0P24 | Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 77 | nStrobe Output | nSTROBE | OD24 | An active low pulse on this output is used to strobe the printer data into the printer. The nSTROBE output is the complement of bit 0 of the Printer Control Register. |
| | | | 0P24 | Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 61 | Busy | BUSY | I | This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 62 | nAcknowledge | nACK | I | A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the nACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 60 | Paper End | PE | I | Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 59 | Printer Selected Status | SLCT | I | This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 75 | nError | nERR | I | A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the nERR input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. |
| 71-68<br>66-63 | Port Data | PD0-PD7 | I/OP24 | The bi-directional parallel data bus is used to transfer information between CPU and peripherals. |
| 100 | IOCHRDY | IOCHRDY | OD24P | In EPP mode, this pin is pulled low to extend the read/write command. This pin has an internal pull-up. |
| **IDE** | | | | |
| 23 | nIDE Low Byte Enable | nIDEENLO | O8 | This active low signal is used in both the XT and AT mode. In the AT mode, this pin is active when the IDE is enabled and the I/O address is accessing 1F0H-1F7H and 3F6H-3F7H in primary address mode or 170H-177H and 376H,377H in secondary address mode. In the XT mode, this signal is active for accessing 320H-323H, 8 bit programmed I/O or DMA. |
| | | S1CF1 | I | FDC37C666GT (Adapter Mode): Primary Serial Configuration 1. Read and latched during reset active to select the address of the Secondary Serial Port. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 24 | nIDE High Byte Enable | nIDEENHI | O8 | This signal is active low only in the AT mode, and when IO16CSB is also active. The I/O addresses for which this pin reacts are 1F0H-1F7H in primary address mode or 170H-177H in secondary address mode. This pin is not used in XT mode. |
| | | S1CF0 | I | FDC37C666GT (Adapter Mode): Primary Serial Configuration 0. Read and latched during reset active to define the address of the Secondary Serial Port. |
| 25 | nHard Disk Chip Select | nHDCS0 | O24 | This is the Hard Disk Chip select corresponding to addresses 1F0H-1F7H in primary address mode or 170H-177H in secondary address mode in the AT mode and addresses 320H-323H in the XT mode. |
| | | IDEACF | I | FDC37C666GT (Adapter Mode): IDE Address Control. Refer to FDC37C666GT hardware configuration for more information. Read and latched during reset active. |
| 26 | nHard Disk Chip Select | nHDCS1 | O24 | This is the Hard Disk Chip select corresponding to 3F6H,3F7H for primary address mode or 376H,377H for secondary address mode in the AT mode and addresses 3F6H,3F7H in the XT mode. |
| | | FACF | I | FDC37C666GT (Adapter Mode): Floppy Disk Address Control. Refer to FDC37C666GT hardware configuration for more information. Read and latched during reset active. |
| 27 | nI/O 16 Bit Indicator | nIOCS16 | I | This input indicates, in AT mode only, when 16 bit transfers are to take place. This signal is generated by the hard disk interface. Logic "0" = 16 bit mode; logic "1" = 8 bit mode. |
| | | nHDACK | I | In the XT mode, this is the Hard Disk Controller DMA Acknowledge, low active. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 22 | IDE Data Bit 7 | IDED7 | I/O24 | IDE data bit 7 in the AT mode. IDED7 transfers data at I/O addresses 1F0H-1F7H (R/W), 3F6 (R/W), 3F7(W). IDED7 should be connected to IDE data bit 7. The FDC37C665GT functions as a buffer transferring data bit 7 between the IDE device and the host. During I/O read of 3F7H, IDED7 is the FDC disk change bit. In the XT mode, IDE7 is not used. |
| **MISCELLANEOUS** | | | | |
| 58 | Power Good | PWRGD | I | FDC37C665GT (Motherboard Mode): This input indicates that the power ($V_{CC}$) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all inputs to the FDC37C665GT are disconnected and put in a low power mode, all outputs are put into high impedance. The contents of all registers are preserved as long as $V_{CC}$ has a valid value. The driver current drain in this mode drops to ISTBY - standby current. This input has a weak pullup resistor to $V_{CC}$. |
| | nGame Port Chip Select | nGAMECS | O4 | FDC37C666GT (Adapter Mode): This is the Game Port Chip Select output - active low. It will go active when the I/O address is 201H. |
| | | PADCF | I | FDC37C666GT (Adapter Mode): Parallel Port Mode Control. Refer to FDC37C666GT hardware configuration for more information. Read and latched during reset active. |
| 20 | CLOCK 1 | X1/CLK1 | ICLK | The external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used. |
| 21 | CLOCK 2 | X2/CLK2 | OCLK | 24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | BUFFER TYPE | DESCRIPTION |
|---|---|---|---|---|
| 15,72 | Power | $V_{CC}$ | | + 5 Volt supply pin. |
| 6,47, 67,95 | Ground | GND | | Ground pin. |

Note 1: These active low open drain outputs select motor drives 0-3. In non-ECP modes, four drives can be supported directly. These motor enable bits are controlled by software via the Digital Output Register (DOR). In ECP mode, MTR0,1 can be used to directly support 2 drives or can support 4 drives by using an external 2 to 4 decoder.

Note 2: Active low open drain outputs select drives 0-3. In non-ECP modes, four drives can be supported directly. These drive select outputs are a decode of bits 0 and 1 of the Digital Output Register and qualified by the appropriate Motor Enable Bit of the DOR (bits 4-7). In ECP mode, DS0,1 can be used to directly support 2 drives or can support 4 drives by using an external 2 to 4 decoder.

## BUFFER TYPE DESCRIPTIONS

| BUFFER TYPE | DESCRIPTION |
|---|---|
| I/O24 | Input/output. 24 mA sink; 12 mA source. |
| O24 | Output. 24 mA sink; 12 mA source. |
| OD24 | Output. 24 mA sink. |
| OD24P | Open drain. 24 mA sink; 30 μA source. |
| OP24 | Output. 24 mA sink; 4 mA source. |
| OD48 | Open drain. 48 mA sink. |
| O4 | Output. 4 mA sink; 2.0 mA source. |
| O8 | Output. 8 mA sink; 4.0 mA source. |
| OCLK | Output to external crystal |
| ICLK | Input to Crystal Oscillator Circuit (CMOS levels) |
| I | Input TTL compatible. |
| IS | Input with Schmitt Trigger |

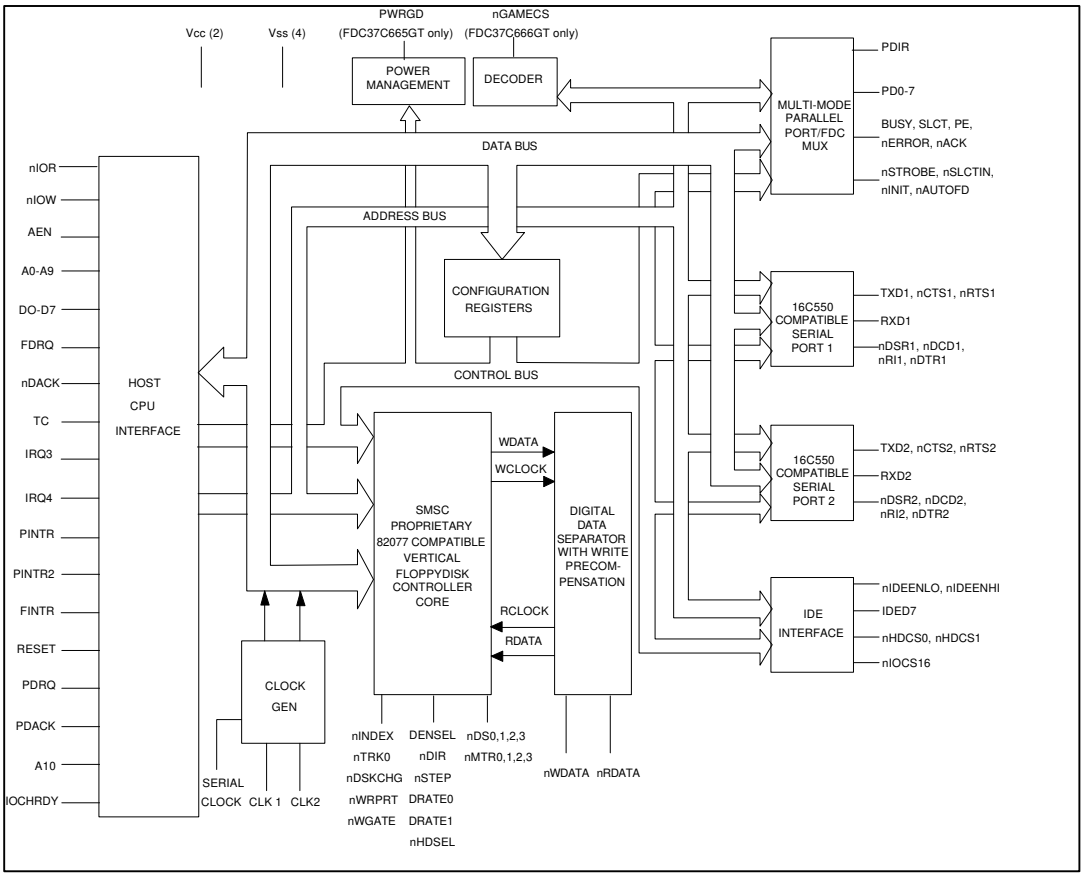



**FIGURE 1 - FDC37C665GT/FDC37C666GT BLOCK DIAGRAM**

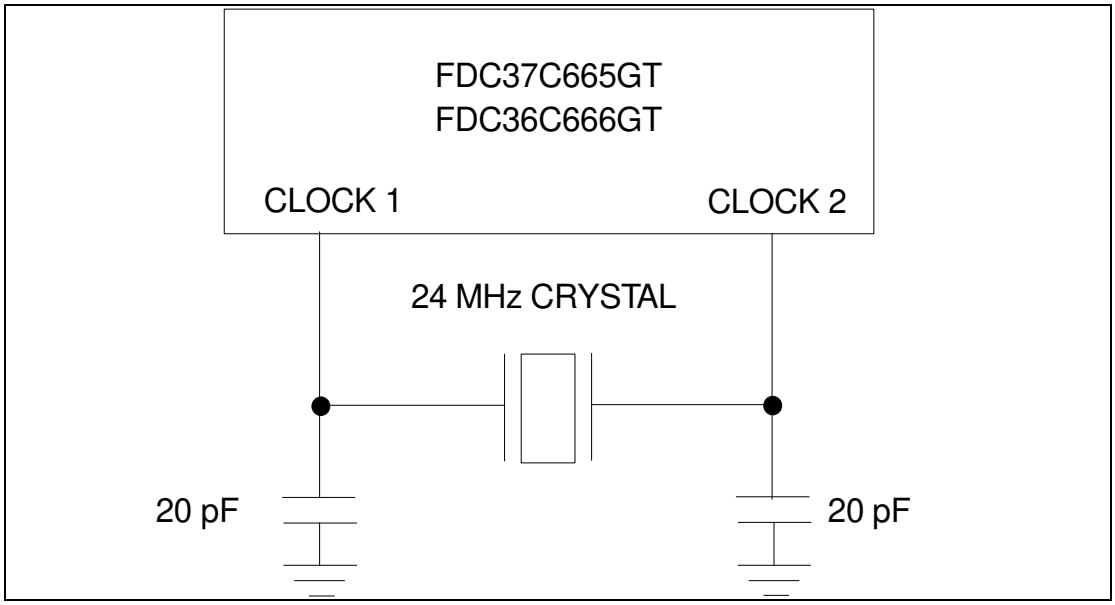



**FIGURE 2 - SUGGESTED 24 MHz OSCILLATOR CIRCUIT**

## FUNCTIONAL DESCRIPTION

### SUPER I/O REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, IDE, serial and parallel ports can be moved via the configuration registers. Some addresses are used to access more than one register.

### HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C665GT/666GT through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide except the IDE data register at port 1F0H which is 16 bits wide. All host interface output buffers are capable of sinking a minimum of 24 mA.

**Table 1 - FDC37C665GT/666GT Block Addresses**

| ADDRESS | BLOCK NAME | NOTES |
|---|---|---|
| 3F0, 3F1 | Configuration | Write only; Note 1, 2 |
| 3F0, 3F1 | Floppy Disk | Read only; Address at power up; Note 2 |
| 3F2, 3F3, 3F4, 3F5, 3F7 | Floppy Disk | Address at power up; Note 2 |
| 3F8-3FF | Serial Port Com 1 | Address at power up; Note 2 |
| 2F8-2FF | Serial Port Com 2 | Address at power up; Note 2 |
| 278-27A | Parallel Port | Address at power up; Note 2 |
| 1F0-1F7, 3F6, 3F7 | IDE | AT Mode; Note 2, 3 |

Note 1: Configuration registers can only be modified in configuration mode, entered only by writing a security code sequence to 3F0. The configuration registers can only be read in configuration mode by accessing 3F1. Access to status registers A and B of the floppy disk is disabled in configuration mode. Outside of configuration mode, a read of 3F0 accesses status register A and a read of 3F1 accesses status register B of the floppy disk.
Note 2: Address at power up; These addresses can be changed in the configuration setup.
Note 3: Addresses 320H-323H and 3F5-3F7H for XT Mode. Selectable in configuration setup.

## FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC37C665GT and FDC37C666GT are compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

## FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

**Table 2 - Status, Data and Control Registers**

| PRIMARY ADDRESS | SECONDARY ADDRESS | | REGISTER | |
|---|---|---|---|---|
| 3F0 | 370 | R | Status Register A | SRA |
| 3F1 | 371 | R | Status Register B | SRB |
| 3F2 | 372 | R/W | Digital Output Register | DOR |
| 3F3 | 373 | R/W | Tape Drive Register | TSR |
| 3F4 | 374 | R | Main Status Register | MSR |
| 3F4 | 374 | W | Data Rate Select Register | DSR |
| 3F5 | 375 | R/W | Data (FIFO) | FIFO |
| 3F6 | 376 | | Reserved | |
| 3F7 | 377 | R | Digital Input Register | DIR |
| 3F7 | 377 | W | Configuration Control Register | CCR |

**For information on the floppy disk on Parallel Port pins, refer to Configuration Register CR4 and Parallel Port Floppy Disk Controller description.**

**STATUS REGISTER A (SRA)**

**Address 3F0 READ ONLY**
This register is read-only and monitors the state of the FINTR pin and several disk interface pins, in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

**PS/2 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | INT PENDING | nDRV2 | STEP | nTRK0 | HDSEL | nINDX | nWP | DIR |
| RESET COND. | 0 | N/A | 0 | N/A | 0 | N/A | N/A | 0 |

**BIT 0 DIRECTION**
Active high status indicating the direction of head movement. A logic "1" indicating inward direction a logic "0" outward.

**BIT 1 nWRITE PROTECT**
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicating that the disk is write protected.

**BIT 2 nINDEX**
Active low status of the INDEX disk interface input.

**BIT 3 HEAD SELECT**
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

**BIT 4 nTRACK 0**
Active low status of the TRK0 disk interface input.

**BIT 5 STEP**
Active high status of the STEP output disk interface output pin.

**BIT 6 nDRV2**
Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed.

**BIT 7 INTERRUPT PENDING**
Active high bit indicating the state of the Floppy Disk Interrupt output.

**PS/2 Model 30 Mode**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | INT PENDING | DRQ | STEP F/F | TRK0 | nHDSEL | INDX | WP | nDIR |
| RESET COND. | 0 | 0 | 0 | N/A | 1 | N/A | N/A | 1 |

**BIT 0 nDIRECTION**
Active low status indicating the direction of head movement. A logic "0" indicating inward direction a logic "1" outward.

**BIT 1 WRITE PROTECT**
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicating that the disk is write protected.

**BIT 2 INDEX**
Active high status of the INDEX disk interface input.

**BIT 3 nHEAD SELECT**
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

**BIT 4 TRACK 0**
Active high status of the TRK0 disk interface input.

**BIT 5 STEP**
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

**BIT 6 DMA REQUEST**
Active high status of the DRQ output pin.

**BIT 7 INTERRUPT PENDING**
Active high bit indicating the state of the Floppy Disk Interrupt output.