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PC 98/99 Compliant Super I/O Floppy Disk Controller with Infrared Support

FEATURES

- 5 Volt Operation
- Intelligent Auto Power Management
- 16 Bit Address Qualification (Optional)
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives Directly
  - Supports Vertical Recording Format
  - 16 Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA option
  - 48 Base I/O Address, *Seven* IRQ and Three DMA Options
- Floppy Disk Available on Parallel Port Pins
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - Infrared - IrDA (HPSIR) and Amplitude Shift Keyed IR (ASKIR)
  - Alternate IR Pins (Optional)
  - 96 Base I/O Address and Eight IRQ Options
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode
  - IBM PC/XT, PC/AT, and PS/2 Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible
  - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - Enhanced Capabilities Port (ECP) Compatible (IEEE 1284 Compliant)
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, Seven IRQ and Three DMA Options
- ISA Host Interface
- IDE Interface (Optional)
  - On-Chip Decode and Select Logic Compatible with IBM PC/XT and PC/AT Embedded Hard Disk Drives
  - 48 Base I/O Address and *Seven* IRQ Options
- Game Port Select Logic
  - 48 Base I/O Addresses
- General Purpose Address Decoder
  - 16 Byte Block decode
  - 48 Base I/O Address Options
- 100 Pin QFP and TQFP Packages; Lead-Free RoHS Compliant Packages also available

ORDER NUMBER(S)

FDC37C669QFP for 100 pin, QFP Package
FDC37C669-MS for 100 pin, QFP Lead-Free RoHS Compliant Package

FDC37C669TQFP for 100 pin, TQFP Package
FDC37C669-MT for 100 pin, TQFP Lead-Free RoHS Compliant Package

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GENERAL DESCRIPTION

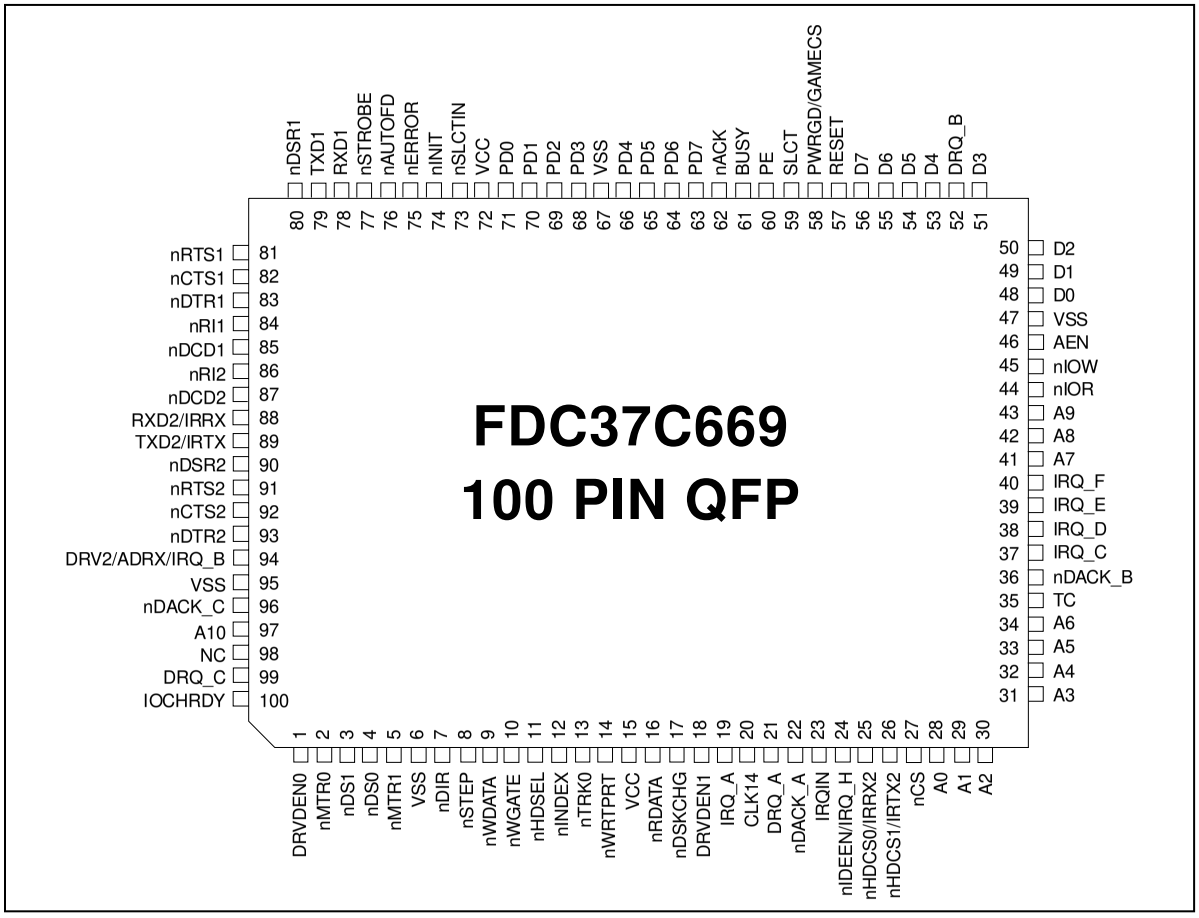
The SMSC FDC37C669 PC 95 Compatible Super I/O Floppy Disk Controller with Infrared Support utilizes SMSC's proven SuperCell technology for increased product reliability and functionality. The FDC37C669 is PC95 compliant and is optimized for motherboard applications. The FDC37C669 supports both 1 Mbps and 2 Mbps data rates and vertical vertical recording operation at 1 Mbps Data Rate.

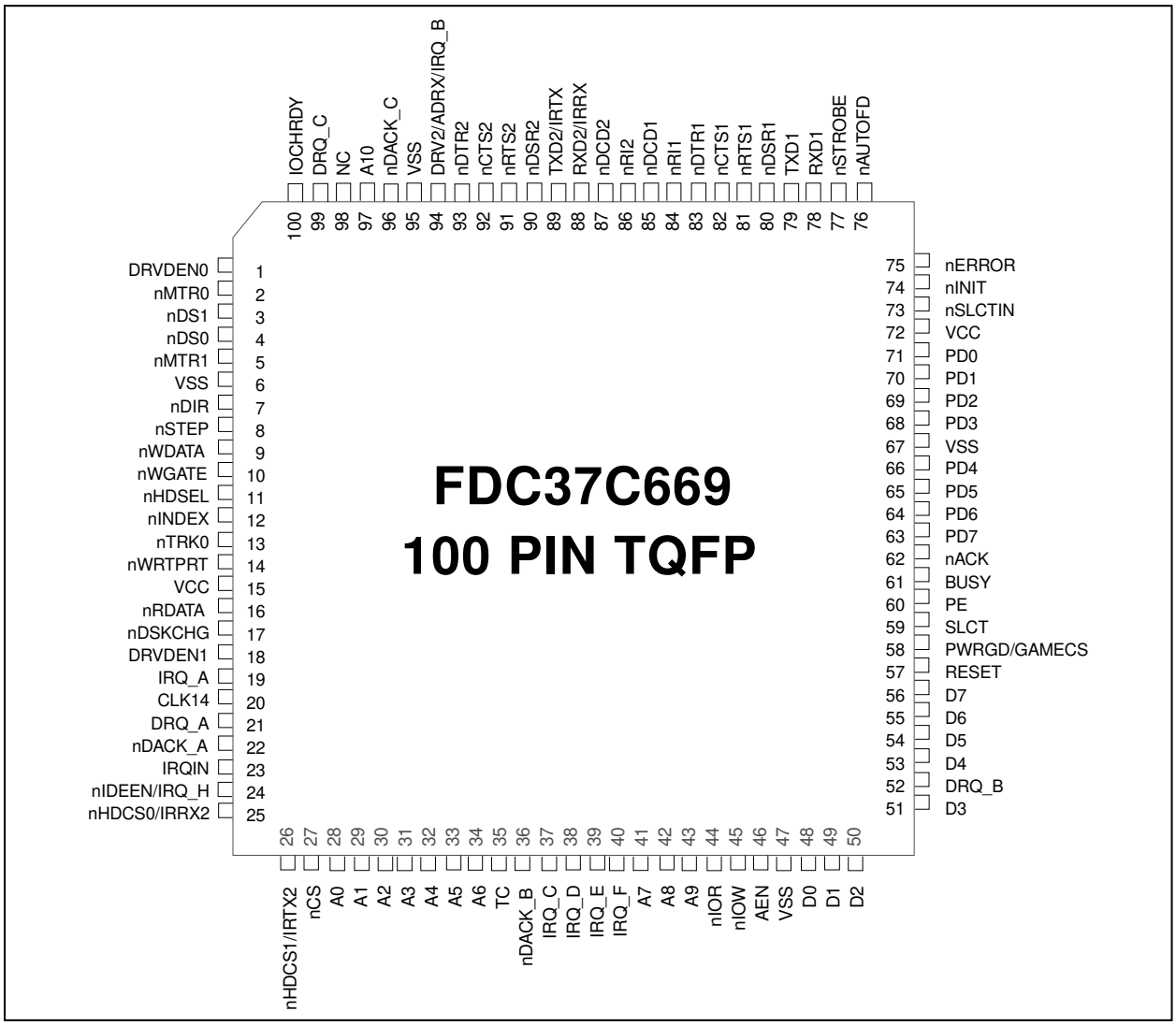
The FDC37C669 incorporates SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port which includes ChiProtect circuitry plus EPP and ECP support, IDE interface, on-chip 12 mA AT bus drivers, game port chip select and two floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use. Both on-chip UARTs are compatible with the NS16C550. One UART includes additional support for a Serial Infrared Interface, complying with IrDA, HPSIR, and ASKIR formats (used by Sharp, Apple Newton, and other PDAs). The parallel port, the IDE interface, and the game port select logic are compatible with IBM PC/AT architectures. The FDC37C669 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C669 Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. Use of the SCL feature allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs. The parallel port ChiProtect prevents damage caused by the printer being powered when the FDC37C669 is not powered.

The FDC37C669 does not require any external filter components, and is, therefore easy to use and offers lower system cost and reduced board area. The FDC37C669 is software and register compatible with SMSC's proprietary 82077AA core.

PIN CONFIGURATION




FDC37C669
100 PIN TQFP
1 DRVDEN0
2 nMTR0
3 nDS1
4 nDS0
5 nMTR1
6 VSS
7 nDIR
8 nSTEP
9 nWDATA
10 nWGATE
11 nHDSEL
12 nINDEX
13 nTRK0
14 nWRTPRT
15 VCC
16 nRDATA
17 nDSKCHG
18 DRVDEN1
19 IRQ_A
20 CLK14
21 DRQ_A
22 nDACK_A
23 IRQIN
24 nIDEEN/IRQ_H
25 nHDCS0/IRRX2
26 nHDCS1/IRTX2
27 nCS
28 A0
29 A1
30 A2
31 A3
32 A4
33 A5
34 A6
35 TC
36 nDACK_B
37 IRQ_C
38 IRQ_D
39 IRQ_E
40 IRQ_F
41 A7
42 A8
43 A9
44 nIOR
45 nIOW
46 AEN
47 VSS
48 D0
49 D1
50 D2
51 D3
52 DRQ_B
53 D4
54 D5
55 D6
56 D7
57 RESET
58 PWRGD/GAMECS
59 SLCT
60 PE
61 BUSY
62 nACK
63 PD7
64 PD6
65 PD5
66 PD4
67 VSS
68 PD3
69 PD2
70 PD1
71 PD0
72 VCC
73 nSLCTIN
74 nINIT
75 nERROR
76 nAUTOFD
77 nSTROBE
78 RXD1
79 TXD1
80 nDSR1
81 nRTS1
82 nCTS1
83 nDTR1
84 nRI1
85 nDCD1
86 nRI2
87 nDCD2
88 RXD2/IRRX
89 TXD2/IRTX
90 nDSR2
91 nRTS2
92 nCTS2
93 nDTR2
94 DRV2/ADRX/IRQ_B
95 VSS
96 nDACK_C
97 A10
98 NC
99 DRQ_C
100 IOCHRDY

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
HOST PROCESSOR INTERFACE				
48-51 53-56	Data Bus 0-7	D0-D7	*I/O24*	The data bus connection used by the host microprocessor to transmit data to and from the chip. These pins are in a high-impedance state when not in the output mode.
44	nI/O Read	nIOR	I	This active low signal is issued by the host microprocessor to indicate a read operation.
45	nI/O Write	nIOW	I	This active low signal is issued by the host microprocessor to indicate a write operation.
46	Address Enable	AEN	I	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
28-34 41-43, 97	I/O Address	A0-A10	I	These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW. All internal address decodes use the full A0 to A10 address bits.
21,52, 99	DMA Request A, B, C	DRQ_A DRQ_B DRQ_C	*O24*	This active high output is the DMA request for byte transfers of data between the host and the chip. This signal is cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode).
22,36, 96	nDMA Acknowledge A, B, C	nDACK_A nDACK_B nDACK_C	I	An active low input acknowledging the request for a DMA transfer of data between the host and the chip. This input enables the DMA read or write internally.
35	Terminal Count	TC	I	This signal indicates to the chip that DMA data transfer is complete. TC is only accepted when nDACK_x is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
19, 37-40,	Interrupt Request A, C, D, E, F,	IRQ_A IRQ_C IRQ_D IRQ_E IRQ_F	*O24* *OD24*	The interrupt request from the logical device or IRQIN is output on one of the IRQA-G signals. Refer to the configuration registers for more information. If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.
27	Chip Select Input	nCS	I	When enabled, this active low pin serves as an input for an external decoder circuit which is used to qualify address lines above A10.
57	Reset	RESET	IS	This active high signal resets the chip and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
FLOPPY DISK INTERFACE				
16	nRead Disk Data	nRDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
10	nWrite Gate	nWGATE	*OD48*	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
9	nWrite Data	nWDATA	*OD48*	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
11	nHead Select	nHDSEL	*OD48*	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
7	Direction Control	nDIR	*OD48*	This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
8	nStep Pulse	nSTEP	*OD48*	This active low high current driver issues a low pulse for each track-to-track movement of the head.
17	Disk Change	nDSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
4,3	nDrive Select O,1	nDS0,1	*OD48*	Active low open drain outputs select drives 0-1.
2,5	nMotor On 0,1	nMTR0,1	*OD48*	These active low open drain outputs select motor drives 0-1.
1	DRVDEN0	DRVDEN0	*OD48*	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
14	nWrite Protected	nWRTPRT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
13	wTrack 00	nTRK00	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
12	nIndex	nINDEX	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
18	DRVDEN1	DRVDEN 1	*OD48*	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
SERIAL PORT INTERFACE				
88	Receive Data 2	RXD2/IRRX	I	Receiver serial data input for port 2. IR Receive Data
89	Transmit Data 2	TXD2/IRTX	*O24*	Transmit serial data output for port 2. IR transmit data.
78	Receive Data 1	RXD1	I	Reciever serial data input for port 1.
79	Transmit Data 1	TXD1	*024*	Transmit serial data output for port 1.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
81,91	nRequest to Send (System Option)	nRTS1 nRTS2 (SYSOPT)	*O4*	Active low Request to Send outputs for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). Forced inactive during loop mode operation. At the trailing edge of hardware reset, the nRTS2 input is latched to determine the configuration base address. 0 : INDEX Base I/O Address = 3F0 Hex 1 : INDEX Base I/O Address = 370 Hex
83,93	nData Terminal Ready	nDTR1 nDTR2	*O4*	Active low Data Terminal Ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). Forced inactive during loop mode operation.
82,92	nClear to Send	nCTS1 nCTS2	I	Active low Clear to Send inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of nCTS.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
80,90	nData Set Ready	nDSR1 nDSR2	I	Active low Data Set Ready inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. Note: Bit 5 of MSR is the complement of nDSR.
85,87	nData Carrier Detect	nDCD1 nDCD2	I	Active low Data Carrier Detect inputs for the serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. Note: Bit 7 of MSR is the complement of nDCD.
84,86	nRing Indicator	nRI1 nRI2	I	Active low Ring Indicator inputs for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. Note: Bit 6 of MSR is the complement of nRI.
PARALLEL PORT INTERFACE				

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
73	nPrinter Select Input	nSLCTIN	*OD24* *0P24*	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
74	nInitiate Output	nINIT	*OD24* *0P24*	This output is bit 2 of the printer control register. This is used to initiate the printer when low. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
76	nAutofeed Output	nAUTOFD	*OD24* *0P24*	This output goes low to cause the printer to automatically feed one line after each line is printed. The nAUTOFD output is the complement of bit 1 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
77	nStrobe Output	nSTROBE	*OD24* *0P24*	An active low pulse on this output is used to strobe the printer data into the printer. The nSTROBE output is the complement of bit 0 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
61	Busy	BUSY	I	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
62	nAcknowledge	nACK	I	A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the nACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
60	Paper End	PE	I	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
59	Printer Selected Status	SLCT	I	This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
75	nError	nERROR	I	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the nERR input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
63-66 68-71	Port Data	PD0-PD7	*I/O24*	The bi-directional parallel data bus is used to transfer information between CPU and peripherals.
100	IOCHRDY	IOCHRDY	*OD24P*	In EPP mode, this pin is pulled low to extend the read/write command. This pin has an internal pull-up.
IDE/ALT IR PINS				
24	nIDE Enable	nIDEEN	*O24P* (Note 1)	This active low signal is active when the IDE is enabled and the I/O address is accessing an IDE register.
	Interrupt Request H	IRQ_H	*024*	The interrupt request from a logical device or IRQIN may be output on the IRQH signal. Refer to the configuration registers for more information.
			OD24	If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.

25	nIDE Chip Select 0 IRRX2	nHDCS0 IRRX2	*O24P* (Note 1) I	This is the Hard Disk Chip select corresponding to the eight control block addresses. Alternate IR Receive input
26	nIDE Chip Select 1 IR Transmit 2	nHDCS1 IRTX2	*O24P* (Note 1) *O24P*	This is the Hard Disk Chip select corresponding to the alternate status register. Alternate IR transmit output
MISCELLANEOUS				
20	CLOCK 14	CLK14	ICLK	The external connection to a single source 14.318 MHz clock.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
94	Drive 2	DRV2	I	In PS/2 mode, this input indicates whether a second drive is connected; DRV2 should be low if a second drive is connected. This status is reflected in a read of Status Register A.
	Address X	nADRX	*OD24*	Active low address decode out: used to decode a 1, 8, or 16 byte address block. (An external pull-up is required). Refer to Configuration registers CR03, CR08 and CR09 for more information. This pin has a 30ua internal pull-up. The interrupt request from a logical device or IRQIN may be output on IRQ_B. Refer to the configuration registers for more information. (If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.)
	Interrupt Request B	IRQ_B	*024* *(OD24)*	
23		IRQIN	I	This pin is used to steer an interrupt signal from an external device onto one of eight IRQ outputs IRQA-H.
58		PWRGD	I	This active high input indicates that the power (V_{CC}) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all inputs to Mercury are disconnected and put into a low power mode; all outputs are put into high impedance. The contents of all registers are preserved as long as V_{CC} has a valid value. The driver current drain in this mode drops to ISTBY - standby current. This input has an internal 30ua pull-up.
		nGAMECS	*O4*	This is the Game Port Chip Select output - active low. It will go active when the I/O address, qualified by AEN, matches that selected in Configuration register CR1E.
98	I/O Power	*NC*		No Connect
15,72	Power	V_{CC}		Positive Supply Voltage.

DESCRIPTION OF PIN FUNCTIONS

QFP/ TQFP PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
6,47, 67,95	Ground	GND		Ground Supply.

Note 1: Refer to Configuration Register 00 for information on the pull-ups for these pins!
Note IDE does not decode for 377, 3F7
Note RI and the Serial interrupt is always active if system power is applied to the chip.

BUFFER TYPE DESCRIPTIONS

BUFFER TYPE	DESCRIPTION
I/O24	*Input/Output. 24 mA sink; 12 mA source*
O24	*Output. 24 mA sink; 12 mA source*
OD48	*Open drain. 48 mA sink*
O4	*Output. 4 mA sink; 2 mA source*
OD24	*Output. 24 mA sink*
OD24P	*Open drain. 24 mA sink; 30µA source*
OP24	*Output. 24 mA sink; 4 mA source*
024P	*Output. 24 mA sink; 12 mA source; with 30µA pull-up*
OCLK	*Output to external crystal*
ICLK	*Input to Crystal Oscillator Circuit (CMOS levels)*
I	*Input TTL compatible.*
IS	*Input with Schmitt Trigger.*

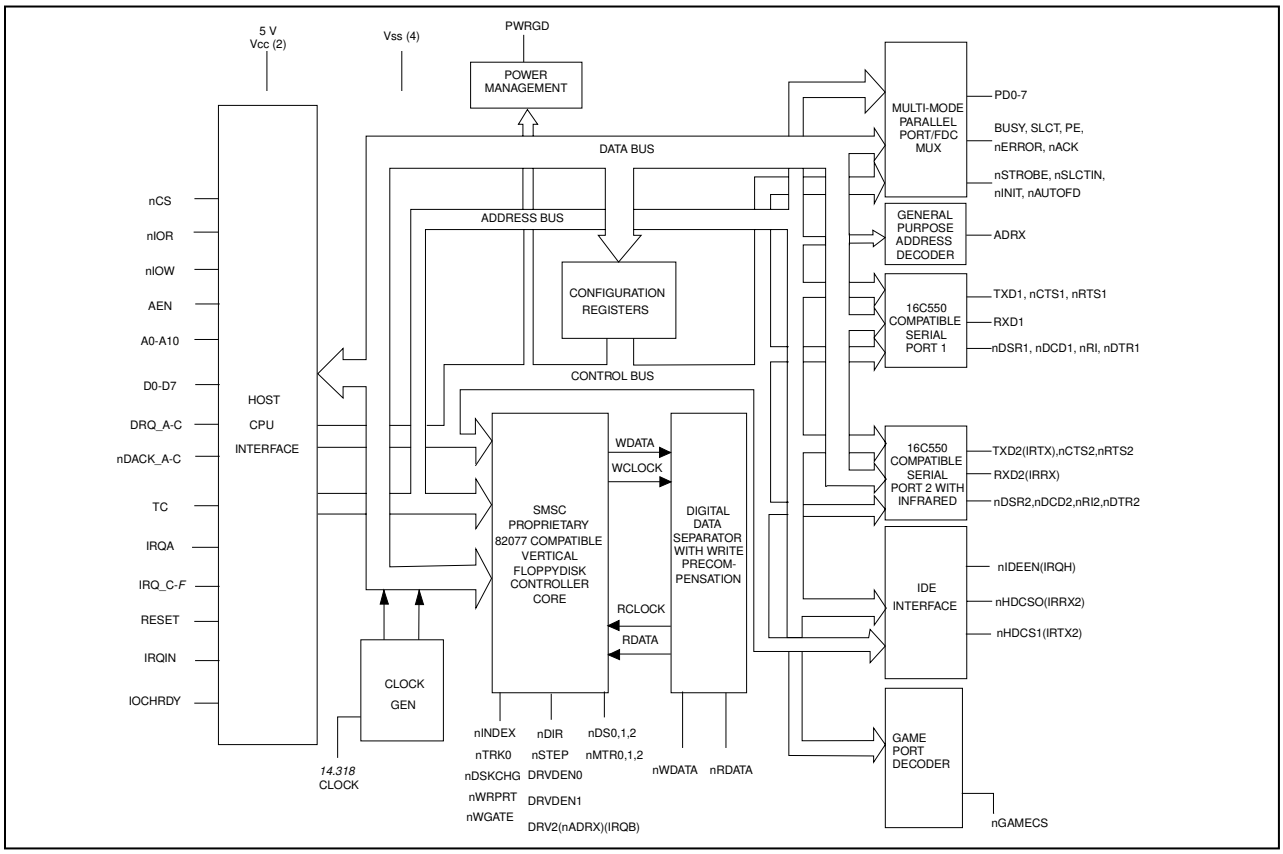


FIGURE 1 - FDC37C669 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

SUPER I/O REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, IDE, serial and parallel ports can be moved via the configuration registers. Some addresses are used to access more than one register.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C669 through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide except the IDE data register at port 1F0H which is 16 bits wide. All host interface output buffers are capable of sinking a minimum of 12 mA.

Table 1 - FDC37C669 Block Addresses

ADDRESS	BLOCK NAME	NOTES
3F0, 3F1 or 370, 371	Configuration	Write only; Note 1, 2
Base +0,1	Floppy Disk	Read only; Disabled at power up; Note 2
Base +[2:5, 7]	Floppy Disk	Disabled at power up; Note 2
Base +[0:7]	Serial Port Com 1	Disabled at power up; Note 2
Base +[0:7]	Serial Port Com 2	Disabled at power up; Note 2
Base +[0:3] all modes Base +[4:7] for EPP Base +[400:403] for ECP	Parallel Port	Disabled at power up; Note 2
Base1 +[0:7] Base2 +[6]	IDE	Disabled at power up; Note 2

Note 1: Configuration registers can only be modified in configuration mode, refer to the configuration register description for more information. Access to status registers A and B of the floppy disk is disabled in configuration mode.

Note 2: The base addresses must be set in the configuration registers before accessing the logical devices.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC37C669 is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the FDC description assumes the Base I/O Address is 3F0.

Table 2 - Status, Data and Control Registers

BASE I/O ADDRESS		REGISTER	
+0	R	Status Register A	SRA
+1	R	Status Register B	SRB
+2	R/W	Digital Output Register	DOR
+3	R/W	Tape Drive Register	TSR
+4	R	Main Status Register	MSR
+4	W	Data Rate Select Register	DSR
+5	R/W	Data (FIFO)	FIFO
+6		Reserved	
+7	R	Digital Input Register	DIR
+7	W	Configuration Control Register	CCR

For information on the floppy disk on Parallel Port pins, refer to Configuration Register CR4 and Parallel Port Floppy Disk Controller description.

STATUS REGISTER A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the FINTR pin and several disk interface pins, in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	N/A	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION

Active high status indicating the direction of head movement. A logic "1" indicating inward direction a logic "0" outward.

BIT 1 nWRITE PROTECT

Active low status of the WRITE PROTECT disk interface input. A logic "0" indicating that the disk is write protected.

BIT 2 nINDEX

Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT

Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0

Active low status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2

Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicating inward direction a logic "1" outward.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicating that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DRQ output pin.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

STATUS REGISTER B (SRB)

Address F1 READ ONLY

This register is read-only and monitors the state of several disk interface pins, in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0

Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1

Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE

Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE

Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE

Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0

Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset.

BIT 6 RESERVED

Always read as a logic "1".

BIT 7 RESERVED

Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2
Active low status of the DS2 disk interface output.

BIT 1 nDRIVE SELECT 3
Active low status of the DS3 disk interface output.

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0
Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1
Active low status of the DS1 disk interface output.

BIT 7 nDRV2
Active low status of the DRV2 disk interface input.

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and contains a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bit a are binary encoded for the four drive selects DS0-DS3, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

PC/AT and Model 30 Mode:

Writing this bit to logic "1" will enable the DRQ, nDACK, TC and FINTR outputs. This bit being a logic "0" will disable the nDACK and TC inputs, and hold the DRQ and FINTR outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DRQ, nDACK, TC and FINTR pins are always enabled. During a reset, the DRQ, nDACK, TC, and FINTR pins will remain enabled, but this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2

This bit controls the MTR2 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 7 MOTOR ENABLE 3

This bit controls the MTR3 disk interface output. A logic "1" in this bit causes the output to go active.

Table 3 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

This register is included for 82077 software compatability. The robust digital data separator used in the FDC37C669 does not require its characteristics modified for tape support. The contents of this register are not used internal to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Table 4- Tape Select Bits

TAPE SEL1	TAPE SEL2	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 5 - Internal 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS3	nDS2	nDS1	nDS0	nMTR3	nMTR2	nMTR1	nMTR0
X	X	X	1	0	0	1	1	1	0	nBIT 7	nBIT 6	nBIT 5	nBIT 4
X	X	1	X	0	1	1	1	0	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
X	1	X	X	1	0	1	0	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
1	X	X	X	1	1	0	1	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4

Table 6 - Internal 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS3	nDS2	nDS1	nDS0	nMTR3	nMTR2	nMTR1	nMTR0
X	X	X	1	0	0	1	1	0	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
X	X	1	X	0	1	1	1	1	0	nBIT 7	nBIT 6	nBIT 4	nBIT 5
X	1	X	X	1	0	1	0	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
1	X	X	X	1	1	0	1	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5

Table 7 - External 2 to 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	0	1	0
X	X	1	X	0	1	0	1	1	0
X	1	X	X	1	0	1	0	1	0
1	X	X	X	1	1	1	1	1	0
X	X	X	0	0	0	0	0	1	1
X	X	0	X	0	1	0	1	1	1
X	0	X	X	1	0	1	0	1	1
0	X	X	X	1	1	1	1	1	1

Table 8 - External 2 to 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	1	0
X	X	1	X	0	1	0	0	1	0
X	1	X	X	1	0	1	0	1	0
1	X	X	X	1	1	1	1	1	0
X	X	X	0	0	0	0	1	1	1
X	X	0	X	0	1	0	0	1	1
X	0	X	X	1	0	1	0	1	1
0	X	X	X	1	1	1	1	1	1