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Floppy Disk Controller

FEATURES

- 3.3/5 Volt Operation
- Intelligent Auto Power Management
- 2.88MB FDC37C78 Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives Directly
  - Supports Vertical Recording Format
  - 16 Byte Data FIFO
  - 100% IBM Compatibility
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA Option
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
- Enhanced Digital Data Separator
  - 2 Mbps (Only Available When V_{CC} = 5V), 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- 48 pin TQFP Package

TABLE OF CONTENTS

GENERAL DESCRIPTION

The SMSC FDC37C78 Floppy Disk Controller utilizes SMSC's proven SuperCell technology for increased product reliability and functionality. The FDC37C78 optimized for motherboard applications. The FDC37C78 supports both 1 Mbps and 2 Mbps data rates and vertical vertical recording operation at 1 Mbps Data Rate.

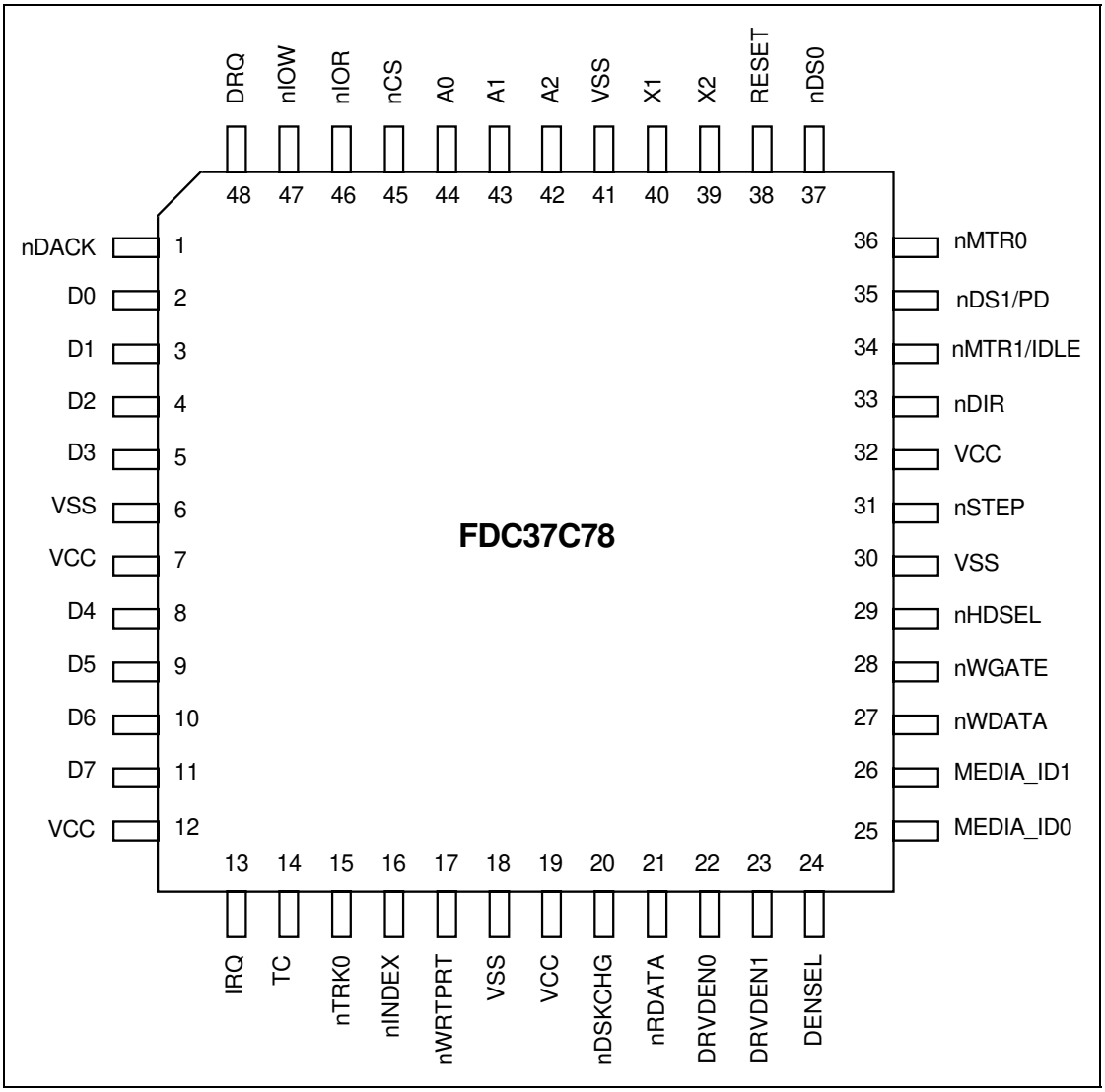
The FDC37C78 incorporates SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte data FIFO, on-chip 12 mA bus drivers and two floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use.

The FDC37C78 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C78 Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. Use of the SCL feature allows programmable system configuration of key functions of FDC

The FDC37C78 does not require any external filter components, and is, therefore easy to use and offers lower system cost and reduced board area. The FDC37C78 is software and register compatible with SMSC's proprietary 82077AA core.

PIN CONFIGURATION



FDC37C78 PIN OUT

FDC37C78 48 Pin FDC

PIN #	NAME	PIN #	NAME
1	nDACK	25	MEDIA_ID0
2	D0	26	MEDIA_ID1
3	D1	27	nWDATA
4	D2	28	nWGATE
5	D3	29	nHDSEL
6	VSS	30	VSS
7	VCC	31	nSTEP
8	D4	32	VCC
9	D5	33	nDIR
10	D6	34	nMTR1/IDLE
11	D7	35	nDS1/PD
12	VCC	36	nMTR0
13	IRQ	37	nDS0
14	TC	38	RESET
15	nTRK0	39	X2
16	nINDEX	40	X1
17	nWRTPRT	41	VSS
18	VSS	42	A2
19	VCC	43	A1
20	nDSKCHG	44	A0
21	nRDATA	45	nCS
22	DRVDEN0	46	nIOR
23	DRVDEN1	47	nIOW
24	DENSEL	48	DRQ

Note: “n” denotes active low signal.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
HOST PROCESSOR INTERFACE				
2-5, 8-11	Data Bus 0-7	D0-D7	I/O12	The data bus connection used by the host microprocessor to transmit data to and from the chip. These pins are in a high-impedance state when not in the output mode.
46	I/O Read	nIOR	I	This active low signal is issued by the host microprocessor to indicate a read operation.
47	I/O Write	nIOW	I	This active low signal is issued by the host microprocessor to indicate a write operation.
44-42	I/O Address	A0-A2	I	These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW.
48	DMA Request	DRQ	O12	This active high output is the DMA request for byte transfers of data between the host and the chip. This signal is cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode).
1	n DMA Acknowledge	nDACK	I	An active low input acknowledging the request for a DMA transfer of data between the host and the chip. This input enables the DMA read or write internally.
14	Terminal Count	TC	I	This signal indicates to the chip that DMA data transfer is complete. TC is only accepted when nDACK is low. TC is active high.
13	Interrupt Request	IRQ	O12	The interrupt request from the logical device is output on the IRQ signal. Refer to the configuration registers for more information.
45	Chip Select Input	nCS	I	When enabled, this active low pin serves as an input for an external decoder circuit which is used to qualify address lines above A2.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
38	Reset	RESET	IS	This active high signal resets the chip and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
FLOPPY DISK INTERFACE				
21	Read Disk Data	nRDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
27	Write Data	nWDATA	OD20	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
29	Head Select	nHDSEL	OD20	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
33	Direction Control	nDIR	OD20	This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
31	Step Pulse	nSTEP	OD20	This active low high current driver issues a low pulse for each track-to-track movement of the head.
20	Disk Change	nDSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
22, 23	DRVDEN 0, DRVDEN 1	DRVDEN0, DRVDEN1	OD20	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
24	Density Select	DENSEL	OD20	Indicates whether a low (250/300 Kb/s) or high (500 Kb/s) data rate has been selected. This is determined by the IDENT bit in Configuration Register 3.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
25, 26	Media ID0, Media ID1	MEDIA_ID0, MEDIA_ID1	I	In Floppy Enhanced Mode 2 - These bits are the Media ID 0,1 inputs. The value of these bits can be read as bits 6 and 7 of the Floppy Tape Register.
28	Write Gate	nWGATE	OD20	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
15	Track 0	nTRK0	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
16	Index	nINDEX	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
17	nWrite Protected	nWRTPRT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
36	nMotor On 0	nMTR0	OD20	This active low open drain output selects motor drive 0.
37	nDrive Select 0	nDS0	OD20	This active low open drain output selects drive 0.
34	nMotor On 1 Idle	nMTR1 IDLE	OD20 OD20	This active low open drain output select motor drive 0. This pin indicates that the part is in the IDLE state and can be powered down. Whenever the part is in this state, IDLE pin is active high. If the part is powered down by the Auto Powerdown Mode, IDLE pin is set high and if the part is powered down by setting the DSR POWERDOWN bit (direct), IDLE pin is set low.
35	nDrive Select 1 Powerdown	nDS1 PD	OD20 OD20	This active low open drain output selects drive 0. This pin is active high whenever the part is in powerdown state, either via DSR POWERDOWN bit (direct) or via the Auto Powerdown Mode. This pin can be used to disable an external oscillator's output.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
MISCELLANEOUS				
40	CLOCK 1	X1	ICLK	The external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
39	CLOCK 2	X2	OCLK	24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
7, 12, 19, 32	Power	V_{CC}		Positive Supply Voltage.
6, 18, 30, 41	Ground	GND		Ground Supply.

BUFFER TYPE DESCRIPTIONS

Note: These values are for 3.3V operation. See Operational Description for 3.3V/5V values.

BUFFER TYPE	DESCRIPTION
I/O12	Input/output. 12 mA sink; 6 mA source
O12	Output. 12 mA sink; 6 mA source
OD20	Open drain. 20 mA sink
OCLK	Output to external crystal
ICLK	Input to Crystal Oscillator Circuit (CMOS levels)
I	Input TTL compatible.
IS	Input with Schmitt Trigger

FUNCTIONAL DESCRIPTION

FDC37C78 REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the FDC37C78 immediately after power up. Some addresses are used to access more than one register.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C78 through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide.

Table 1 - FDC37C78 Block Addresses

ADDRESS	BLOCK NAME	NOTES
+0, +1	Configuration	Write only; Note 1, 2
Base +0,1	Floppy Disk	Read only; Disabled at power up; Note 2
Base +[2:5, 7]	Floppy Disk	Disabled at power up; Note 2

Note 1: Configuration registers can only be modified in configuration mode, refer to the configuration register description for more information. Access to status registers A and B of the floppy disk is disabled in configuration mode.

Note 2: The fdc must be enabled in the configuration registers before accessing the registers.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC37C78 is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the FDC description assumes the Base I/O Address is 3F0.

Table 2 - Status, Data and Control Registers

BASE I/O ADDRESS		REGISTER	
+0		Reserved	
+1		Reserved	
+2	R/W	Digital Output Register	DOR
+3	R/W	Tape Drive Register	TSR
+4	R	Main Status Register	MSR
+4	W	Data Rate Select Register	DSR
+5	R/W	Data (FIFO)	FIFO
+6		Reserved	
+7	R	Digital Input Register	DIR
+7	W	Configuration Control Register	CCR

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and contains a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bit a are binary encoded for the four drive selects DS0-DS3, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

Writing this bit to logic "1" will enable the DRQ, nDACK, TC and IRQ outputs. This bit being a logic "0" will disable the nDACK and TC inputs, and hold the DRQ and IRQ outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2

This bit controls the MTR2 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 7 MOTOR ENABLE 3

This bit controls the MTR3 disk interface output. A logic "1" in this bit causes the output to go active.

Table 3 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

This register is included for 82077 software compatability. The robust digital data separator used in the FDC37C78 does not require its characteristics modified for tape support. The contents of this register are not used internal to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Table 4- Tape Select Bits

TAPE SEL1	TAPE SEL2	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 5 - Internal 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS3	nDS2	nDS1	nDS0	nMTR3	nMTR2	nMTR1	nMTR0
X	X	X	1	0	0	1	1	1	0	nBIT 7	nBIT 6	nBIT 5	nBIT 4
X	X	1	X	0	1	1	1	0	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
X	1	X	X	1	0	1	0	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
1	X	X	X	1	1	0	1	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4

Table 6 - Internal 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS3	nDS2	nDS1	nDS0	nMTR3	nMTR2	nMTR1	nMTR0
X	X	X	1	0	0	1	1	0	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
X	X	1	X	0	1	1	1	1	0	nBIT 7	nBIT 6	nBIT 4	nBIT 5
X	1	X	X	1	0	1	0	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
1	X	X	X	1	1	0	1	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5

Table 7 - External 2 to 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	0	1	0
X	X	1	X	0	1	0	1	1	0
X	1	X	X	1	0	1	0	1	0
1	X	X	X	1	1	1	1	1	0
X	X	X	0	0	0	0	0	1	1
X	X	0	X	0	1	0	1	1	1
X	0	X	X	1	0	1	0	1	1
0	X	X	X	1	1	1	1	1	1

Table 8 - External 2 to 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	1	0
X	X	1	X	0	1	0	0	1	0
X	1	X	X	1	0	1	0	1	0
1	X	X	X	1	1	1	1	1	0
X	X	X	0	0	0	0	1	1	1
X	X	0	X	0	1	0	0	1	1
X	0	X	X	1	0	1	0	1	1
0	X	X	X	1	1	1	1	1	1

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are a high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Media ID1	Media ID0	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

For this mode, DRATE0 and DRATE1 pins are inputs, and these inputs are gated into bits 6 and 7 of the 3F3 register. These two bits are not affected by a hard or soft reset.

BIT 7 Media ID 1; Read Only (See Table 9a)

BIT 6 Media ID 0; Read Only (See Table 9b)

BITS 5 and 4 Drive Type ID - These Bits reflect two of the bits of configuration register 6; which two bits depends on the last drive selected in the Digital Output Register (3F2). (See Table 11)

BITS 3 and 2 Floppy Boot Drive - These bits reflect the value of configuration register 7 bits 1, 0. Bit 3 = CR7 Bit DB1. Bit 2 = CR7 Bit DB0.

Bits 1 and 0 - Tape Drive Select (READ/WRITE). Same as in Normal and Enhanced Floppy Mode. 1.

Table 9a

	Media ID1	
Pin 26	Bit 7	
	CR7-DB3=0	CR7-DB3=1
0	0	1
1	1	0

Table 9b

	Media ID0	
Pin 25	Bit 6	
	CR7-DB2=0	CR7-DB2=1
0	0	1
1	1	0

Table 9c - Drive Type ID

Digital Output Register		**Register 3F3 - Drive Type ID**	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	CR6 - Bit 1	CR6 - Bit 0
0	1	CR6 - Bit 3	CR6 - Bit 2
1	0	CR6 - Bit 5	CR6 - Bit 4
1	1	CR6 - Bit 7	CR6 - Bit 6

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 13 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT

These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 12 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. this starting track number can be changed by the configure command.

BIT 5 UNDEFINED

Should be written as a logic "0".

BIT 6 LOW POWER

A logic "1" written to this bit will put the floppy controller into Manual Low Power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Table 10 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY
111	0.00 ns-DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	Default (See Table 14)

Table 11 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL (1)		DRATE (2)	
DRT1	**DRT0**	**SEL1**	**SEL0**	**MFM**	**FM**	**IDENT=1**	**IDENT=0**	**1**	**2**
0	0	1	1	1Meg	---	1	0	1	1
0	0	0	0	500	250	1	0	0	0
0	0	0	1	300	150	0	1	0	1
0	0	1	0	250	125	0	1	1	0
0	1	1	1	1Meg	---	1	0	1	1
0	1	0	0	500	250	1	0	0	0
0	1	0	1	500	250	0	1	0	1
0	1	1	0	250	125	0	1	1	0
1	0	1	1	1Meg	---	1	0	1	1
1	0	0	0	500	250	1	0	0	0
1	0	0	1	2Meg	---	0	1	0	1
1	0	1	0	250	125	0	1	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: This is for DENSEL in normal mode.
Note 2: This is for DRATE0, DRATE1 when Drive Opt are 00.

Table 12 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

*The 2 Mbps data rate is only available if V_{CC} = 5V.

MAIN STATUS REGISTER

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. NO delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY

BIT 0 - 3 DRVx BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 15 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold \# } x \left| \frac{1}{\text{DATA RATE}} \text{ x } 8 \right| - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 13- FIFO Service Delay

FIFO THRESHOLD EXAMPLES	**MAXIMUM DELAY TO SERVICING AT 2 Mbps* DATA RATE**
1 byte	1 x 4 µs - 1.5 µs = 2.5 µs
2 bytes	2 x 4 µs - 1.5 µs = 6.5 µs
8 bytes	8 x 4 µs - 1.5 µs = 30.5 µs
15 bytes	15 x 4 µs - 1.5 µs = 58.5 µs
FIFO THRESHOLD EXAMPLES	**MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE**
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs
FIFO THRESHOLD EXAMPLES	**MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE**
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

*The 2 Mbps data rate is only available if V_{CC} = 5V.

DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY
This register is read-only.

	7	6	5	4	3	2	1	0
	DSK CHG							
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 will remain in a high impedance state during a read of this register.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

CONFIGURATION CONTROL REGISTER (CCR)

Address 3F7 WRITE ONLY

	7	6	5	4	3	2	1	0
							DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 13 for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0" by the DOR and the DSR resets.

STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 14 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 15 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D*). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

* D= Decimal

Table 16 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. Read Data command - the FDC encountered a deleted data address mark. 2. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 17 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the RESET pin of the FDC37C78, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

RESET Pin (Hardware Reset)

The RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODE OF OPERATION

PC/AT mode - (IDENT high, MFM a "don't care")

The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (IRQ and DRQ can be hi Z), and TC and DENSEL become active high signals.