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FDC6312P

Dual P-Channel 1.8V PowerTrench® Specified MOSFET

General Description

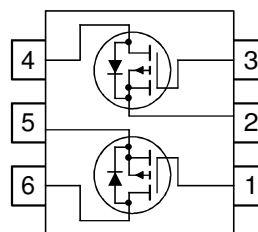
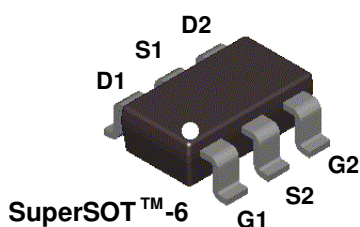
These P-Channel 1.8V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Power management
- Load switch

Features

- -2.3 A, -20 V. $R_{DS(ON)} = 115 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
 $R_{DS(ON)} = 155 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
 $R_{DS(ON)} = 225 \text{ m}\Omega @ V_{GS} = -1.8 \text{ V}$
- High performance trench technology for extremely low $R_{DS(ON)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick)



Absolute Maximum Ratings T_A=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|-----------------------------------|--|---------------|-------|
| V _{DSS} | Drain-Source Voltage | -20 | V |
| V _{GSS} | Gate-Source Voltage | ±8 | V |
| I _D | Drain Current – Continuous (Note 1a) | -2.3 | A |
| | – Pulsed | -7 | |
| P _D | Power Dissipation for Single Operation (Note 1a) | 0.96 | W |
| | | 0.9 (Note 1b) | |
| | | 0.7 (Note 1c) | |
| T _J , T _{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|------------------|---|-----|------|
| R _{θJA} | Thermal Resistance, Junction-to-Ambient (Note 1a) | 130 | °C/W |
| R _{θJC} | Thermal Resistance, Junction-to-Case (Note 1) | 60 | °C/W |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|----------------|----------|-----------|------------|------------|
| .312 | FDC6312P | 13" | 12mm | 3000 units |

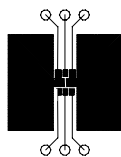
Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|------|-------------------------|--------------------------|----------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain–Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$ | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | -11 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$ | | | -1 | μA |
| I_{GSSF} | Gate–Body Leakage, Forward | $V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$ | | | 100 | nA |
| I_{GSSR} | Gate–Body Leakage, Reverse | $V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$ | | | -100 | nA |
| On Characteristics (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | -0.4 | -0.9 | -1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | 2 | | mV/ $^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS} = -4.5\text{ V}, I_D = -2.3\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -1.9\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -1.6\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -2.3\text{ A}, T_J = 125^\circ\text{C}$ | | 92 116 166 112 | 115 155 225 150 | m Ω |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$ | -7 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$ | | 5.3 | | S |
| Dynamic Characteristics | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ | | 467 | | pF |
| C_{oss} | Output Capacitance | $f = 1.0\text{ MHz}$ | | 85 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 38 | | pF |
| Switching Characteristics (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ | | 8 | 16 | ns |
| t_r | Turn–On Rise Time | $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$ | | 13 | 23 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 18 | 32 | ns |
| t_f | Turn–Off Fall Time | | | 8 | 16 | ns |
| Q_g | Total Gate Charge | $V_{DS} = -10\text{ V}, I_D = -2.3\text{ A},$ | | 4.4 | 7 | nC |
| Q_{gs} | Gate–Source Charge | $V_{GS} = -4.5\text{ V}$ | | 1.0 | | nC |
| Q_{gd} | Gate–Drain Charge | | | 0.8 | | nC |
| Drain–Source Diode Characteristics and Maximum Ratings | | | | | | |
| I_S | Maximum Continuous Drain–Source Diode Forward Current | | | | -0.8 | A |
| V_{SD} | Drain–Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = -0.8\text{ A}$ (Note 2) | | -0.7 | -1.2 | V |

Notes:

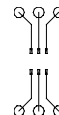
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 130 °C/W when mounted on a 0.125 in² pad of 2 oz. copper.



b) 140 °W when mounted on a .004 in² pad of 2 oz copper



c) 180 °W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

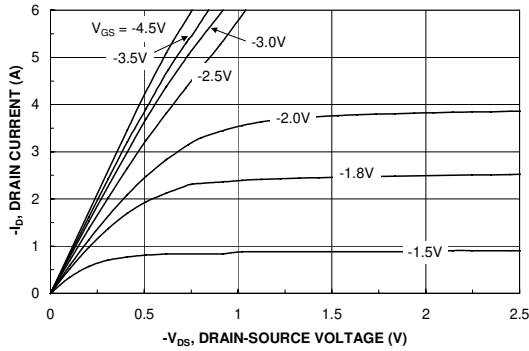


Figure 1. On-Region Characteristics.

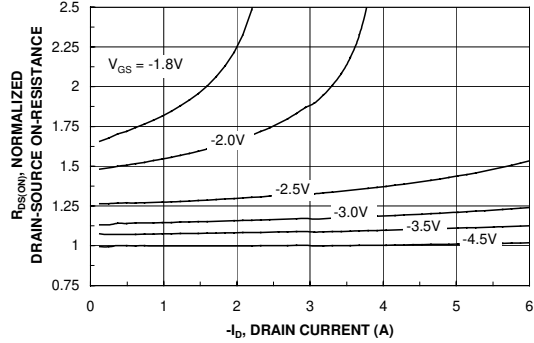


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

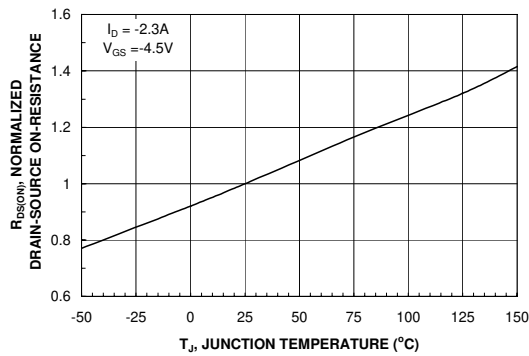


Figure 3. On-Resistance Variation with Temperature.

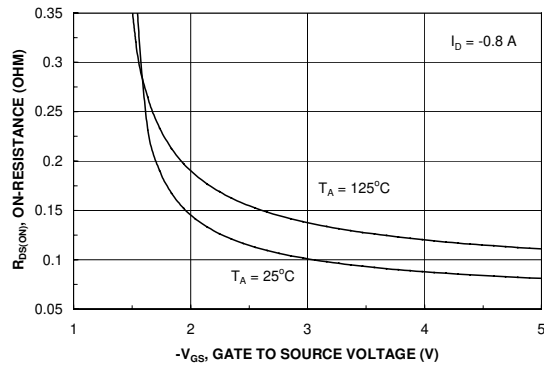


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

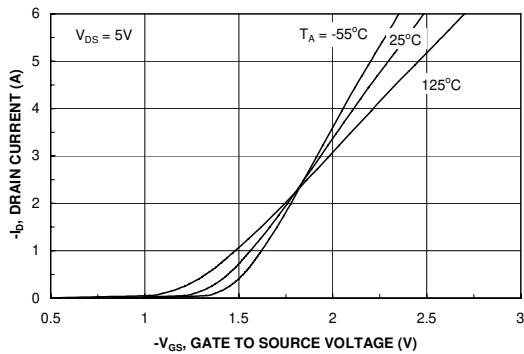


Figure 5. Transfer Characteristics.

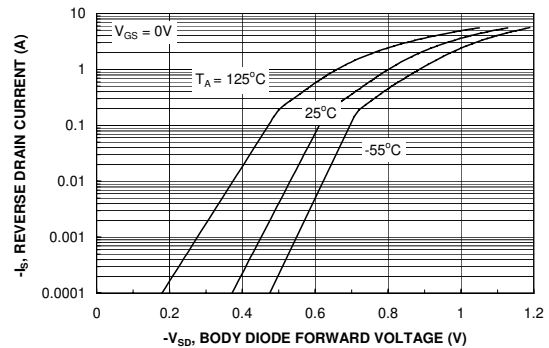


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

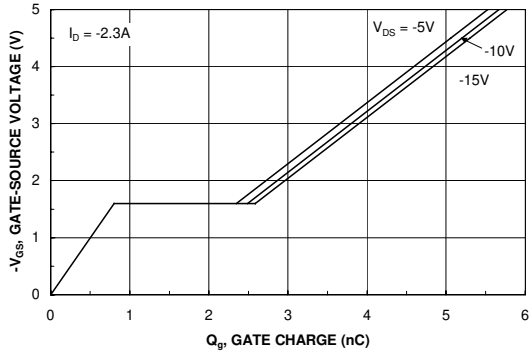


Figure 7. Gate Charge Characteristics.

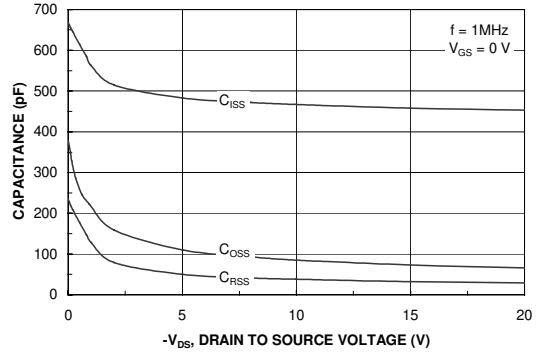


Figure 8. Capacitance Characteristics.

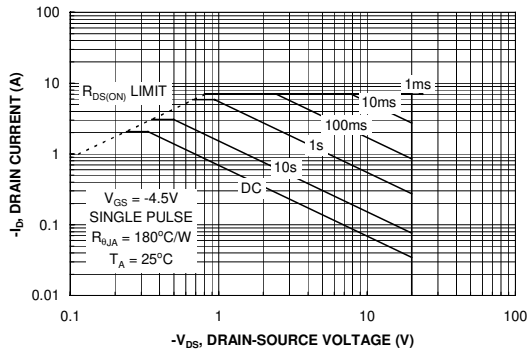


Figure 9. Maximum Safe Operating Area.

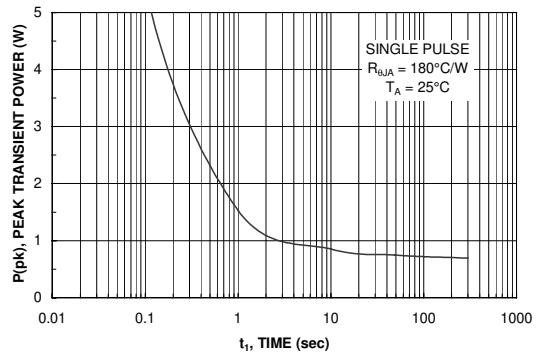


Figure 10. Single Pulse Maximum Power Dissipation.

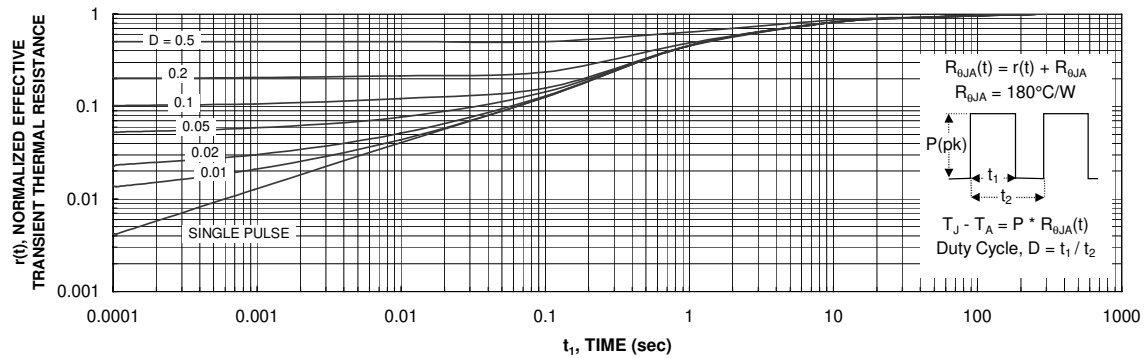


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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