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FDC6321C Dual N & P Channel , Digital FET

General Description

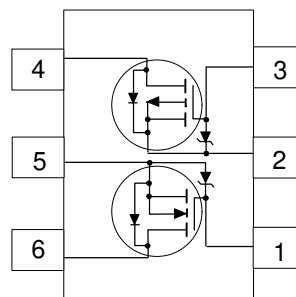
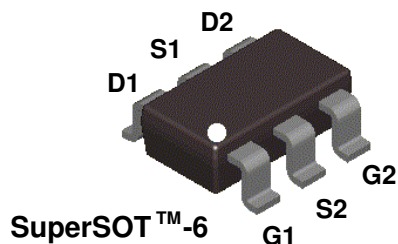
These dual N & P Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors in load switching applications. Since bias resistors are not required this dual digital FET can replace several digital transistors with different bias resistors.

Features

- N-Ch 25 V, 0.68 A, $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
- P-Ch -25 V, -0.46 A, $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 V$.
- Very low level gate drive requirements allowing direct operation in 3 V circuits. $V_{GS(th)} < 1.0V$.
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Replace multiple dual NPN & PNP digital transistors.



Mark: .321



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}, V_{CC}	Drain-Source Voltage, Power Supply Voltage	25	-25	V
V_{GS}, V_{IN}	Gate-Source Voltage,	8	-8	V
I_D, I_O	Drain/Output Current - Continuous - Pulsed	0.68	-0.46	A
		2	-1.5	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.9		W
		0.7		
T_J, T_{STG}	Operating and Storage Temperature Ranges	-55 to 150		$^\circ C$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6		kV

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ C/W$

Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	25			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-25			
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	N-Ch		26		$\text{mV}/^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	P-Ch		-22		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V},$ $T_J = 55^\circ\text{C}$	N-Ch			1	μA
						10	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V},$ $T_J = 55^\circ\text{C}$	P-Ch			-1	μA
						-10	
I_{GSS}	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	N-Ch			100	nA
		$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	P-Ch			-100	
ON CHARACTERISTICS (Note 2)							
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	N-Ch		-2.6		$\text{mV}/^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$	P-Ch		2.1		
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.65	0.8	1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.65	-0.86	-1.5	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$ $T_J = 125^\circ\text{C}$	N-Ch		0.33	0.45	Ω
					0.51	0.72	
		$V_{GS} = 2.7\text{ V}, I_D = 0.25\text{ A}$			0.44	0.6	
		$V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$ $T_J = 125^\circ\text{C}$	P-Ch		0.87	1.1	
			1.21	1.8			
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	1			A
		$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-1			
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}$	N-Ch		1.45		S
		$V_{DS} = -5\text{ V}, I_D = -0.5\text{ A}$	P-Ch		0.8		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$	N-Ch		50		pF
			P-Ch		63		
C_{oss}	Output Capacitance	$f = 1.0\text{ MHz}$ P-Channel	N-Ch		28		pF
			P-Ch		34		
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		9		pF
			P-Ch		10		

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

SWITCHING CHARACTERISTICS (Note 2)

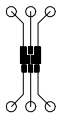
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
t _{D(on)}	Turn - On Delay Time	N-Channel V _{DD} = 6 V, I _D = 0.5 A,	N-Ch		3	6	nS
			P-Ch		7	20	
t _r	Turn - On Rise Time	V _{GS} = 4.5 V, R _{GEN} = 50 Ω	N-Ch		8	16	nS
			P-Ch		9	18	
t _{D(off)}	Turn - Off Delay Time	P-Channel V _{DD} = -6 V, I _D = -0.5 A,	N-Ch		17	30	nS
			P-Ch		55	110	
t _f	Turn - Off Fall Time	V _{Gen} = -4.5 V, R _{GEN} = 50 Ω	N-Ch		13	25	nS
			P-Ch		35	70	
Q _g	Total Gate Charge	N-Channel V _{DS} = 5 V, I _D = 0.5 A,	N-Ch		1.64	2.3	nC
			P-Ch		1.1	1.5	
Q _{gs}	Gate-Source Charge	V _{GS} = 4.5 V	N-Ch		0.38		nC
			P-Ch		0.32		
Q _{gd}	Gate-Drain Charge	V _{DS} = -5 V, I _D = -0.25 A, V _{GS} = -4.5 V	N-Ch		0.45		nC
			P-Ch		0.25		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

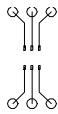
I _S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.3	A
			P-Ch			-0.5	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.5 A (Note)	N-Ch		0.83	1.2	V
				T _J = 125°C	0.69	0.85	
		V _{GS} = 0 V, I _S = -0.5 A (Note)	P-Ch		-0.89	-1.2	
				T _J = 125°C	-0.75	-0.85	

Notes:

- R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{JA} is guaranteed by design while R_{JCA} is determined by the user's board design.
- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.



a. 140°C/W on a 0.125 in² pad of 2oz copper.



b. 180°C/W on a 0.005 in² of pad of 2oz copper.

Typical Electrical Characteristics: N-Channel

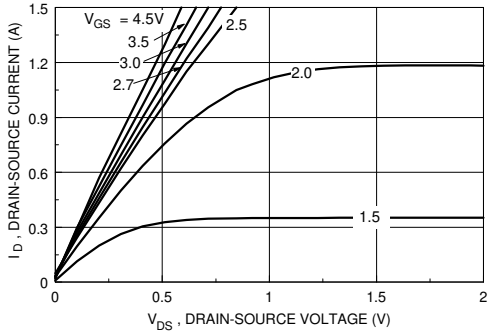


Figure 1. On-Region Characteristics.

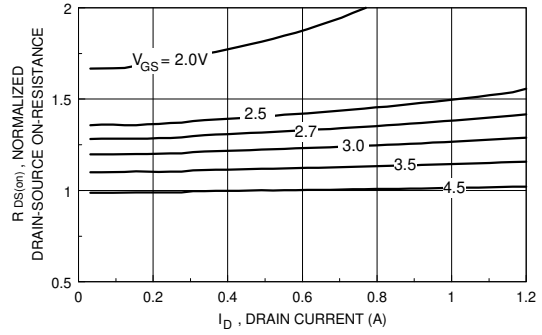


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

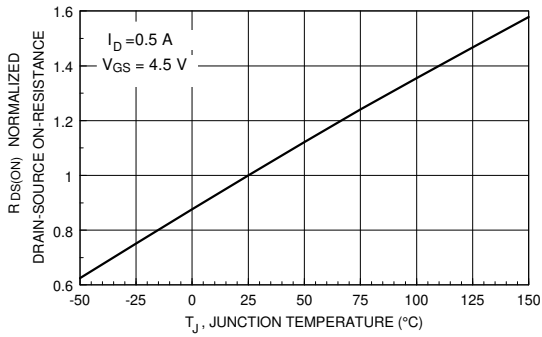


Figure 3. On-Resistance Variation with Temperature.

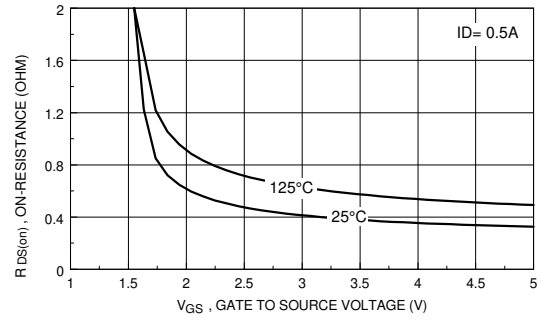


Figure 4. On Resistance Variation with Gate-To-Source Voltage.

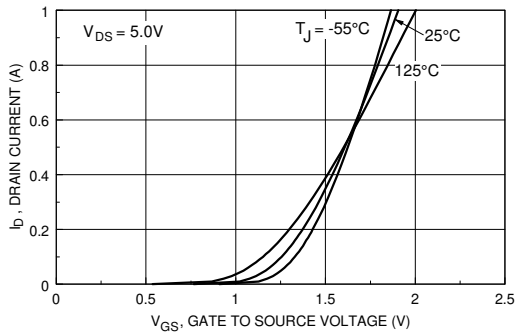


Figure 5. Transfer Characteristics.

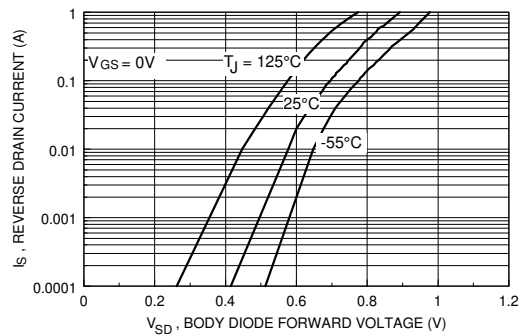


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

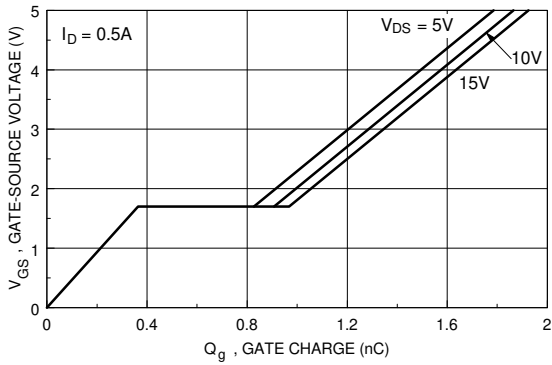


Figure 7. Gate Charge Characteristics.

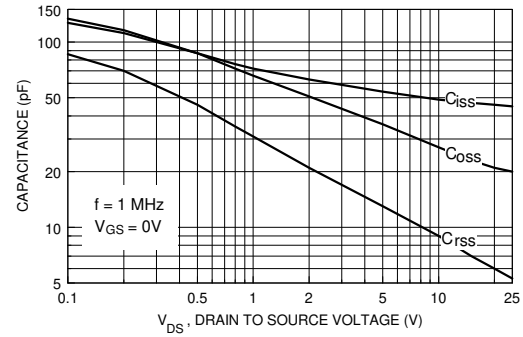


Figure 8. Capacitance Characteristics.

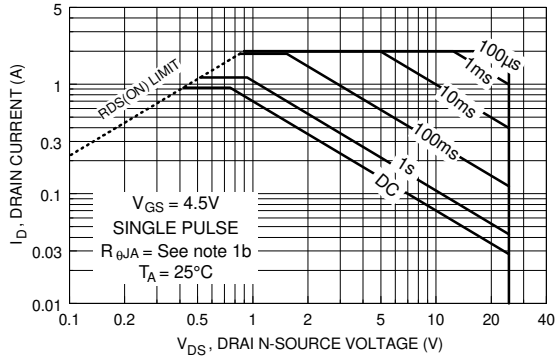


Figure 9. Maximum Safe Operating Area.

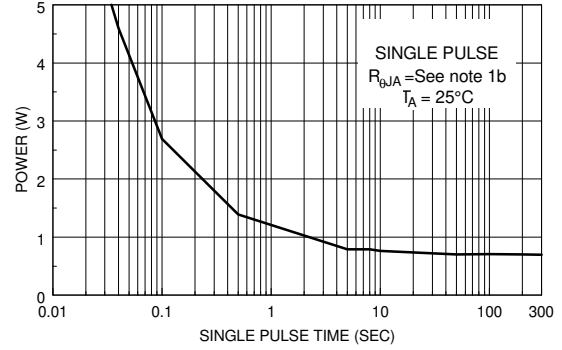


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

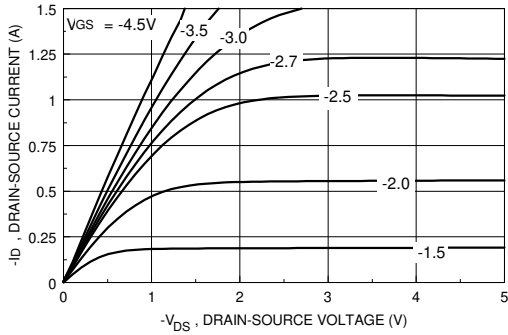


Figure 11. On-Region Characteristics.

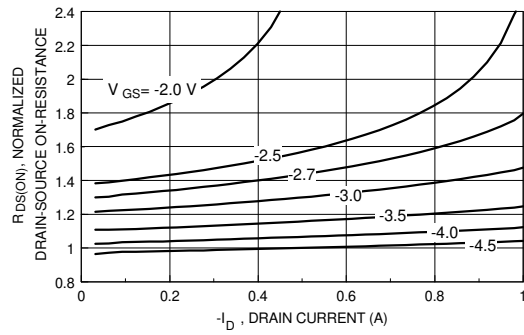


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

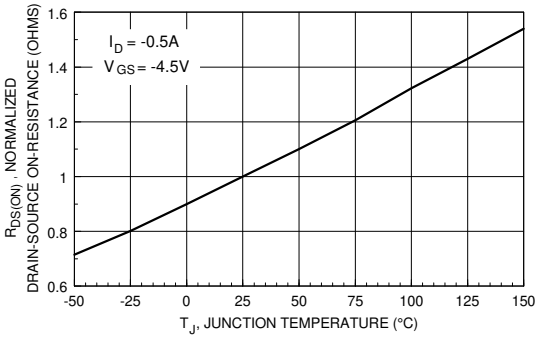


Figure 13. On-Resistance Variation with Temperature.

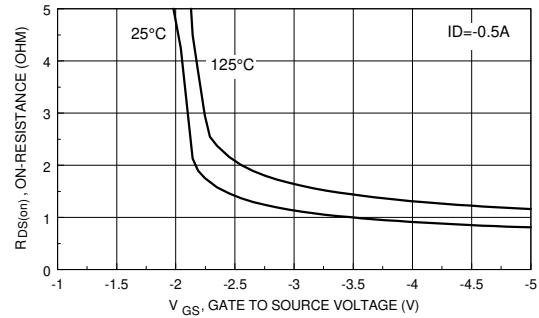


Figure 14. On Resistance Variation with Gate-To- Source Voltage.

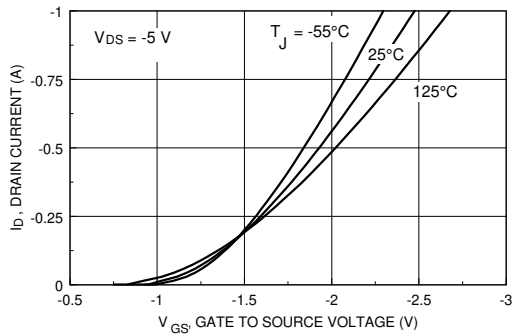


Figure 15. Transfer Characteristics.

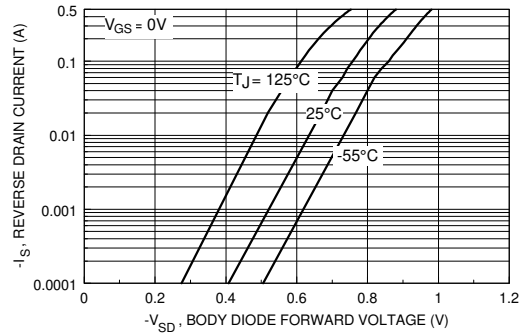


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

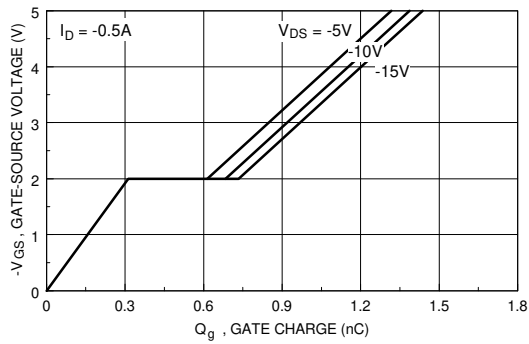


Figure 17. Gate Charge Characteristics.

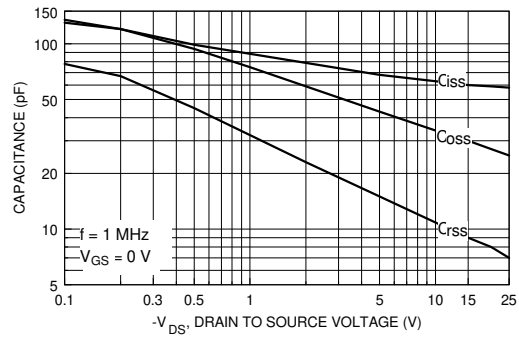


Figure 18. Capacitance Characteristics.

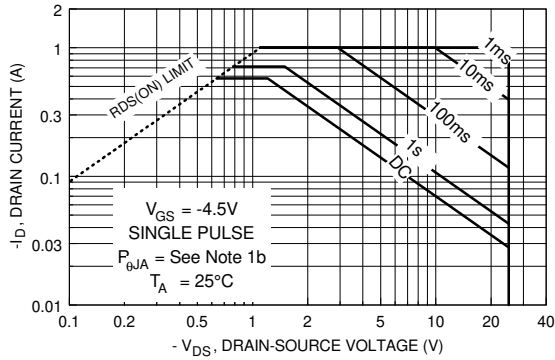


Figure 19. Maximum Safe Operating Area.

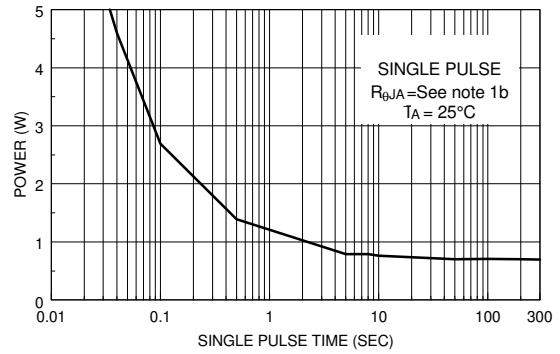


Figure 20. Single Pulse Maximum Power Dissipation.

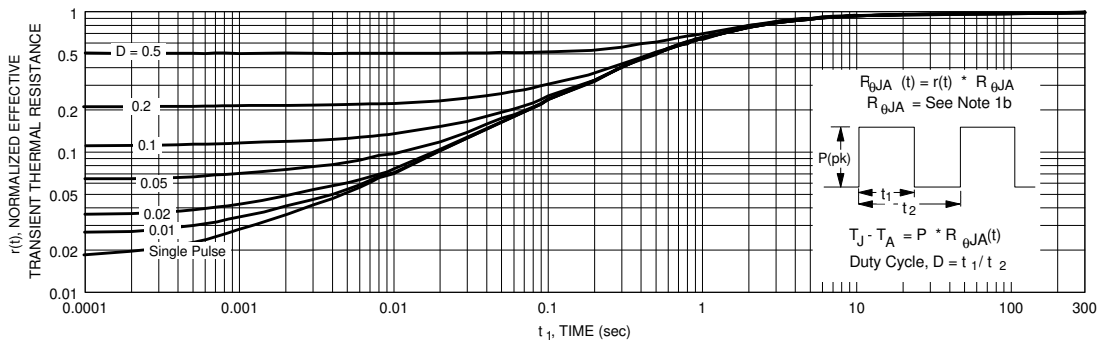


Figure 21. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

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