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March 1999

FAIRCHILD SEMICONDUCTOR™

FDC6324L
Integrated Load Switch

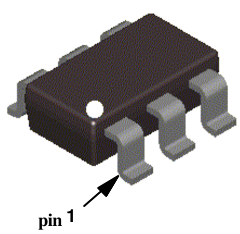
General Description

These Integrated Load Switches are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage high side load switch application where low conduction loss and ease of driving are needed.

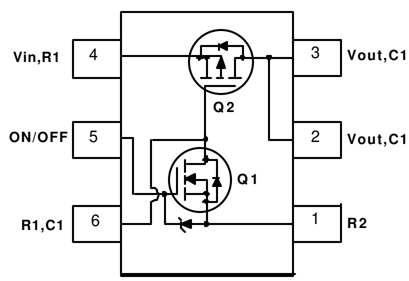
Features

- V_{DROP}=0.2V @ V_{IN}=12V, I_L=1A, $V_{ON/OFF}$=1.5 to 8V
  V_{DROP}=0.3V @ V_{IN}=5V, I_L=1A, $V_{ON/OFF}$=1.5 to 8V.
- High density cell design for extremely low on-resistance.
- $V_{ON/OFF}$ Zener protection for ESD ruggedness. >6KV Human Body Model.
- SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.

SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16

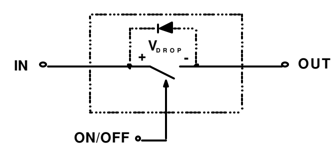


SuperSOT ™-6



See Application Circuit

EQUIVALENT CIRCUIT



Absolute Operating Range T_A = 25°C unless otherwise noted

Symbol	Parameter	FDC6324L	Units
V_{IN}	Input Voltage Range	3 - 20	V
$V_{ON/OFF}$	ON/OFF Voltage Range	1.5 - 8	V
I_L	Load Current @ V_{DROP}=0.5V - Continuous (Note 1)	1.5	A
	- Pulsed (Note 1 & 3)	2.5	
P_D	Maximum Power Dissipation (Note 2a)	0.7	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf/1500Ohm)	6	kV
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 2a)	180	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	60	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
I_{FL}	Forward Leakage Current	V_{IN} = 20 V, $V_{ON/OFF}$ = 0 V			1	μA
I_{RL}	Reverse Leakage Current	V_{IN} = -20 V, $V_{ON/OFF}$ = 0 V			-1	μA
ON CHARACTERISTICS (Note 3)						
V_{IN}	Input Voltage		3		20	V
$V_{ON/OFF}$	On/Off Voltage		1.5		8	V
V_{DROP}	Conduction Voltage Drop @ 1A	V_{IN} = 10 V, $V_{ON/OFF}$ = 3.3V		0.135	0.2	V
		V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V		0.215	0.3	
I_L	Load Current	V_{DROP} = 0.2 V, V_{IN} = 10 V, $V_{ON/OFF}$ = 3.3 V	1			A
		V_{DROP} = 0.3 V, V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V	1			

Notes:

1. V_{IN}=20V, $V_{ON/OFF}$=8V, V_{DROP}=0.5V, T_A=25°C

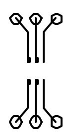
2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on FR-4 PCB in astill air environment:

a. 180°C/W when mounted on a 2oz minimum copper pad.

2a



Scale 1 : 1 on letter size paper

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%

Typical Electrical Characteristics (T_A = 25 °C unless otherwise noted)

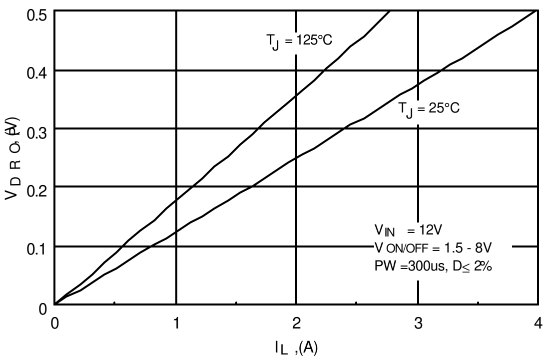


Figure 1. V_{DROP} Versus I_L at V_{IN}=12V.

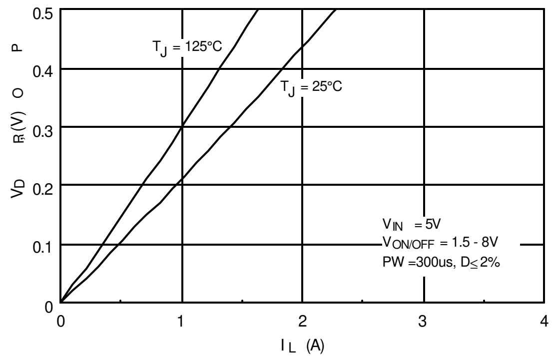


Figure 2. V_{DROP} Versus I_L at V_{IN}=5.0V.

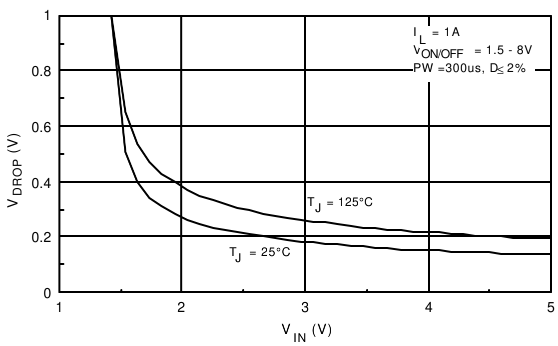


Figure 3. V_{DROP} Versus V_{IN} at I_L=1A.

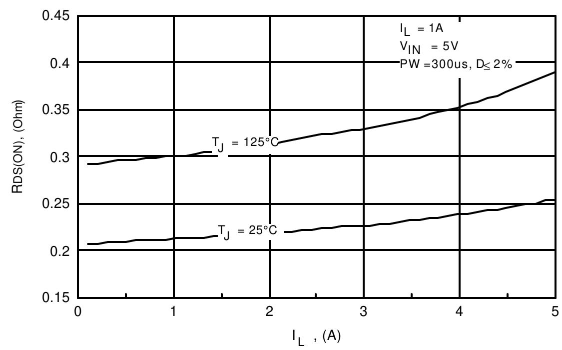


Figure 4. $R_{(ON)}$ Versus I_L at V_{IN}=5.0V.

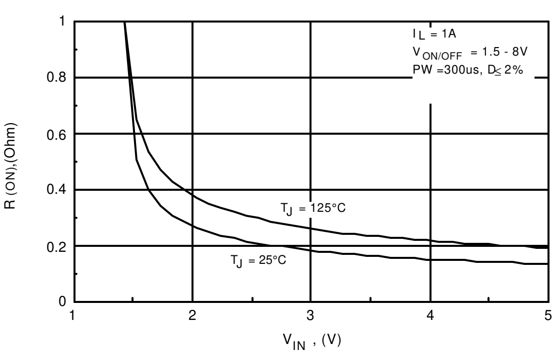


Figure 5. On Resistance Variation with Input Voltage.

Typical Electrical Characteristics (T$_A$ = 25 °C unless otherwise noted)

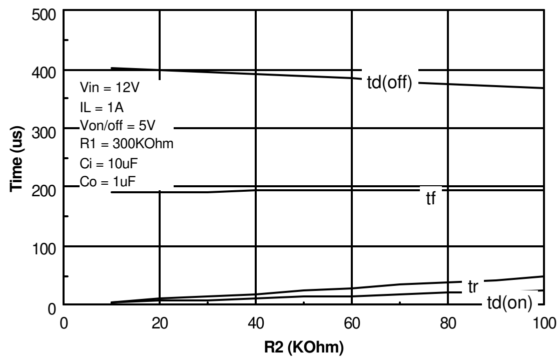


Figure 6. Switching Variation with R2 at Vin= 12V and R1= 300KOhm.

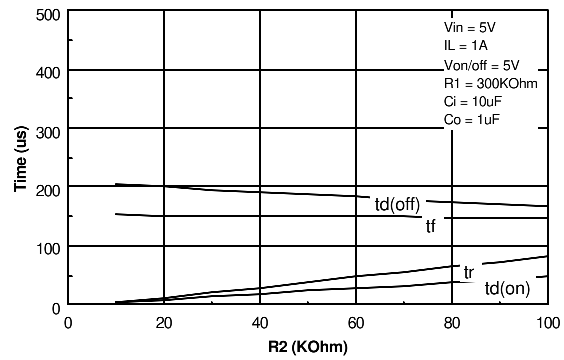


Figure 7. Switching Variation with R2 at Vin=5V and R1=300KOhm.

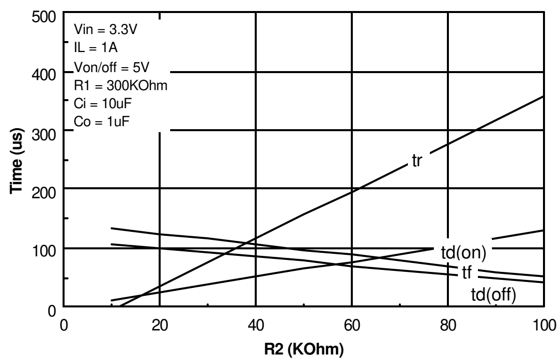


Figure 8. Switching Variation with R2 at Vin=3.3V and R1=300KOhm.

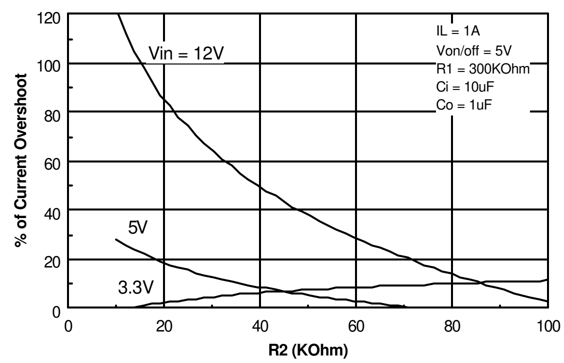


Figure 9. % of Current Overshoot Variation with Vin and R2.

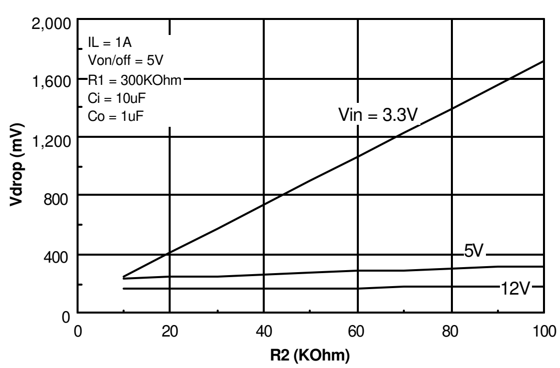


Figure 10. Vdrop Variation with Vin and R2.

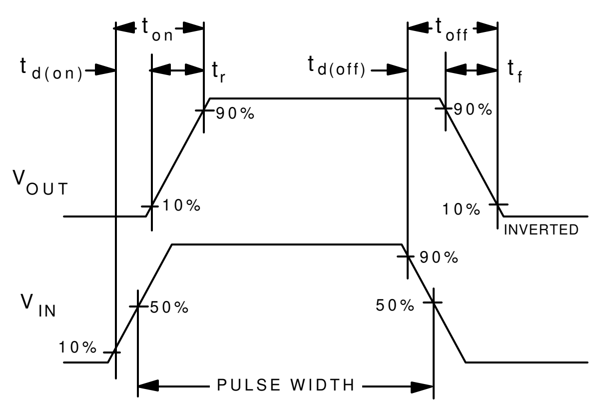


Figure 11. Switching Waveforms.

Typical Electrical Characteristics (T_A = 25 °C unless otherwise noted)

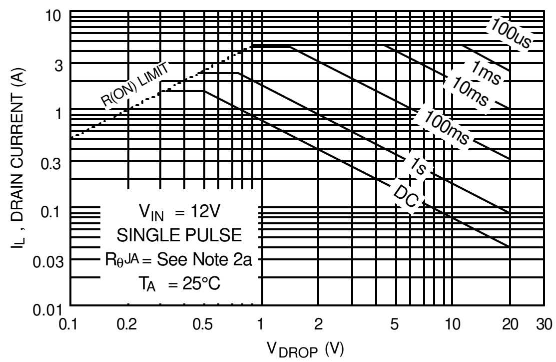


Figure 12. Safe Operating Area.

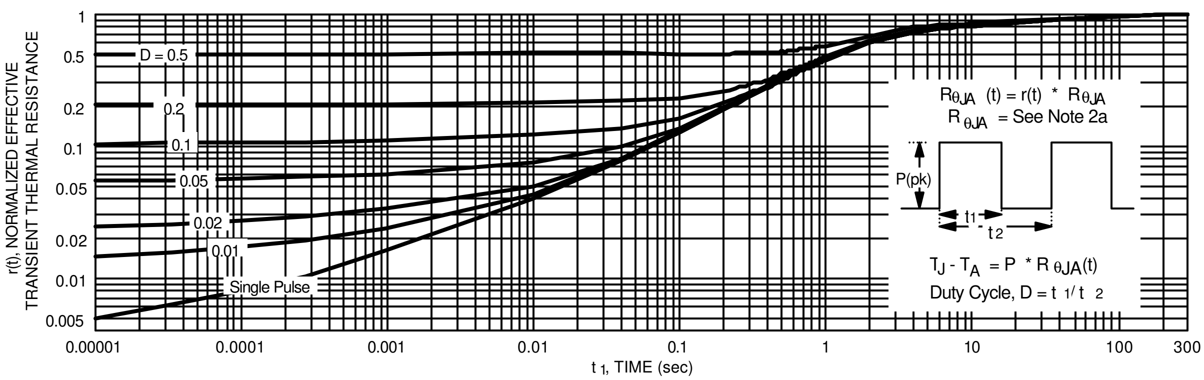
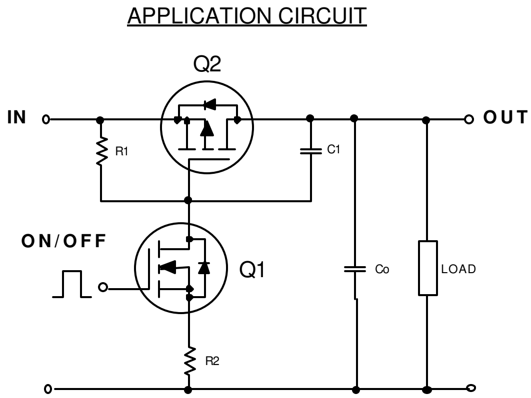


Figure 13. Transient Thermal Response Curve.

Note: Thermal characterization performed on the conditions described in Note 2a. Transient thermal response will change depends on the circuit board

FDC6324L Load Switch Application



General Description

This device is particularly suited for computer peripheral switching applications where 20V input and 1A output current capability are needed. This load switch integrates a small N-Channel Power MOSFET (Q1) which drives a large P-Channel Power MOSFET (Q2) in one tiny SuperSOT™-6 package.

A load switch is usually configured for high side switching so that the load can be isolated from the active power source. A P-Channel Power MOSFET, because it does not require its drive voltage above the input voltage, is usually more cost effective than using an N-Channel device in this particular application. A large P-Channel Power MOSFET minimizes voltage drop. By using a small N-Channel device the driving stage is simplified.

Component Values

R1	Typical	10k - 1MΩ	
R2	Typical	0 - 10kΩ	(optional)
C1	Typical	1000pF	(optional)

Design Notes

- R1 is needed to turn off Q2.
- R2 can be used to soft start the switch in the case the output capacitance Co is small.
- R2 ≤ should be at least 10 times smaller than R1 to guarantee Q1 turns on.
- By using R1 and R2 a certain amount of current is lost from the input. This bias current loss is given by the equation

  $I_{BIAS\_LOSS} = \frac{Vin}{R1 + R2}$ when the switch is ON. I_{BIAS_LOSS} can be minimized by large R1.

- R2 and C_{RSS} of Q2 make ramp for slow turn on. If excessive overshoot current occurs due to fast turn on, additional capacitance C1 can be added externally to slow down the turn on.

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