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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

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# FDD3510H

## Dual N & P-Channel PowerTrench<sup>®</sup> MOSFET

N-Channel: 80V, 13.9A, 80mΩ P-Channel: -80V, -9.4A, 190mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 80mΩ at  $V_{GS} = 10V, I_D = 4.3A$
- Max  $r_{DS(on)}$  = 88mΩ at  $V_{GS} = 6V, I_D = 4.1A$

Q2: P-Channel

- Max  $r_{DS(on)}$  = 190mΩ at  $V_{GS} = -10V, I_D = -2.8A$
- Max  $r_{DS(on)}$  = 224mΩ at  $V_{GS} = -4.5V, I_D = -2.6A$
- 100% UIL Tested
- RoHS Compliant

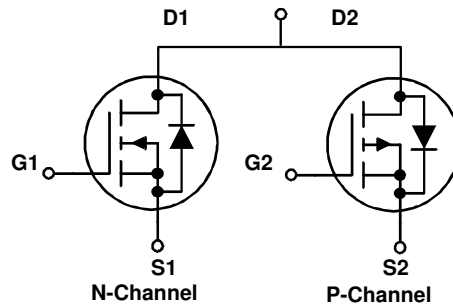
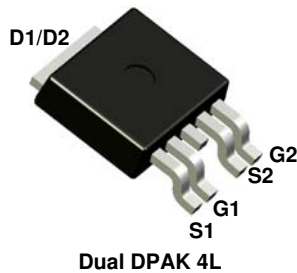


### General Description

These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

### Applications

- Inverter
- H-Bridge



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	80	-80	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current - Continuous $T_C = 25^\circ\text{C}$	13.9	-9.4	A
	- Continuous $T_A = 25^\circ\text{C}$	4.3	-2.8	
	- Pulsed	20	-10	
$P_D$	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$ (Note 1)	35	32	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.1		
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3		
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	37	54	mJ
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1)	3.5	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1)	3.9	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3510H	FDD3510H	TO-252-4L	13"	16mm	2500 units

FDD3510H Dual N & P-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q1 Q2	80 -80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		84 -67	mV	$^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = -64\text{V}, V_{GS} = 0\text{V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q1 Q2	2.0 -1.0	2.6 -1.6	4.0 -3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$ $I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	Q1 Q2		-6.7 4.6	mV	$^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4.3\text{A}$ $V_{GS} = 6.0\text{V}, I_D = 4.1\text{A}$ $V_{GS} = 10\text{V}, I_D = 4.3\text{A}, T_J = 125^\circ\text{C}$	Q1		64 70 121	80 88 152	m $\Omega$
		$V_{GS} = -10\text{V}, I_D = -2.8\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -2.6\text{A}$ $V_{GS} = -10\text{V}, I_D = -2.8\text{A}, T_J = 125^\circ\text{C}$	Q2		153 184 259	190 224 322	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{V}, I_D = 4.3\text{A}$ $V_{DD} = -5\text{V}, I_D = -2.8\text{A}$	Q1 Q2		15 6.8		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		600 660	800 880	pF
$C_{oss}$	Output Capacitance	Q2	Q1 Q2		56 50	75 70	pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		27 25	41 40	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$	Q1 Q2		1.7 7.2		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1 $V_{DD} = 40\text{V}, I_D = 4.3\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	Q1 Q2		7 6	13 11	ns
$t_r$	Rise Time		Q1 Q2		2 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -40\text{V}, I_D = -2.8\text{A}$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	Q1 Q2		16 25	29 40	ns
$t_f$	Fall Time		Q1 Q2		2 5	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 $V_{GS} = 10\text{V}, V_{DD} = 40\text{V}, I_D = 4.3\text{A}$	Q1 Q2		13 14	18 20	nC
$Q_{gs}$	Gate to Source Charge		Q1 Q2		2.3 1.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	Q2 $V_{GS} = -10\text{V}, V_{DD} = -40\text{V}, I_D = -2.8\text{A}$	Q1 Q2		3.2 2.9		nC

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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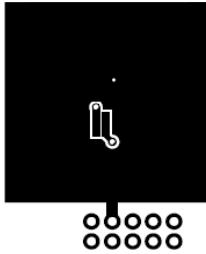
### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.6\text{A}$ (Note 2)	Q1	0.8	1.2	V
		$V_{GS} = 0\text{V}, I_S = -2.6\text{A}$ (Note 2)	Q2	-0.8	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 4.3\text{A}, di/dt = 100\text{A/s}$	Q1	29	46	ns
			Q2	30	48	
$Q_{rr}$	Reverse Recovery Charge	$I_F = -2.8\text{A}, di/dt = 100\text{A/s}$	Q1	28	45	nC
			Q2	30	48	

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

Q1



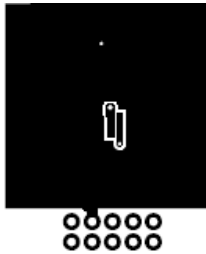
a.  $40^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper

Scale 1 : 1 on letter size paper



b.  $96^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

Q2



a.  $40^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper

Scale 1 : 1 on letter size paper



b.  $96^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

- Starting  $T_J = 25^\circ\text{C}$ , N-ch:  $L = 3\text{mH}, I_{AS} = 5\text{A}, V_{DD} = 80\text{V}, V_{GS} = 10\text{V}$ ; P-ch:  $L = 3\text{mH}, I_{AS} = -6\text{A}, V_{DD} = -80\text{V}, V_{GS} = -10\text{V}$ .



**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

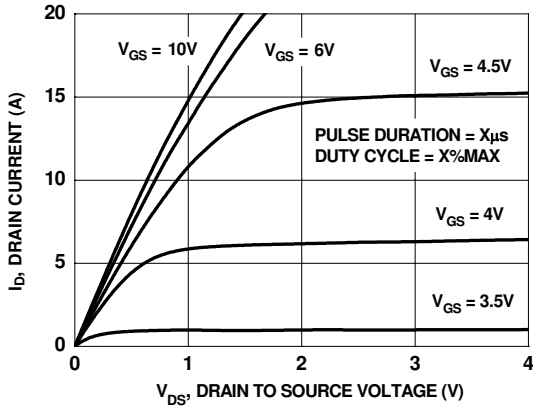


Figure 1. On Region Characteristics

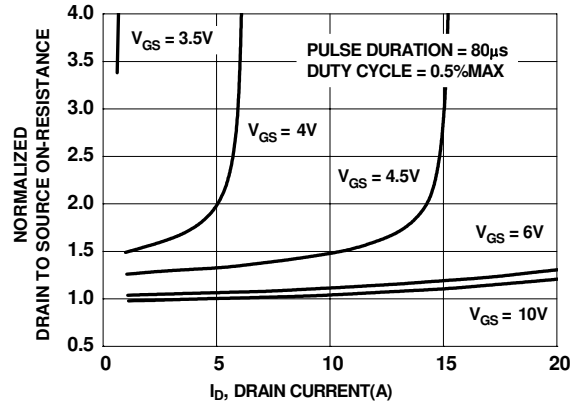


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

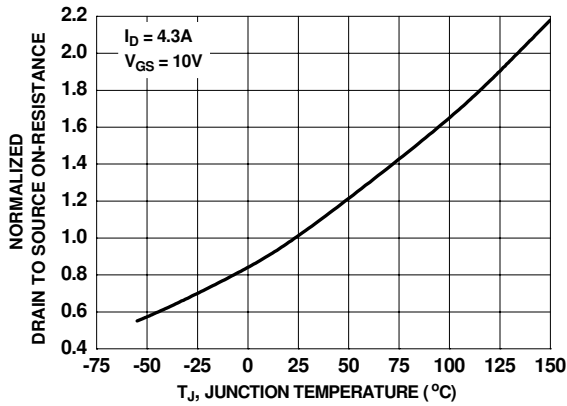


Figure 3. Normalized On Resistance vs Junction Temperature

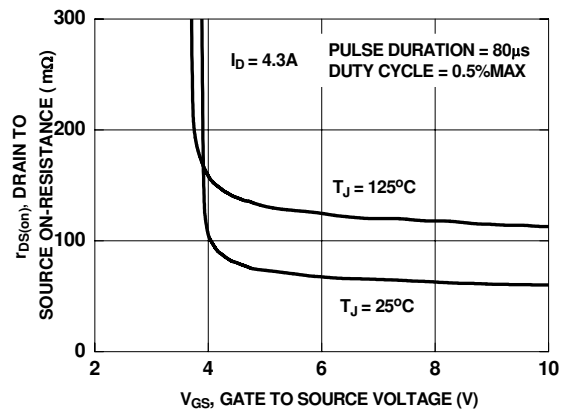


Figure 4. On-Resistance vs Gate to Source Voltage

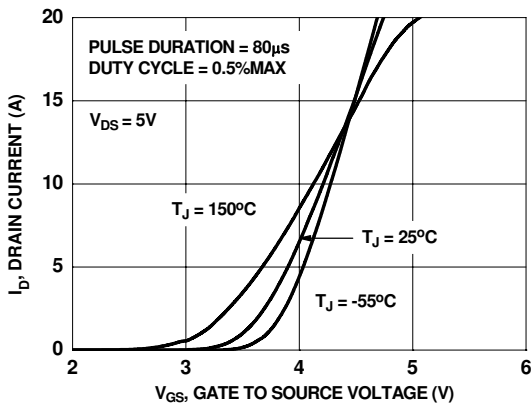


Figure 5. Transfer Characteristics

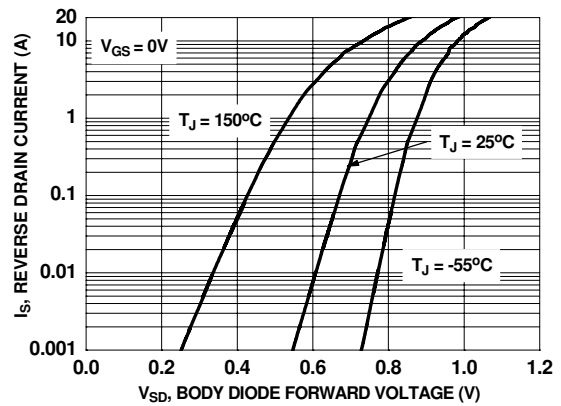
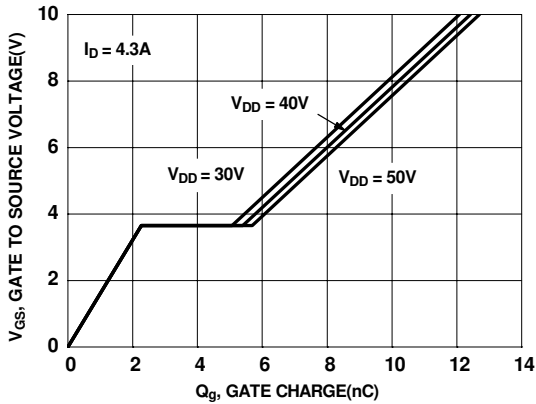
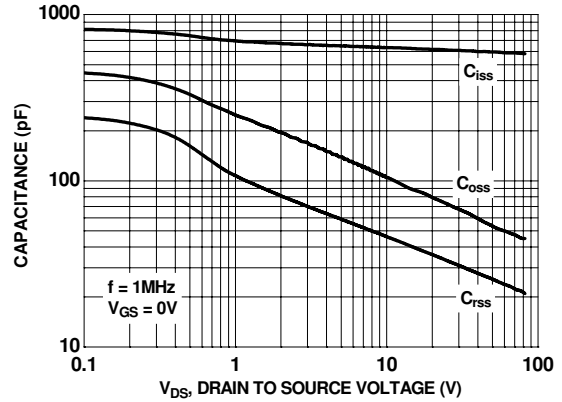


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

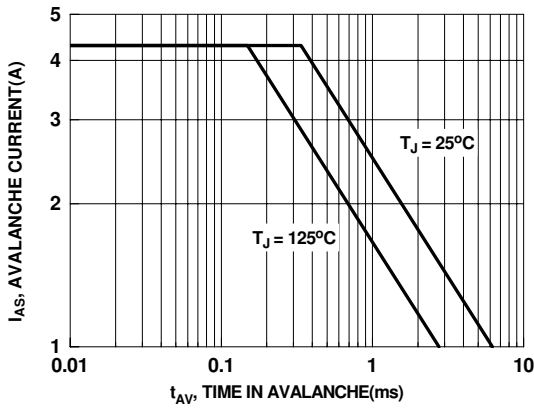
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



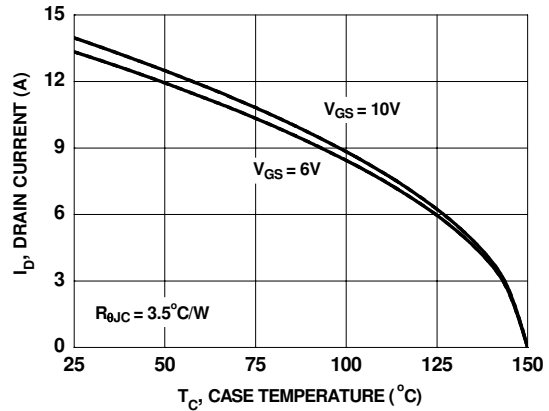
**Figure 7. Gate Charge Characteristics**



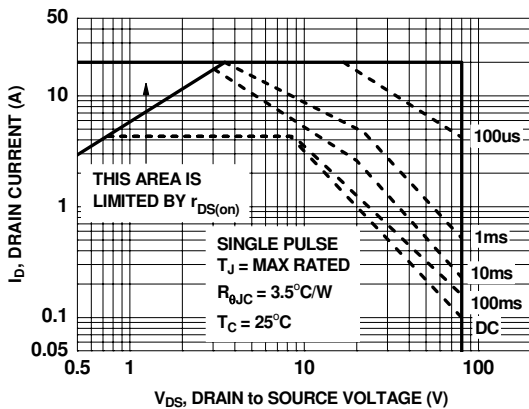
**Figure 8. Capacitance vs Drain to Source Voltage**



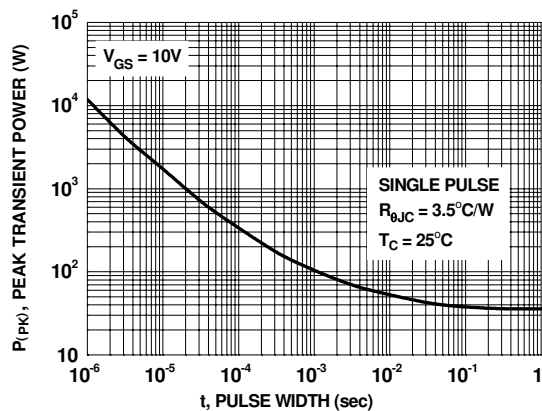
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

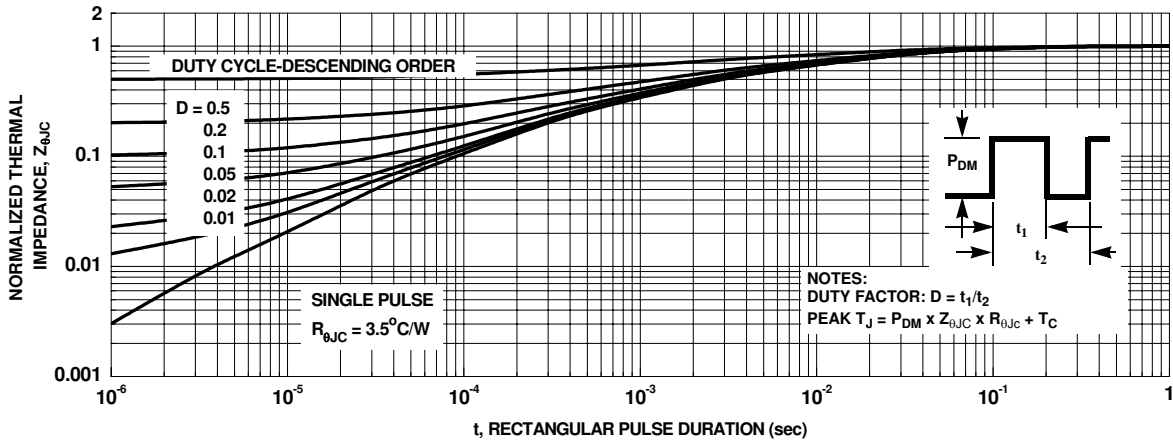


**Figure 11. Forward Bias Safe Operating Area**

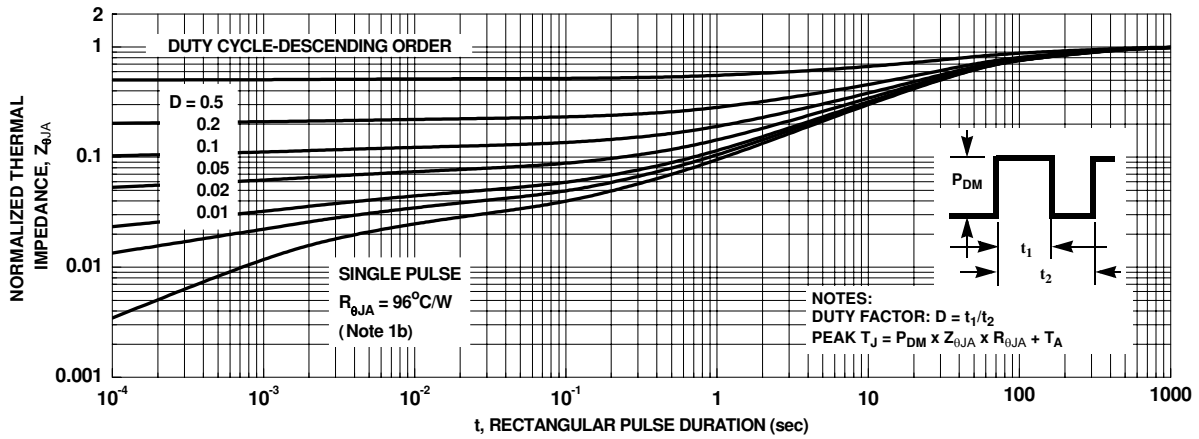


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**



**Figure 14. Transient Thermal Response Curve**



**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

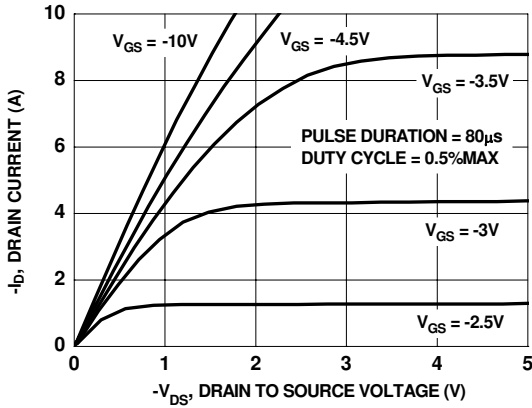


Figure 15. On-Region Characteristics

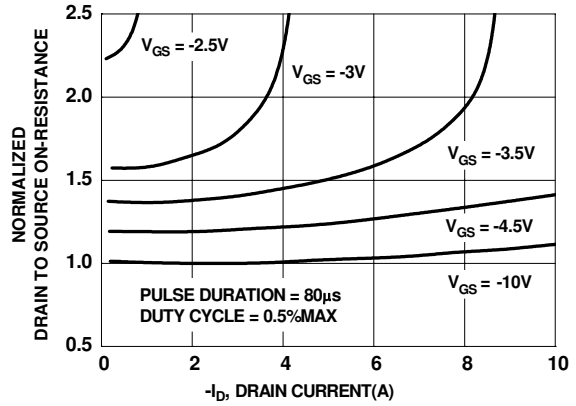


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

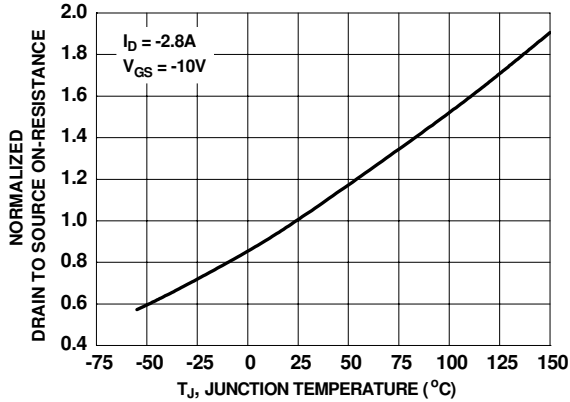


Figure 17. Normalized On-Resistance vs Junction Temperature

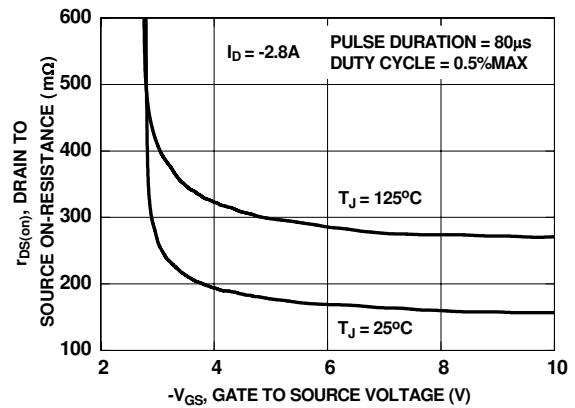


Figure 18. On-Resistance vs Gate to Source Voltage

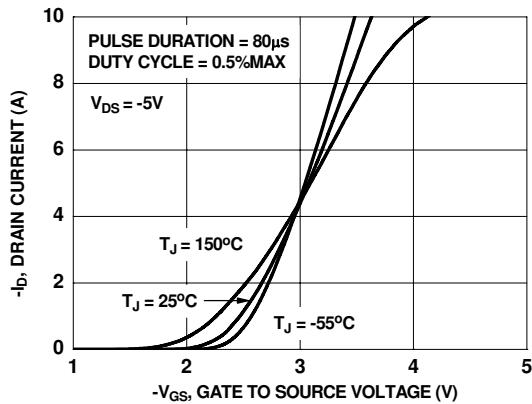


Figure 19. Transfer Characteristics

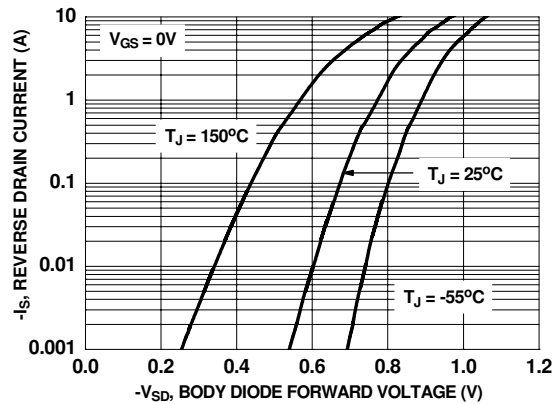
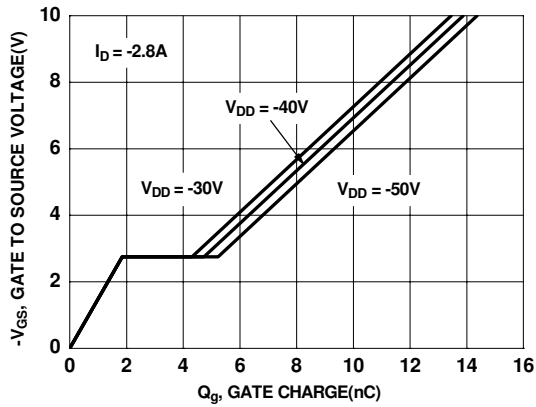
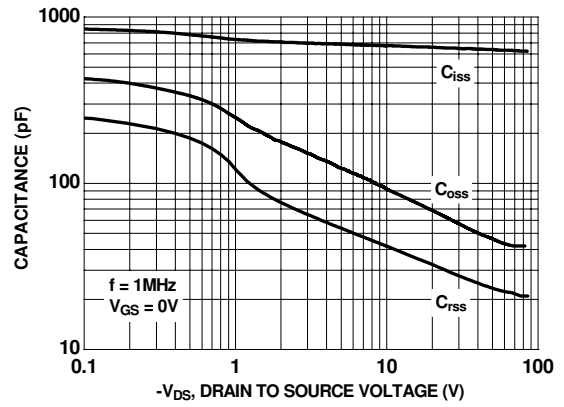


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

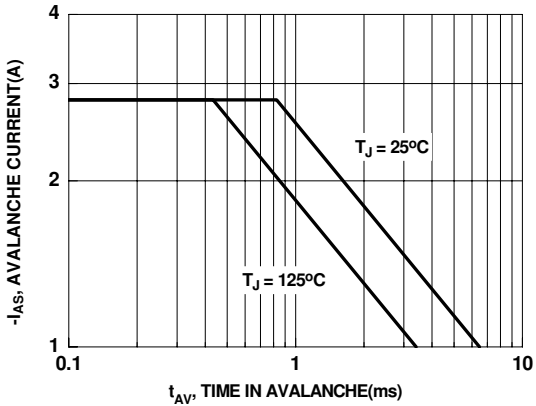
**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



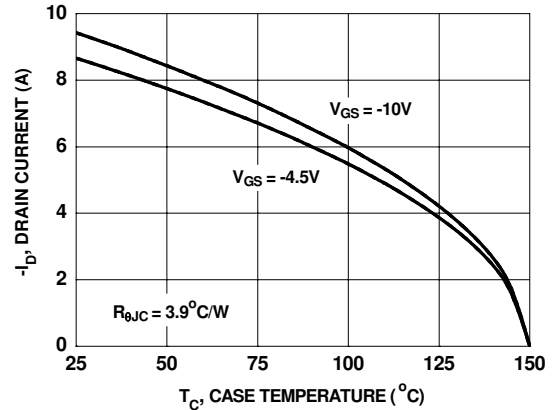
**Figure 21. Gate Charge Characteristics**



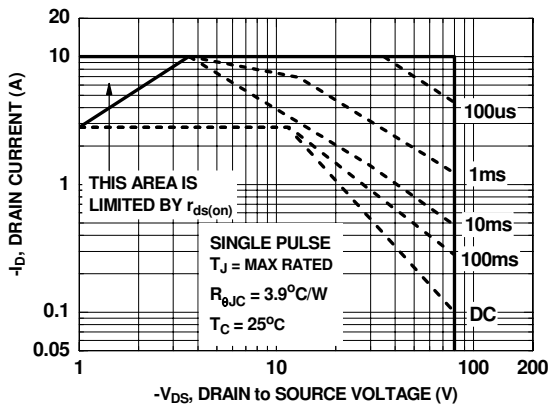
**Figure 22. Capacitance vs Drain to Source Voltage**



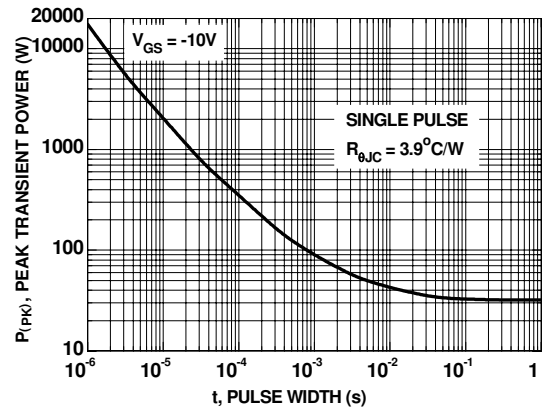
**Figure 23. Unclamped Inductive Switching Capability**



**Figure 24. Maximum Continuous Drain Current vs Case Temperature**

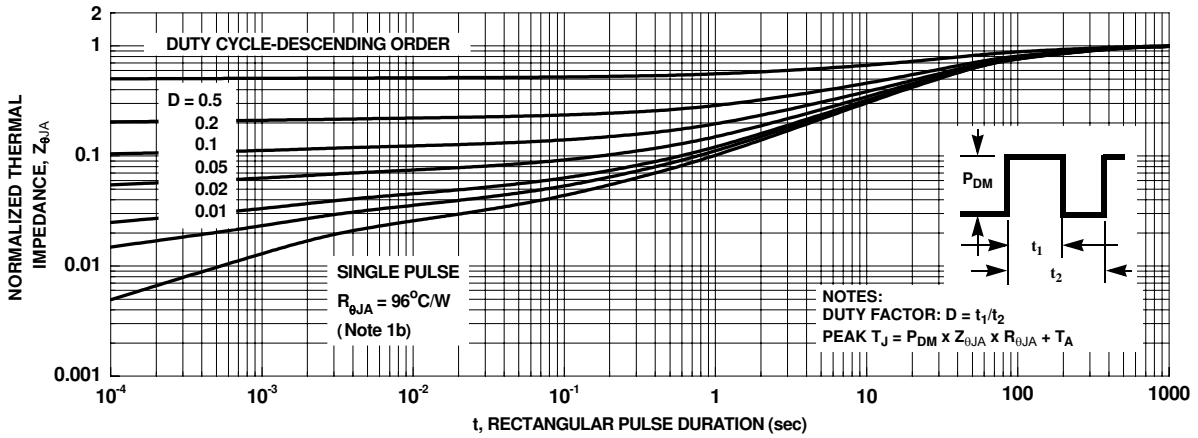
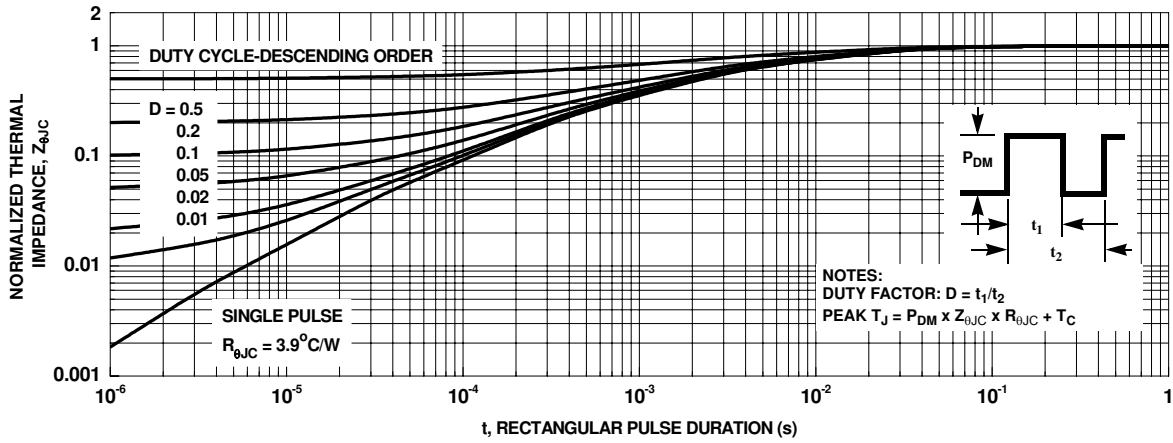


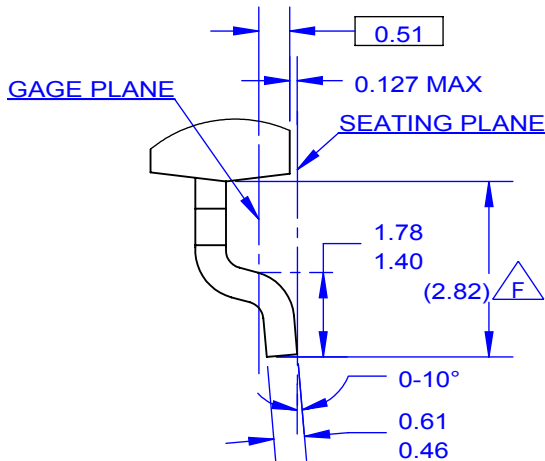
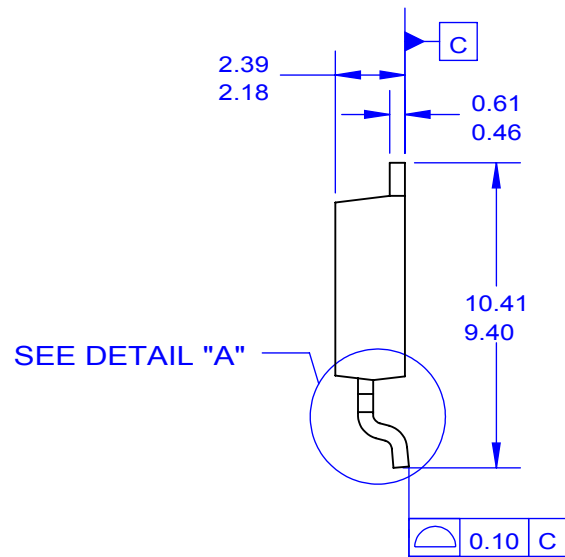
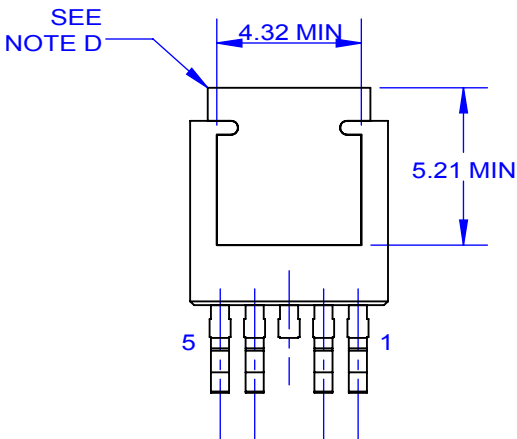
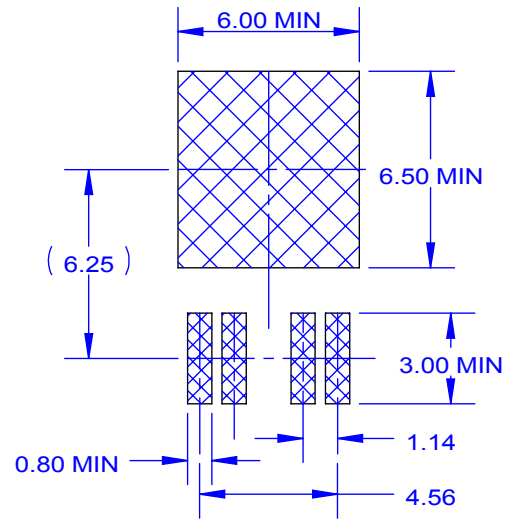
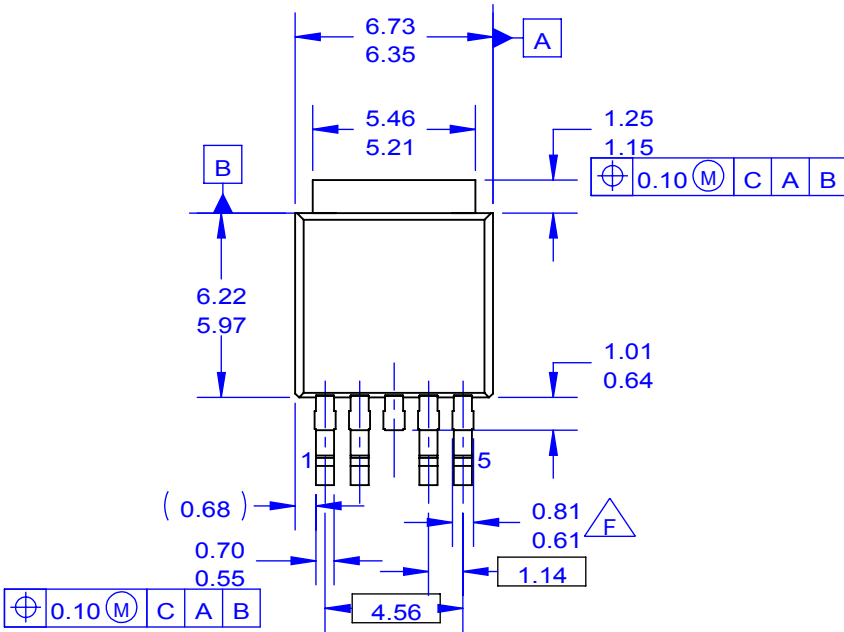
**Figure 25. Forward Bias Safe Operating Area**



**Figure 26. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 P-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted





DETAIL A  
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE CONFORMS TO JEDEC, TO252 VARIATION AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
- D. HEATSINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-2009.
- F. EXCEPTION TO TO-252 STANDARD.
- G. FILE NAME: TO252B05REV3
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