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March 2015

FDD3706/FDU3706

20V N-Channel PowerTrench® MOSFET

General Description

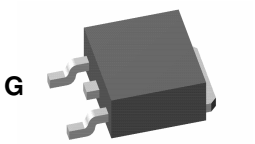
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and extremely low $R_{DS(ON)}$ in a small package.

Applications

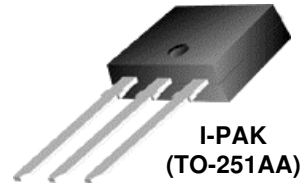
- DC/DC converter
- Motor Drives

Features

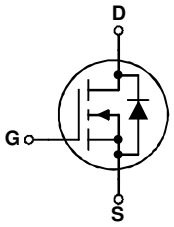
- 50 A, 20 V $R_{DS(ON)}$ = 9 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 11 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 16 mΩ @ V_{GS} = 2.5 V
- Low gate charge (16 nC)
- Fast Switching
- High performance trench technology for extremely low $R_{DS(ON)}$



D-PAK
(TO-252)



I-PAK
(TO-251AA)



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain-Source Voltage			20	V
V_{GSS}	Gate-Source Voltage			±12	V
I_D	Continuous Drain Current	@T_C=25°C	(Note 3)	50	A
		@T_A=25°C	(Note 1a)	14.7	
		Pulsed	(Note 1a)	60	
P_D	Power Dissipation	@T_C=25°C	(Note 3)	44	W
		@T_A=25°C	(Note 1a)	3.8	
		@T_A=25°C	(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD3706	FDD3706	D-PAK (TO-252)	13”	16mm	2500 units
FDU3706	FDU3706	I-PAK (TO-251)	Tube	N/A	75

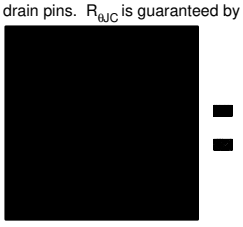
Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
E_{AS}	Drain-Source Avalanche Energy	Single Pulse, V_{DD} = 10V, I_D=7A			60	mJ
I_{AS}	Drain-Source Avalanche Current				7	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA,Referenced to 25°C		13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –12 V V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA,Referenced to 25°C		–3.5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 16.2 A V_{GS} = 4.5 V, I_D = 14.7 A V_{GS} = 2.5 V, I_D = 12.2 A V_{GS} = 4.5 V, I_D = 14.7 A,T_J = 125°C		7.5 8 11 12.6	9 11 16 19	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	30			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 14.7 A		65		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1882		pF
C_{oss}	Output Capacitance			430		pF
C_{rss}	Reverse Transfer Capacitance			201		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn–On Rise Time			15	27	ns
$t_{d(off)}$	Turn–Off Delay Time			35	56	ns
t_f	Turn–Off Fall Time			16	29	ns
Q_g	Total Gate Charge	V_{DS} = 10V, I_D = 14.7 A, V_{GS} = 4.5 V		16	23	nC
Q_{gs}	Gate–Source Charge			3.7		nC
Q_{gd}	Gate–Drain Charge			4		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				3.2	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.2 A (Note 2)		0.7	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in^2 pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A

Typical Characteristics

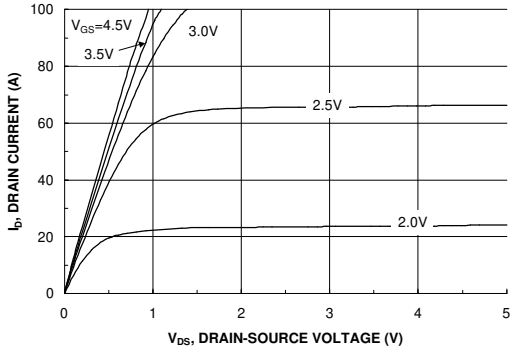


Figure 1. On-Region Characteristics

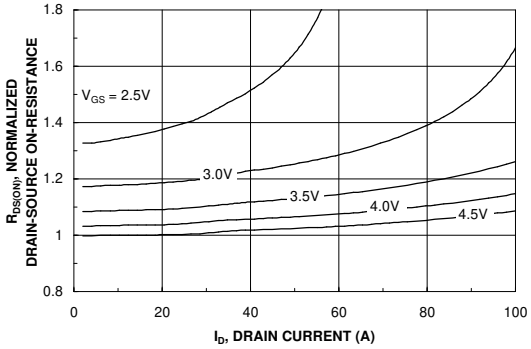


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

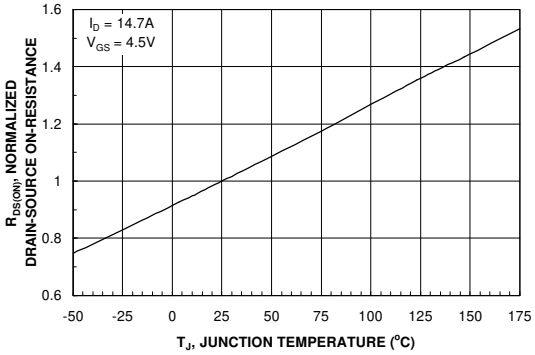


Figure 3. On-Resistance Variation withTemperature

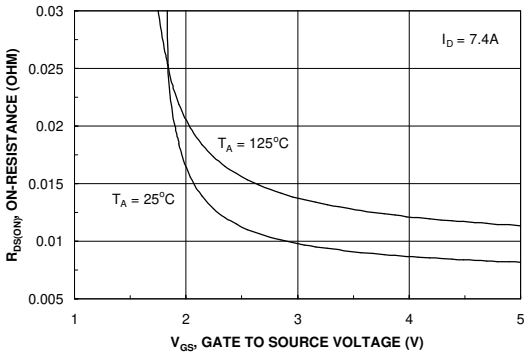


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

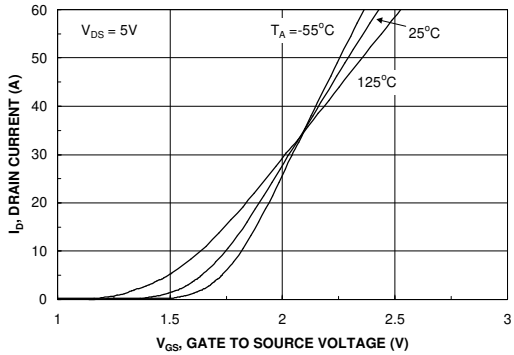


Figure 5. Transfer Characteristics

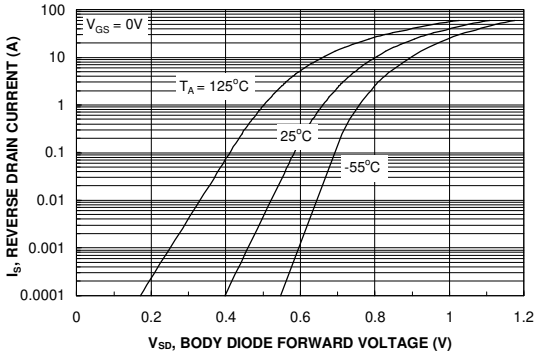


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

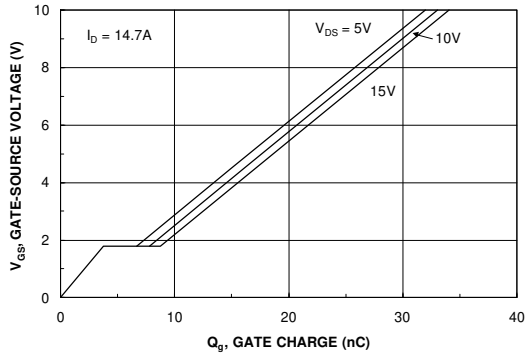


Figure 7. Gate Charge Characteristics

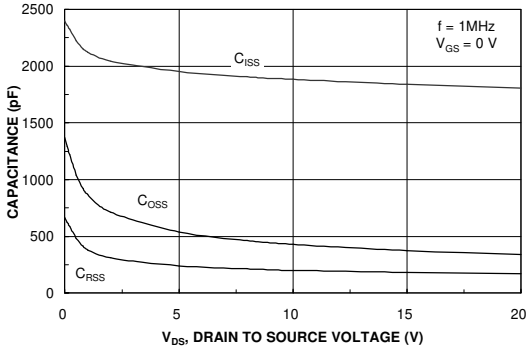


Figure 8. Capacitance Characteristics

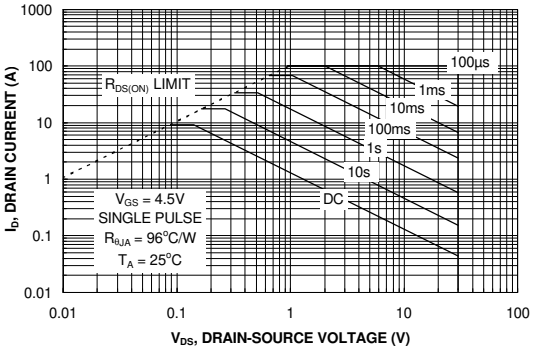


Figure 9. Maximum Safe Operating Area

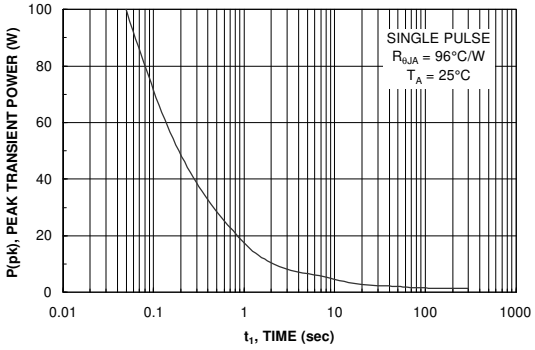


Figure 10. Single Pulse Maximum Power Dissipation

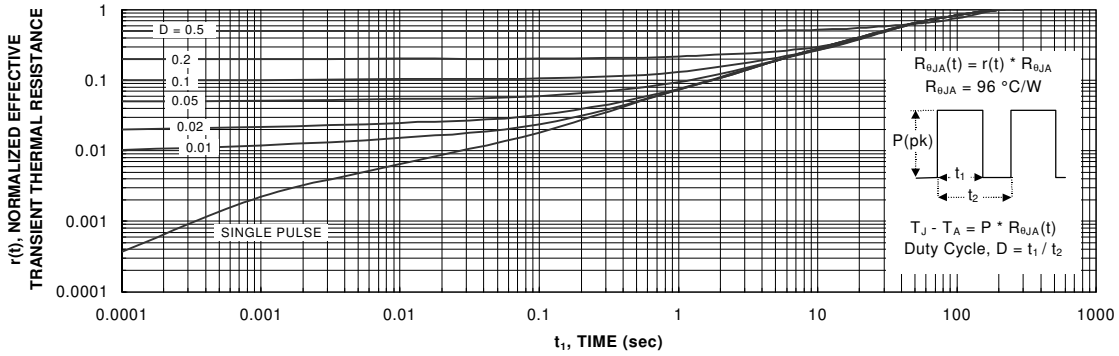
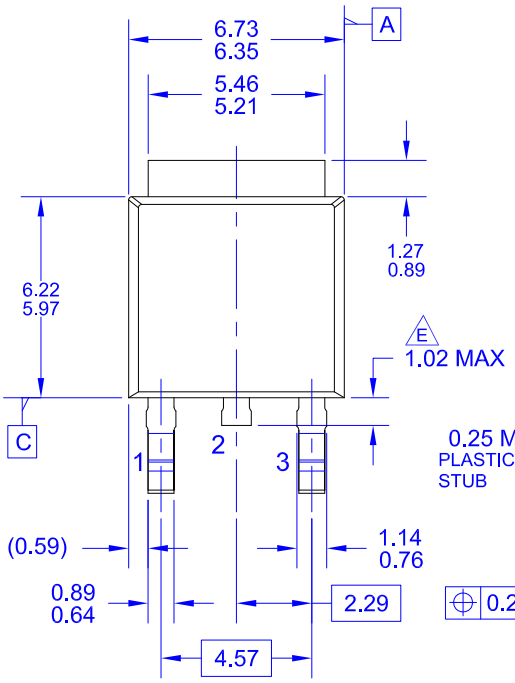
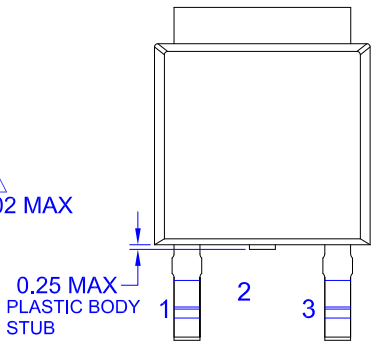


Figure 11. Transient Thermal Response Curve

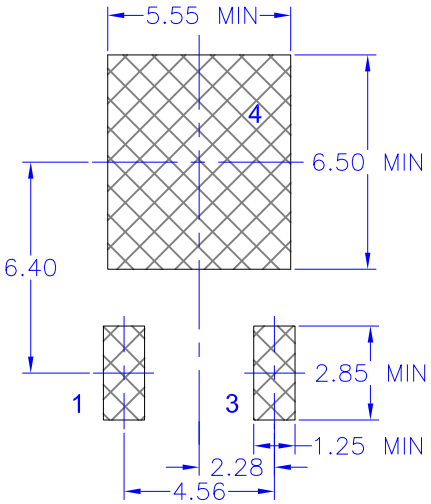
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



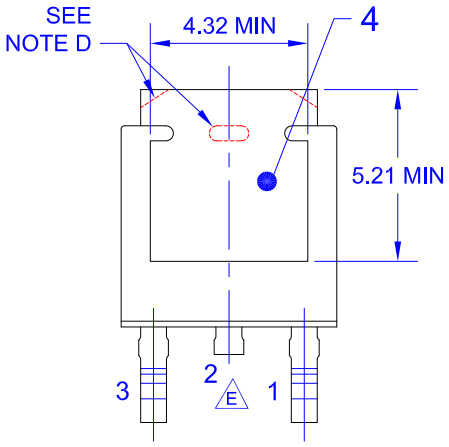
NON-DIODE PRODUCTS VERSION



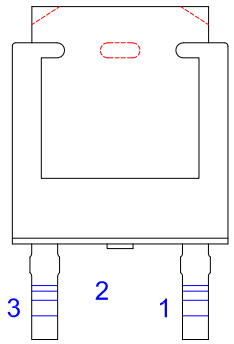
DIODE PRODUCTS VERSION



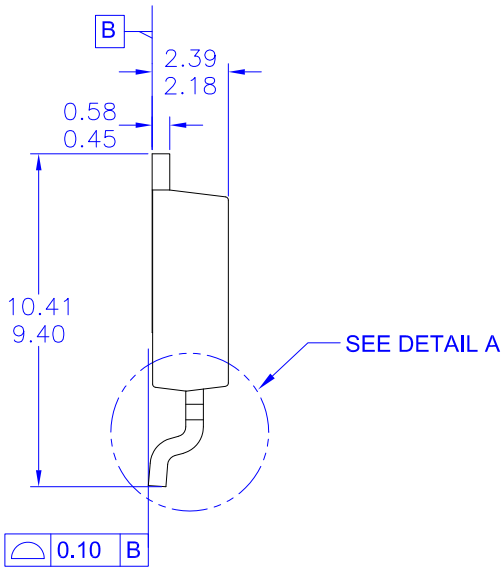
LAND PATTERN RECOMMENDATION



NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



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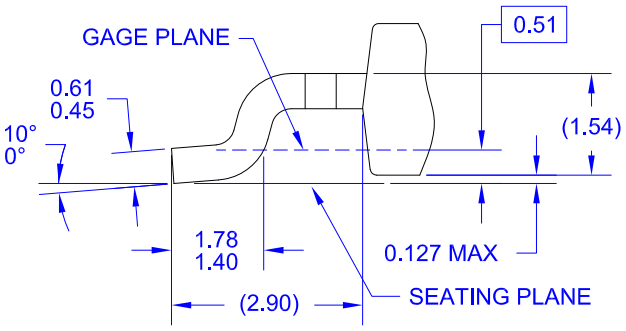
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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