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# FDD4243\_F085

## P-Channel PowerTrench<sup>®</sup> MOSFET

### -40V, -14A, 64mΩ

#### Features

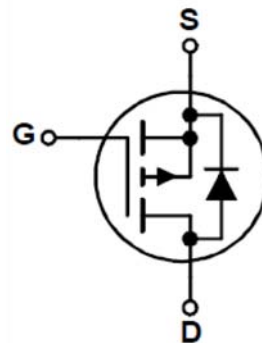
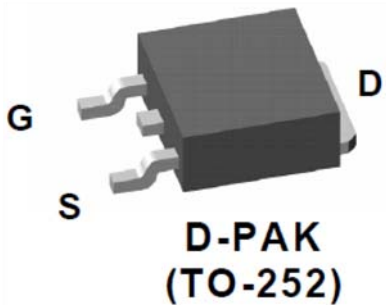
- Typ  $r_{DS(on)}$  = 36mΩ at  $V_{GS} = -10V$ ,  $I_D = -6.7A$
- Typ  $r_{DS(on)}$  = 48mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -5.5A$
- Typ  $Q_{g(TOT)}$  = 21nC at  $V_{GS} = -10V$
- High performance trench technology for extremely low  $r_{DS(on)}$
- RoHS Compliant
- Qualified to AEC Q101

#### Applications

- Inverter
- Power Supplies



FDD4243\_F085 P-Channel PowerTrench<sup>®</sup> MOSFET



## MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	-40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current Continuous ( $T_C < 130^\circ\text{C}$ , $V_{GS} = 10\text{V}$ )	-14	A
	Pulsed	See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	84	mJ
$P_D$	Power Dissipation	50	W
	Dereate above $25^\circ\text{C}$	0.34	$\text{W}/^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

## Thermal Characteristics

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case	3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient TO-252, $1\text{in}^2$ copper pad area	40	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD4243	FDD4243_F085	TO252	13"	12mm	2500 units

**Note:**

1. A suffix as "...F085P" has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$	-40	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	-	-32	-	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -32\text{V}$ $T_J = 125^\circ\text{C}$	-	-	-1	$\mu\text{A}$
			-	-	-100	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\mu\text{A}$	-1.4	-1.6	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$	-	4.7	-	$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = -6.7\text{A}$ , $V_{GS} = -10\text{V}$	-	36	44	m $\Omega$
		$I_D = -5.5\text{A}$ , $V_{GS} = -4.5\text{V}$	-	48	64	
		$I_D = -6.7\text{A}$ , $V_{GS} = -10\text{V}$ , $T_J = 150^\circ\text{C}$	-	57	70	
$g_{FS}$	Forward Transconductance	$I_D = -6.7\text{A}$ , $V_{DS} = -5\text{V}$ ,	-	23	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -20\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	1165	1550	pF
$C_{oss}$	Output Capacitance		-	165	220	pF
$C_{rss}$	Reverse Transfer Capacitance		-	90	135	pF
$R_G$	Gate Resistance	$f = 1\text{MHz}$	-	4	-	$\Omega$
$Q_{g(TOT)}$	Total Gate Charge	$V_{DD} = -20\text{V}$ , $V_{GS} = -10\text{V}$ , $I_D = -6.7\text{A}$	-	21	29	nC
$Q_{gs}$	Gate to Source Gate Charge		-	3.4	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	4	-	nC

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{V}, I_D = -6.7\text{A}$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	-	6	12	ns
$t_r$	Rise Time		-	15	26	ns
$t_{d(off)}$	Turn-Off Delay Time		-	22	35	ns
$t_f$	Fall Time		-	7	14	ns

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = -6.7\text{A}, V_{GS} = 0\text{V}$	-	-0.86	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = -6.7\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	29	43	ns
$Q_{rr}$	Reverse Recovery Charge		-	30	44	nC

**Note:**

- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 7.5\text{A}$ ,  $V_{GS} = 10\text{V}$ ,  $V_{DD} = 40\text{V}$  during the inductor charging time and  $0\text{V}$  during the time in avalanche.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

### Typical Characteristics

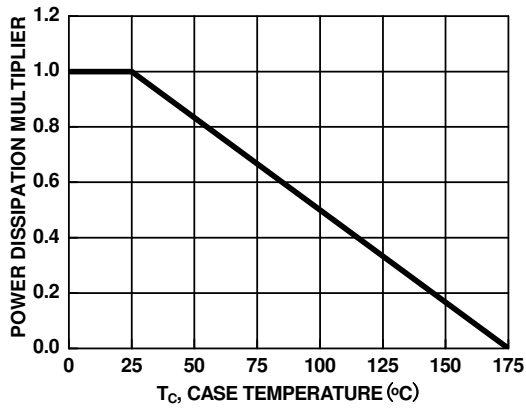


Figure 1. Normalized Power Dissipation vs Case Temperature

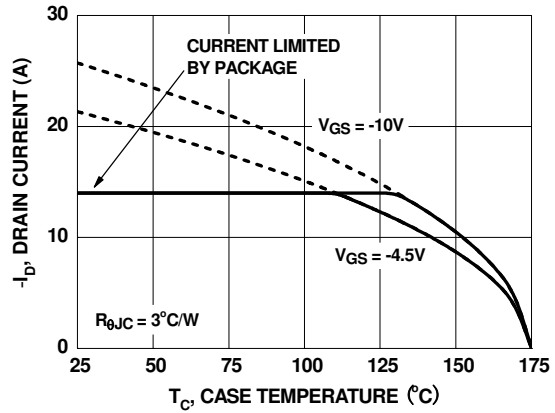


Figure 2. Maximum Continuous Drain Current vs Case Temperature

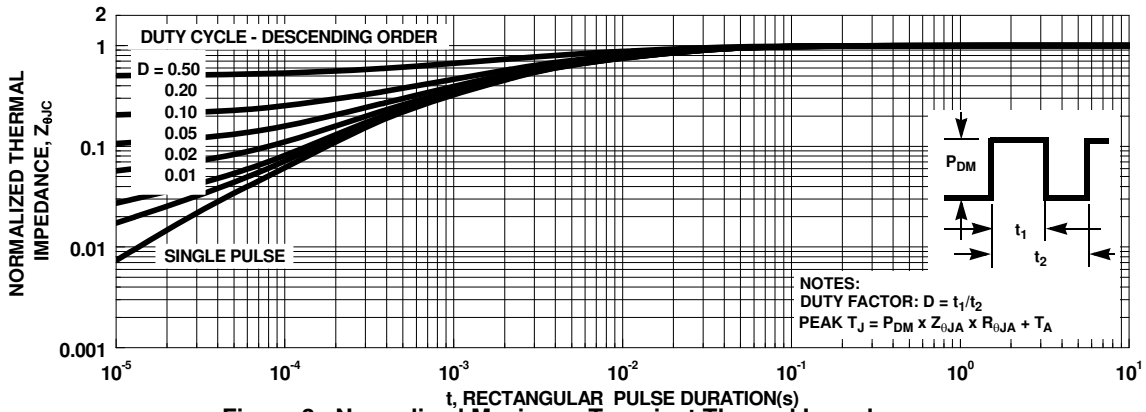


Figure 3. Normalized Maximum Transient Thermal Impedance

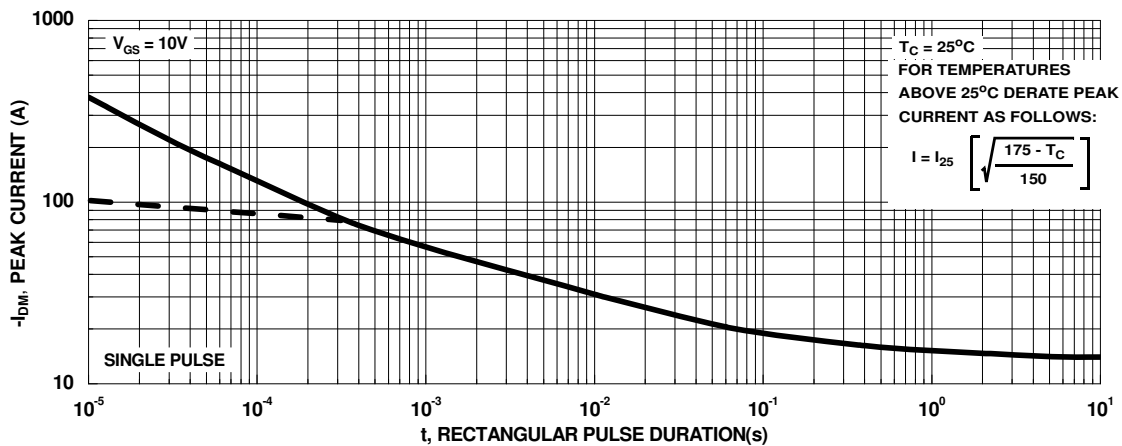


Figure 4. Peak Current Capability



## Typical Characteristics

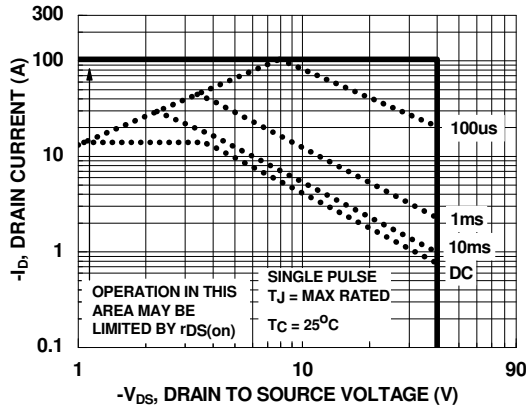
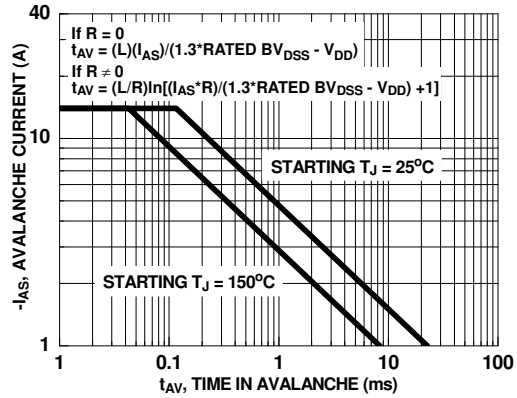


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

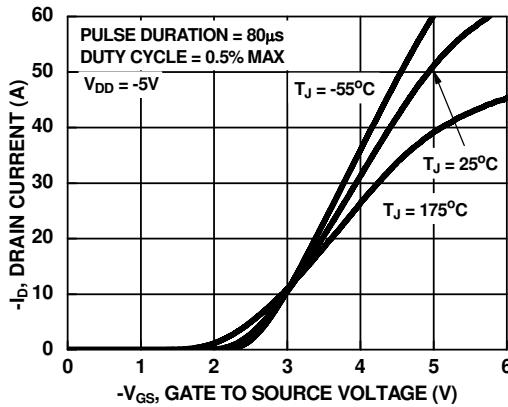


Figure 7. Transfer Characteristics

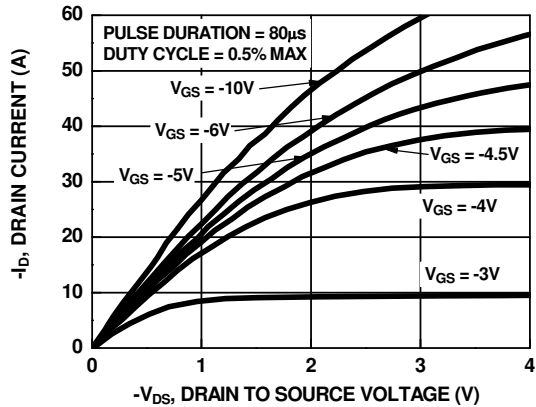


Figure 8. Saturation Characteristics

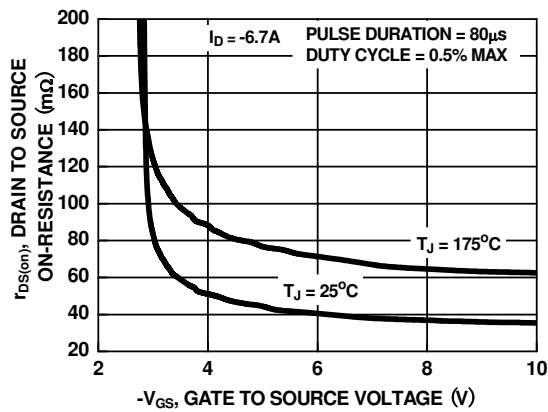


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

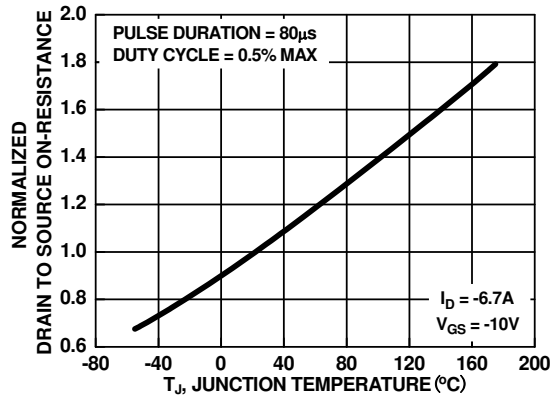


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

### Typical Characteristics

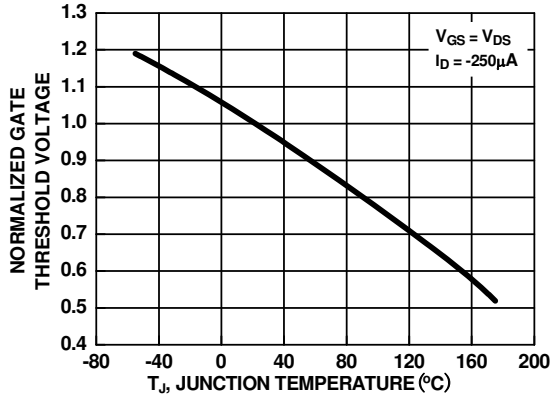


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

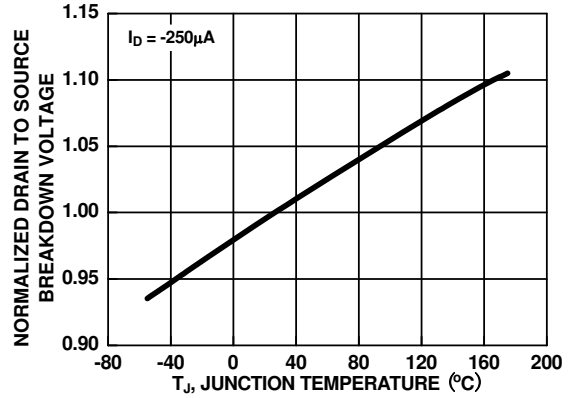


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

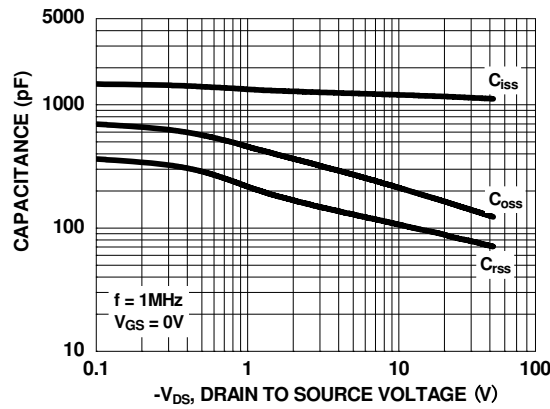


Figure 13. Capacitance vs Drain to Source Voltage

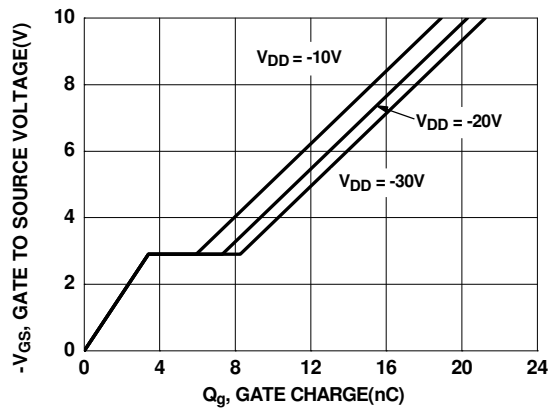
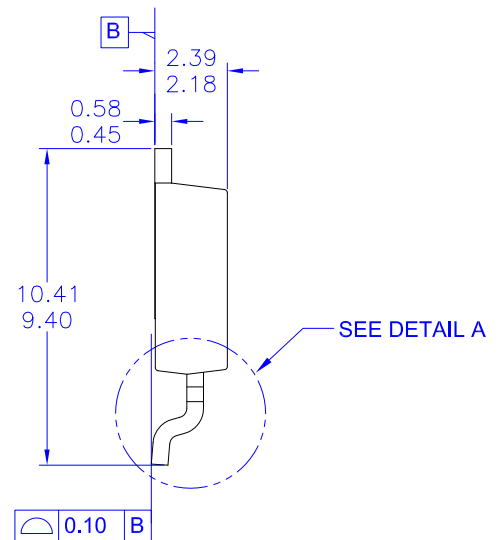
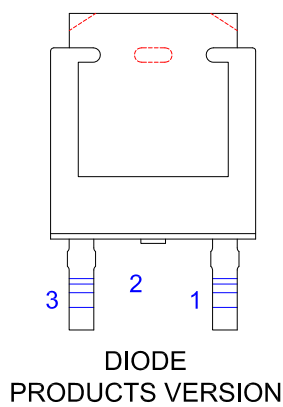
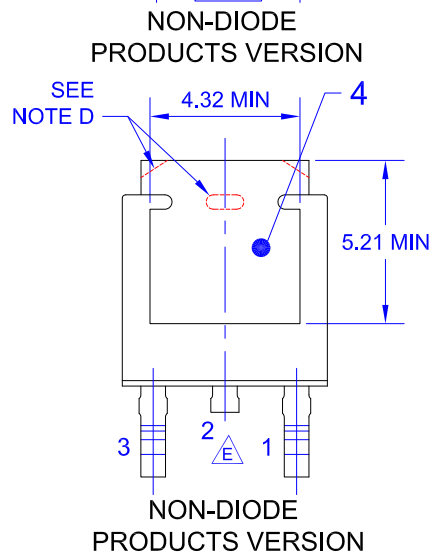
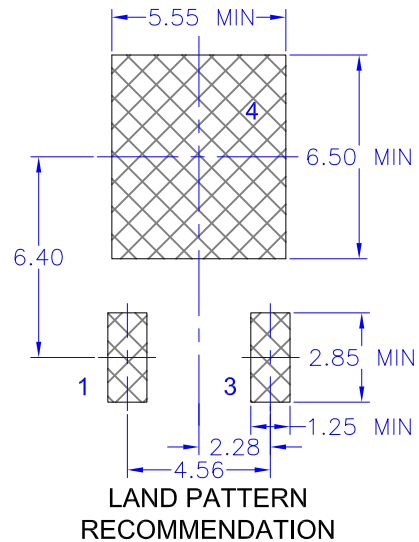
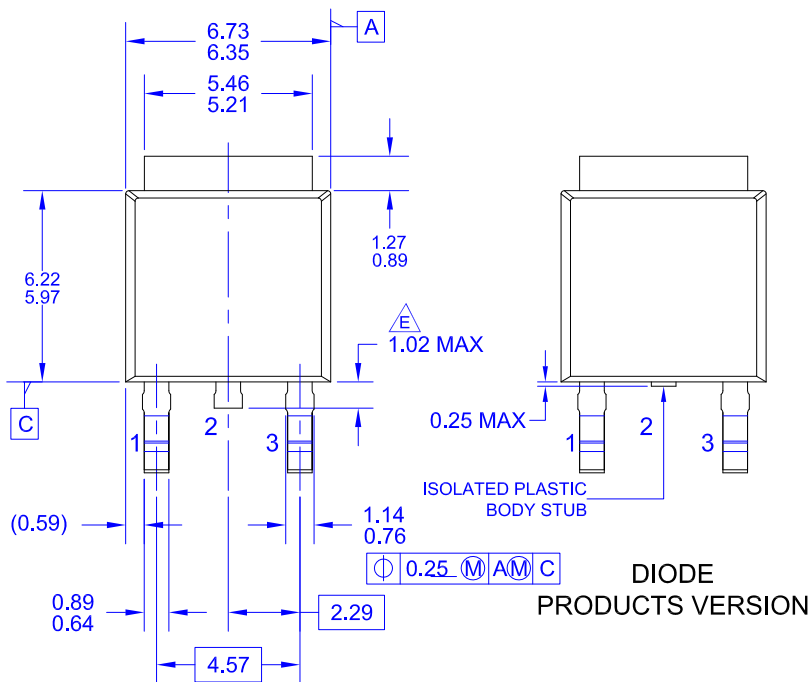


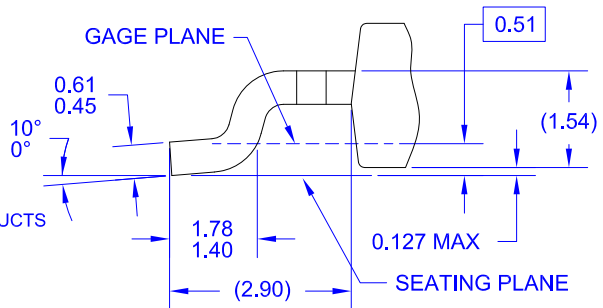
Figure 14. Gate Charge vs Gate to Source Voltage





NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A  
(ROTATED -90°)  
SCALE: 12X



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