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November 2013

## FDD5N50U

# N-Channel UniFET<sup>TM</sup> Ultra FRFET<sup>TM</sup> MOSFET 500 V, 3 A, 2.0 $\Omega$

#### **Features**

- $R_{DS(on)}$  = 1.65  $\Omega$  (Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 1.5 A
- Low Gate Charge (Typ. 11 nC)
- Low C<sub>rss</sub> (Typ. 5 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

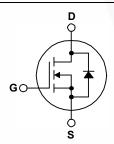
## **Applications**

- LCD/LED/PDP TV
- Lighting
- · Uninterruptible Power Supply

## Description

UniFET<sup>TM</sup> MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. UniFET Ultra FRFET<sup>TM</sup> MOSFET has much superior body diode reverse recovery performance. Its t<sub>rr</sub> is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





#### **MOSFET Maximum Ratings** T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FDD5N50UTM_WS	Unit
$V_{DSS}$	Drain to Source Voltage			500	V
$V_{GSS}$	Gate to Source Voltage			±30	V
	Drain Current	- Continuous (T <sub>C</sub> = 25°C)		3	А
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 100°C)		1.8	_ A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	12	Α
E <sub>AS</sub>	Single Pulsed Avalanche	Energy	(Note 2)	275	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)		(Note 1)	3	Α
E <sub>AR</sub>	Repetitive Avalanche Ene	Repetitive Avalanche Energy (Note 1)		4	mJ
dv/dt	Peak Diode Recovery dv/	dt	(Note 3)	4.5	V/ns
D	$(T_C = 25^{\circ}C)$			40	W
$P_D$	Power Dissipation	- Derate Above 25°C		0.3	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +150	οС
$T_L$	Maximum Lead Temperat	ture for Soldering, 1/8" from Case for 5 S	econds	300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FDD5N50UTM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta,JA}$	Thermal Resistance, Junction to Ambient, Max.	110	*C/VV

## **Package Marking and Ordering Information**

Pa	art Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD	5N50UTM_WS	FDD5N50U	DPAK	Tape and Reel	330 mm	16 mm	2500 units

## **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV <sub>DSS</sub> / ΔΤ <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C	-	0.6	-	V/°C
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	25	^
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 400 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	250	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

#### **On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3	-	5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A	-	1.65	2.0	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 1.5 \text{ A}$	ı	4	-	S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05.V.V 0.V		-	485	650	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	65	90	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 WH12		-\	5	8	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 5 A,		-	11	15	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V		-	3	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	5	-	nC

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	14	38	ns
t <sub>r</sub>		$V_{DD} = 250 \text{ V}, I_D = 5 \text{ A},$	-	21	52	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_G$ = 25 $\Omega$	-	27	64	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	20	50	ns

#### **Drain-Source Diode Characteristics**

				ı	1	т —
IS	Maximum Continuous Drain to Source Dio	Maximum Continuous Drain to Source Diode Forward Current		-	3	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode F	Maximum Pulsed Drain to Source Diode Forward Current		-	12	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 3 A	-	-	1.6	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 5 A,	-	36	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	33	_	nC

#### Notes:

- 1: Repetitive rating: pulse width limited by maximum junction temperature.
- 2: L = 61 mH, I<sub>AS</sub> = 3 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25°C.
- 3:  $I_{SD} \leq 3$  A, di/dt  $\leq 200$  A/ $\mu$ s,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J$  = 25°C.
- 4: Essentially independent of operating temperature typical characteristics.

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

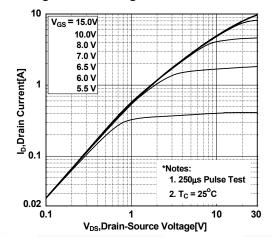


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

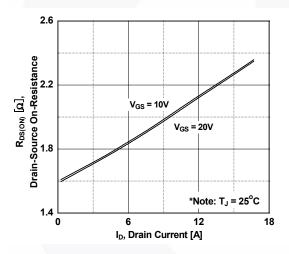
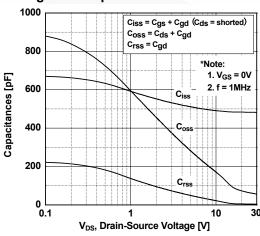


Figure 5. Capacitance Characteristics



**Figure 2. Transfer Characteristics** 

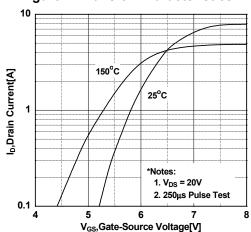


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

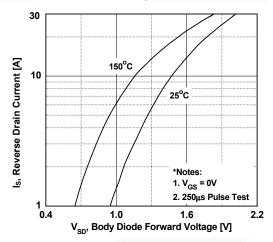
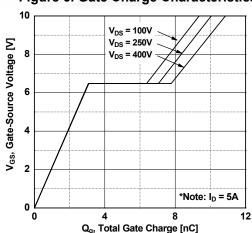


Figure 6. Gate Charge Characteristics



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

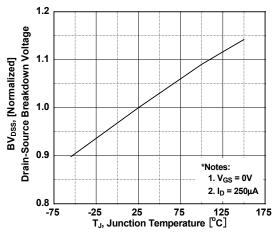


Figure 8. Maximum Safe Operating Area

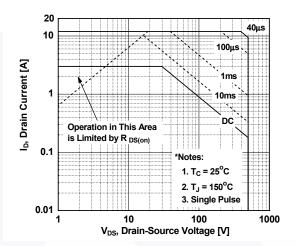


Figure 9. Maximum Drain Current vs. Case Temperature

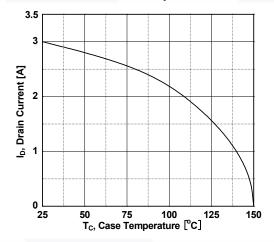
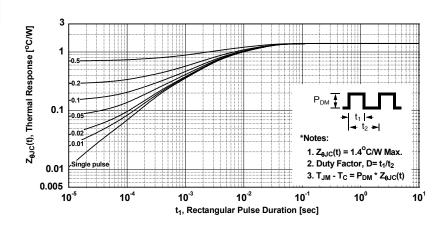


Figure 10. Transient Thermal Response Curve



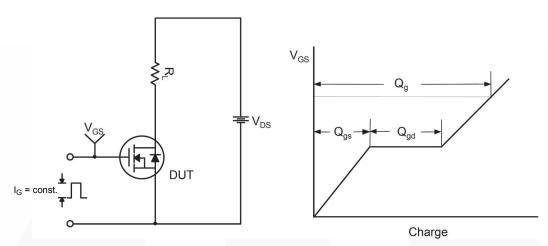


Figure 11. Gate Charge Test Circuit & Waveform

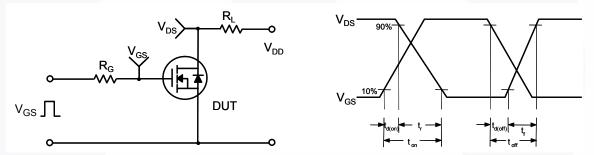


Figure 12. Resistive Switching Test Circuit & Waveforms

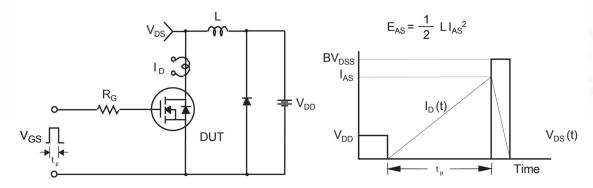


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

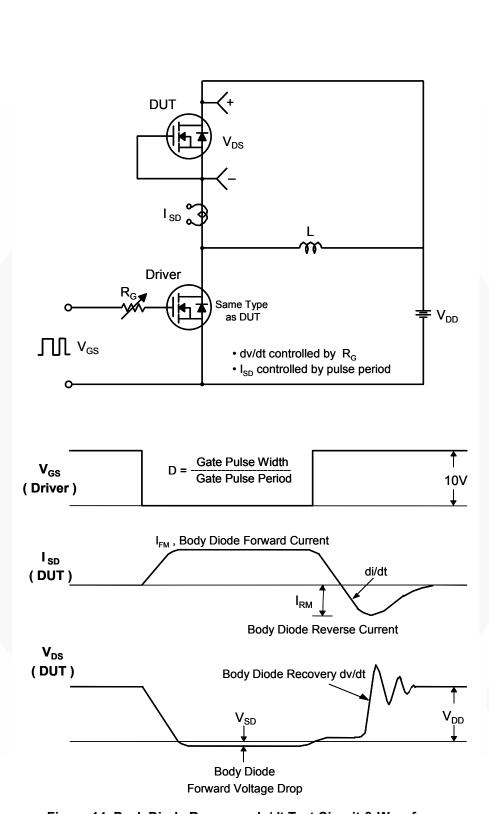


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

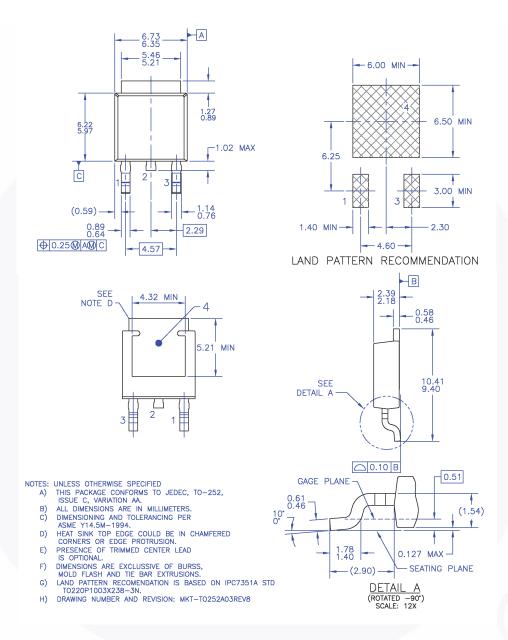


Figure 15. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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