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February 2007

# UniFET™

## **FDD6N25 / FDU6N25**

#### 250V N-Channel MOSFET

#### **Features**

- 4.4A, 250V,  $R_{DS(on)} = 1.1\Omega @V_{GS} = 10 \text{ V}$
- Low gate charge (typical 4.5 nC)
- Low  $C_{rss}$  (typical 5 pF)
- Fast switching
- 100% avalanche tested
- · Improved dv/dt capability

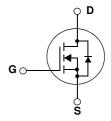
## **Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.







### **Absolute Maximum Ratings**

Symbol	Parameter		FDD6N25 / FDU6N25	Unit
V <sub>DSS</sub>	Drain-Source Voltage		250	V
I <sub>D</sub>	$ \begin{array}{ccc} \text{Drain Current} & & -\text{Continuous } (T_C = 25^{\circ}\text{C}) \\ & -\text{Continuous } (T_C = 100^{\circ}\text{C}) \end{array} $		4.4 2.6	A A
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	18	Α
V <sub>GSS</sub>	Gate-Source voltage		±30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	45	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	4.4	Α
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C		50 0.4	W W/°C
$T_{J,}T_{STG}$	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

#### **Thermal Characteristics**

Symbol	Parameter	Тур	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		110	°C/W

# **Package Marking and Ordering Information**

<b>Device Marking</b>	Device	Package	Reel Size	Tape Width	Quantity
FDD6N25	FDD6N25TM	D-PAK	380mm	16mm	2500
FDD6N25	FDD6N25TF	D-PAK	380mm	16mm	2000
FDU6N25	FDU6N25TU	I-PAK	-	-	70

## $\textbf{Electrical Characteristics} \quad \textbf{T}_{C} = 25^{\circ}\text{C unless otherwise noted}$

Symbol	Parameter	Conditions	Min.	Тур.	Max	Units
Off Charac	Off Characteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	250			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C		0.25		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 250V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 200V, T <sub>C</sub> = 125°C			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	$V_{GS} = 30V$ , $V_{DS} = 0V$			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -30V$ , $V_{DS} = 0V$			-100	nA
On Charac	teristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu A$	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.2A		0.9	1.1	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40V, I_D = 2.2A$ (Note 4)		5.5		S
Dynamic C	haracteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$		194	250	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0MHz		38	50	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			5	8	pF
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 125V, I_D = 6A$		10	30	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25\Omega$		25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			7	24	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4, 5)		12	34	ns
$Q_g$	Total Gate Charge	$V_{DS} = 200V, I_{D} = 6A$		4.5	6	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{GS} = 10V$		1.5		nC
$Q_{gd}$	Gate-Drain Charge	(Note 4, 5)		1.8		nC
Drain-Sour	ce Diode Characteristics and Maximun	n Ratings		·		
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				4.4	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				18	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 4.4A			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0V$ , $I_S = 6A$		145		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s $ (Note 4)		0.55		μС
	•	•		•		

#### NOTES

<sup>1.</sup> Repetitive Rating: Pulse width limited by maximum junction temperature

<sup>2.</sup> L = 3.7mH, I  $_{AS}$  = 4.4A, V  $_{DD}$  = 50V, R  $_{G}$  = 25 $\!\Omega$ , Starting T  $_{J}$  = 25°C

<sup>3.</sup>  $I_{SD} \le 4.4 A, \, di/dt \le 200 A/\mu s, \, V_{DD} \le BV_{DSS}, \, Starting \, T_J = 25^{\circ}C$ 

<sup>4.</sup> Pulse Test: Pulse width  $\leq 300 \mu s, \ \text{Duty Cycle} \leq 2\%$ 

<sup>5.</sup> Essentially Independent of Operating Temperature Typical Characteristics

## **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

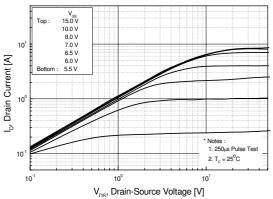


Figure 3. On-Resistance Variation vs. **Drain Current and Gate Voltage** 

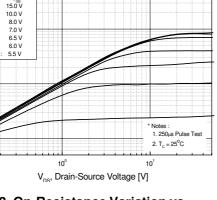


Figure 4. Body Diode Forward Voltage Variation vs. Source Current

10<sup>0</sup> – 0.2

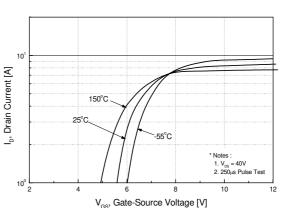
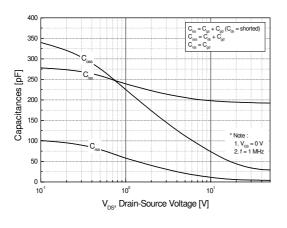


Figure 2. Transfer Characteristics

Drain-Source On-Resistance  $V_{GS} = 10V$  $R_{DS(ON)}[\Omega],$ \* Note :  $T_J = 25^{\circ}C$ I<sub>D</sub>, Drain Current [A]

Figure 5. Capacitance Characteristics



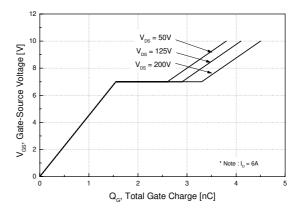
Reverse Drain Current [A] Notes :

and Temperatue

Figure 6. Gate Charge Characteristics

 $V_{\rm SD}$ , Source-Drain voltage [V]

1. V<sub>GS</sub> = 0V 2. 250μs Pulse Test



## **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

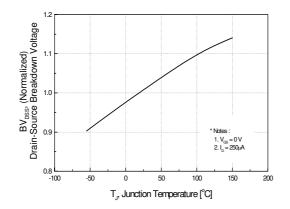


Figure 8. On-Resistance Variation vs. Temperature

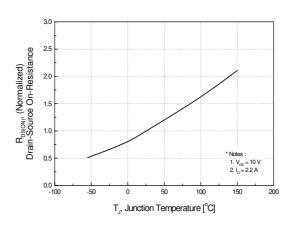
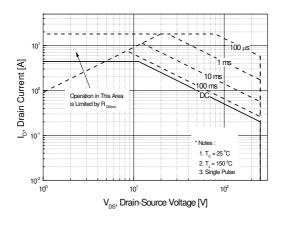


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature



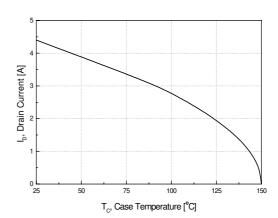
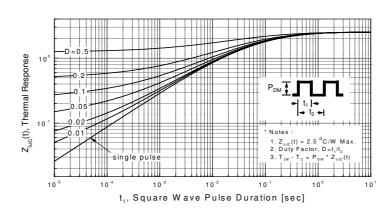
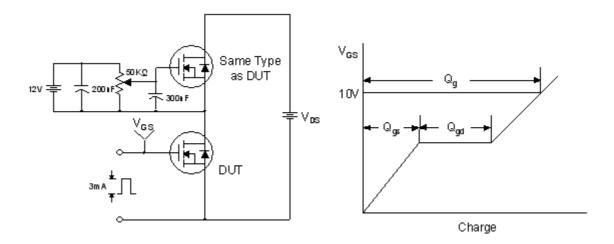


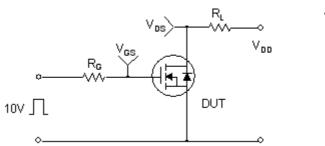
Figure 11. Transient Thermal Response Curve

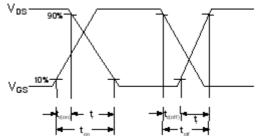


### **Gate Charge Test Circuit & Waveform**

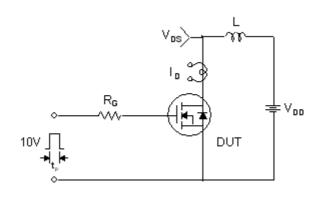


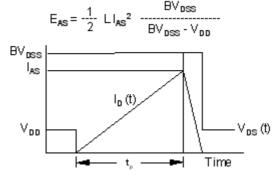
#### **Resistive Switching Test Circuit & Waveforms**



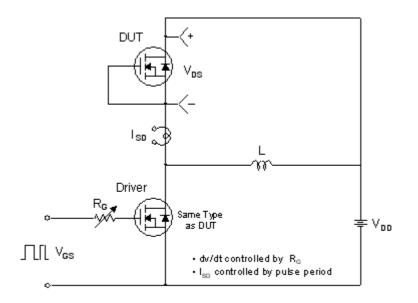


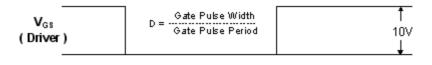
#### **Unclamped Inductive Switching Test Circuit & Waveforms**

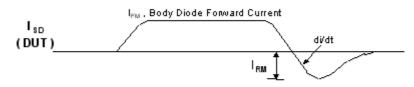


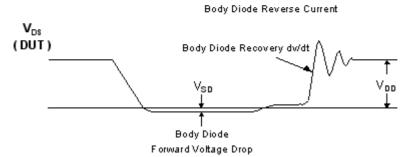


### Peak Diode Recovery dv/dt Test Circuit & Waveforms



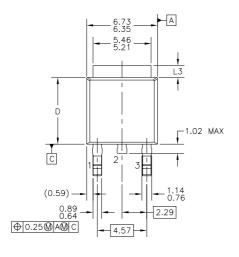


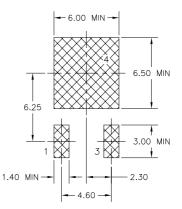




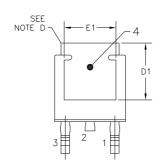
### **Mechanical Dimensions**

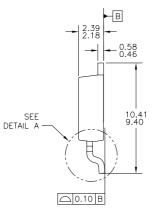
# **D-PAK**

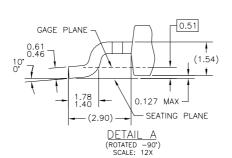




LAND PATTERN RECOMMENDATION







- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  E) DIMENSIONS L3,D,E1&D1 TABLE:

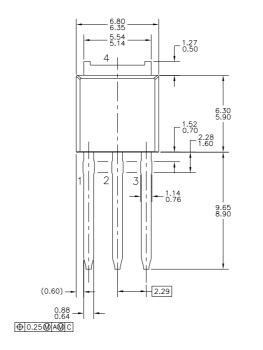
  | DIMENSIONS L3,D,E1&D1 TABLE:
  | DIMENSIONS L3,D,E1&D2 TABLE:
  | DIMENSIONS L3,D,E1&

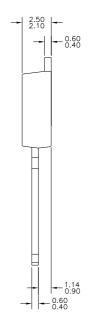
	L3	0.89-1.27	1.52-2.03	
	D	5.97-6.22	5.33-5.59	
	E1	4.32 MIN	3.81 MIN	
	D1	5.21 MIN	4.57 MIN	
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## **Mechanical Dimensions**

# I-PAK











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