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March 2015

# FDD8796/FDU8796
# N-Channel PowerTrench® MOSFET
## 25V, 35A, 5.7mΩ

## General Description

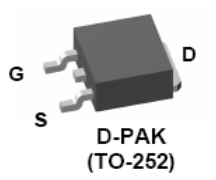
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.

## Application

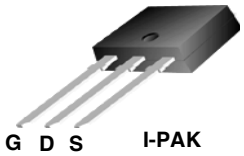
- Vcore DC-DC for Desktop Computers and Servers
- VRM for Intermediate Bus Architecture

## Features

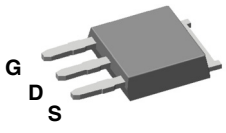
- Max $r_{DS(on)}$ = 5.7mΩ at $V_{GS}$ = 10V, $I_D$ = 35A
- Max $r_{DS(on)}$ = 8.0mΩ at $V_{GS}$ = 4.5V, $I_D$ = 35A
- Low gate charge: $Q_{g(10)}$ = 37nC(Typ), $V_{GS}$ = 10V
- Low gate resistance
- Avalanche rated and 100% tested
- RoHS Compliant



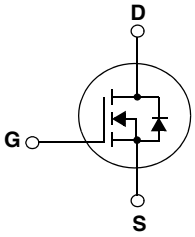
D-PAK
(TO-252)



I-PAK
(TO-251AA)



Short Lead I-PAK




## MOSFET Maximum Ratings $T_C$= 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 25 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current -Continuous (Package Limited) | | 35 | A |
| | -Continuous (Die Limited) | | 98 | |
| | -Pulsed | (Note 1) | 305 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | (Note 2) | 91 | mJ |
| $P_D$ | Power Dissipation | | 88 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | | -55 to 175 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case TO_252, TO_251 | 1.7 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient TO_252, TO_251 | 100 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient TO-252,1in$^2$ copper pad area | 52 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDD8796 | FDD8796 | TO-252AA | 13” | 16mm | 2500 units |
| FDU8796 | FDU8796 | TO-251AA | N/A (Tube) | N/A | 75 units |
| FDU8796 | FDU8796_F071 | TO-251AA | N/A (Tube) | N/A | 75 units |

## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250μA, $V_{GS}$ = 0V | 25 | | | V |
| $\frac{\Delta B_{VDSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | 7 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 20V, $V_{GS}$ = 0V | | | 1 | μA |
| | | $V_{DS}$ = 20V, $V_{GS}$ = 0V, $T_J$ = 150°C | | | 250 | |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1.2 | 1.8 | 2.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250μA, referenced to 25°C | | -6.7 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 10V, $I_D$ = 35A | | 4.5 | 5.7 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 35A | | 6.0 | 8.0 | |
| | | $V_{DS}$ = 10V, $I_D$ = 35A, $T_J$ = 175°C | | 6.9 | 9.5 | |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 13V, $V_{GS}$ = 0V, f = 1MHz | | 1960 | 2610 | pF |
| $C_{oss}$ | Output Capacitance | | | 455 | 605 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 315 | 475 | pF |
| $R_G$ | Gate Resistance | f = 1MHz | | 1.1 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ =13V, $I_D$ = 35A, $V_{GS}$ = 10V, $R_{GS}$ = 20Ω | | 10 | 20 | ns |
| $t_r$ | Rise Time | | | 24 | 39 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 99 | 158 | ns |
| $t_f$ | Fall Time | | | 57 | 91 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 to10V, $V_{DD}$ =13V, $I_D$ = 35A, $I_g$ = 1.0mA | | 37 | 52 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 to 5V | | 19 | 27 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | 6 | | nC |
| $Q_{gd}$ | Gate to Drain Charge | | | 6 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Voltage | $V_{GS}$ = 0V, $I_S$ = 35A | | 0.9 | 1.25 | V |
| | | $V_{GS}$ = 0V, $I_S$ = 15A | | 0.8 | 1.0 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 35A, di/dt = 100A/μs | | 30 | 45 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | $I_F$ = 35A, di/dt = 100A/μs | | 23 | 35 | nC |

**Notes:**
**1:** Pulse time < 300μs, Duty cycle = 2%.
**2:** Starting $T_J$ = 25°C, L = 0.3mH, $I_{AS}$ = 24.7A, $V_{DD}$ = 23V, $V_{GS}$ = 10V.

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

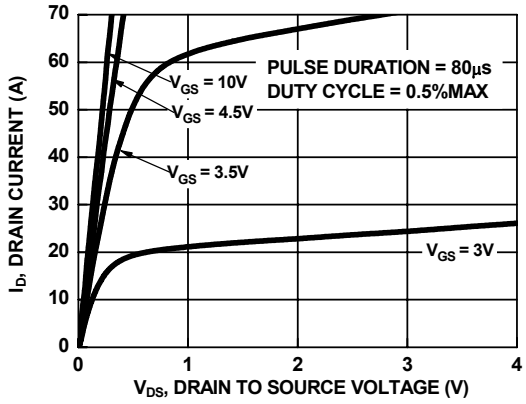



**Figure 1. On Region Characteristics**

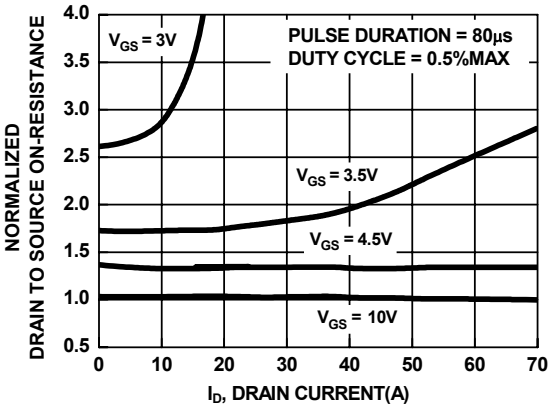



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

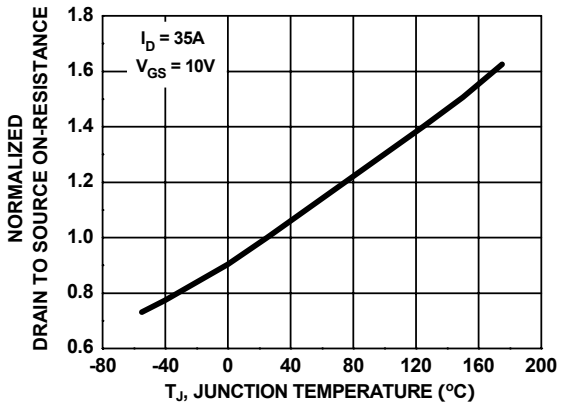



**Figure 3. Normalized On Resistance vs Junction Temperature**

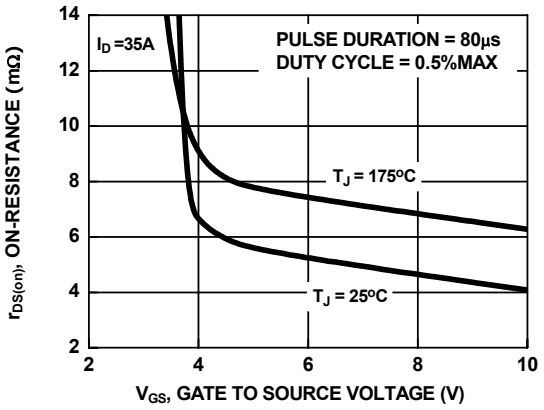



**Figure 4. On-Resistance vs Gate to Source Voltage**

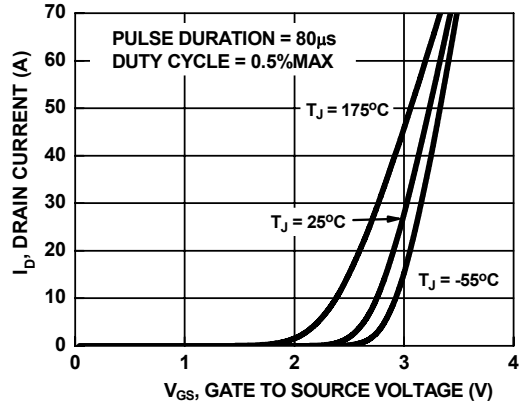



**Figure 5. Transfer Characteristics**

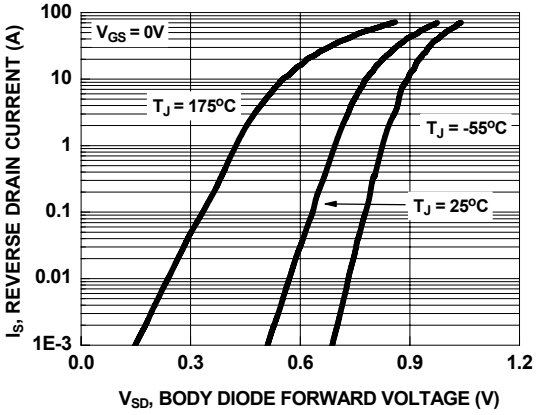



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

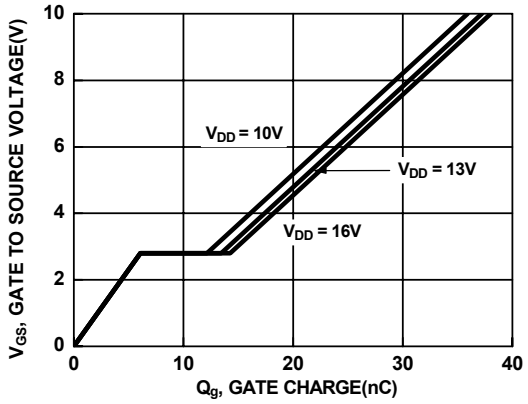



Figure 7. Gate Charge Characteristics

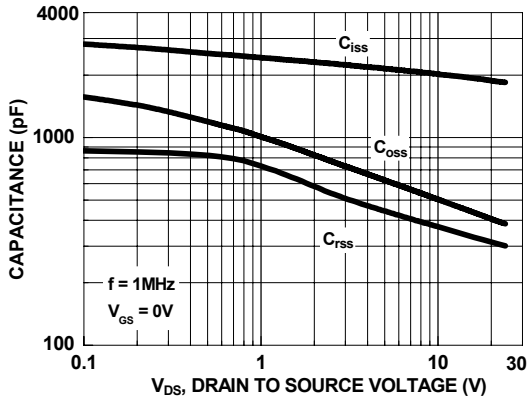



Figure 8. Capacitance vs Drain to Source Voltage

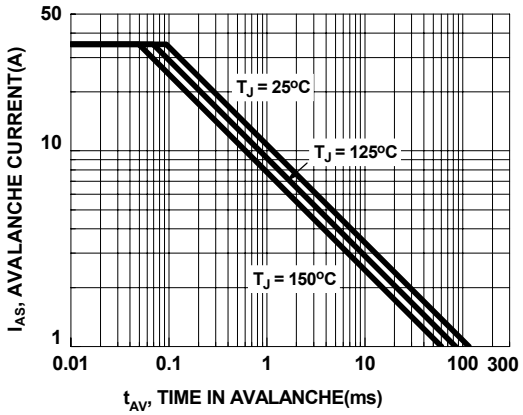



Figure 9. Unclamped Inductive Switching Capability

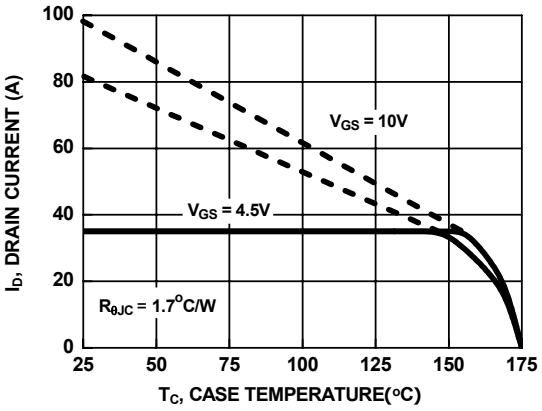



Figure 10. Maximum Continuous Drain Current vs Case Temperature

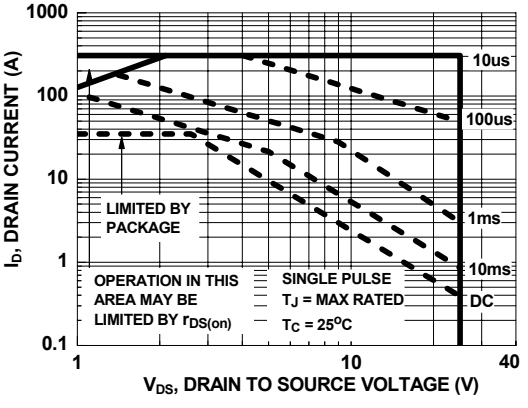



Figure 11. Forward Bias Safe Operating Area

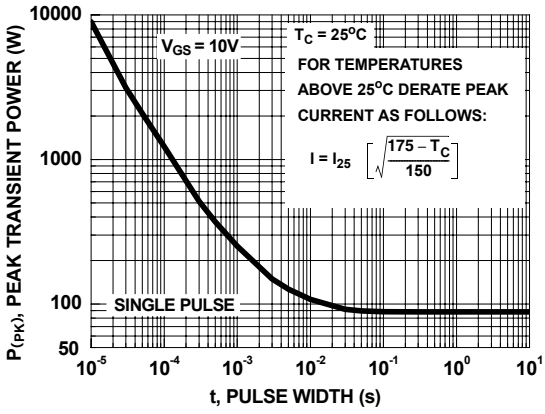



Figure 12. Single Pulse Maximum Power Dissipation

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

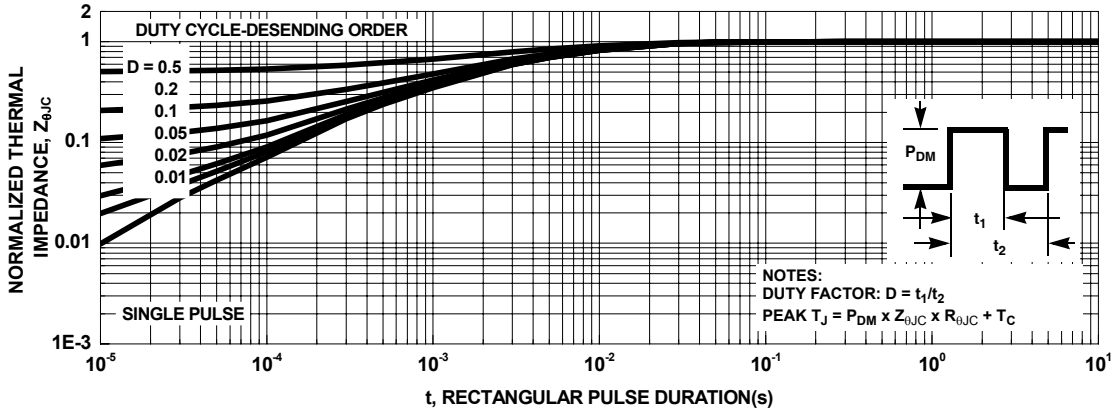
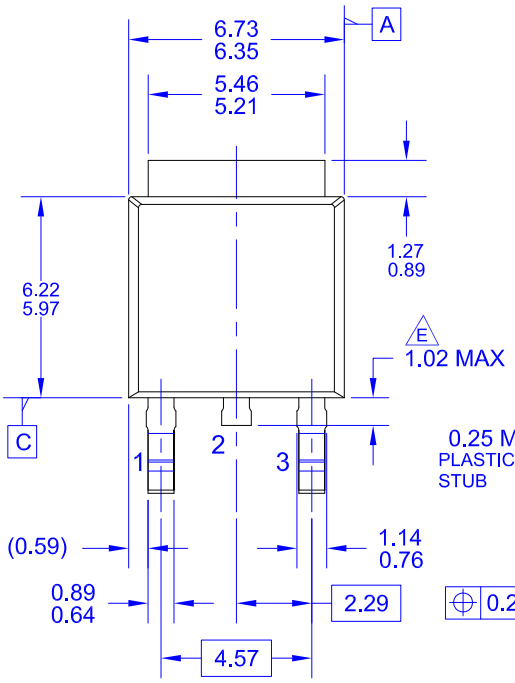
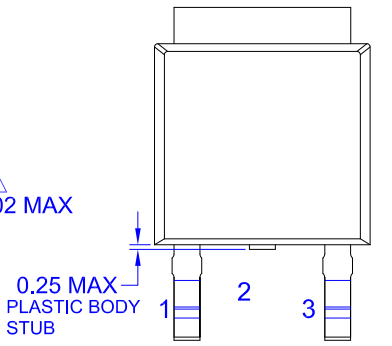


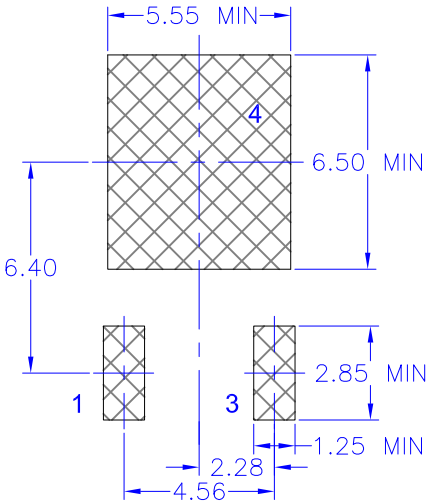

**Figure 13. Transient Thermal Response Curve**



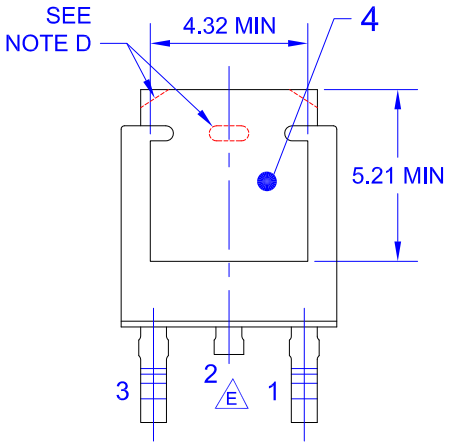

NON-DIODE PRODUCTS VERSION




DIODE PRODUCTS VERSION




LAND PATTERN RECOMMENDATION

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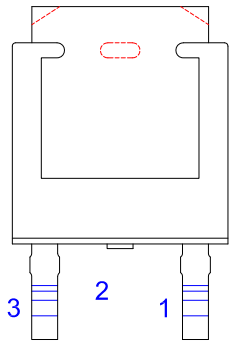


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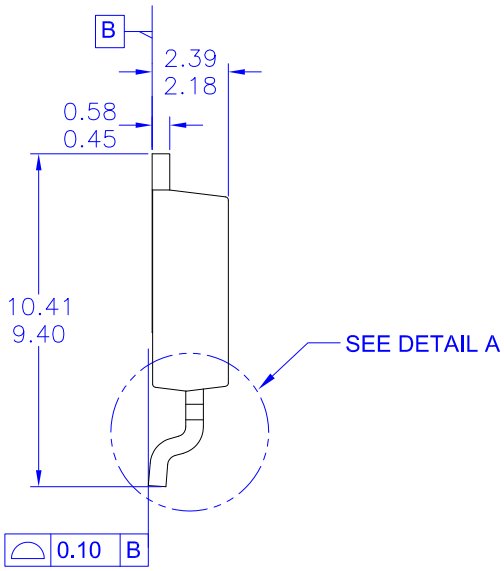
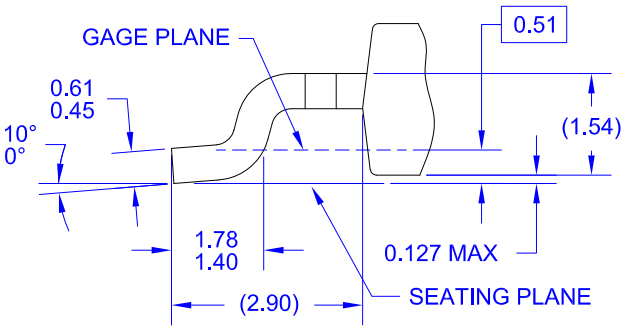



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10

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### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

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