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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



March 2015

FDD8876 / FDU8876

FDD8876 / FDU8876

N-Channel PowerTrench® MOSFET 30V, 73A, 8.2mΩ

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

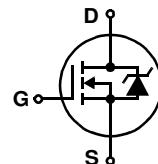
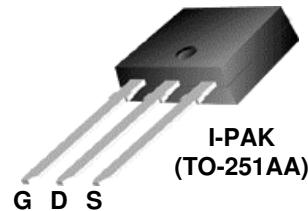
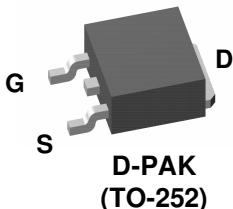
Applications

- DC/DC converters



Features

- $r_{DS(ON)} = 8.2\text{m}\Omega$, $V_{GS} = 10\text{V}$, $I_D = 35\text{A}$
- $r_{DS(ON)} = 10\text{m}\Omega$, $V_{GS} = 4.5\text{V}$, $I_D = 35\text{A}$
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$) (Note 1)	73	A
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5\text{V}$) (Note 1)	66	A
	Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$, with $R_{\theta JA} = 52^\circ\text{C/W}$)	15	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	95	mJ
P_D	Power dissipation	70	W
	Derate above 25°C	0.47	W/ $^\circ\text{C}$
T_J , T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252, TO-251	2.14	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, TO-251	100	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8876	FDD8876	TO-252AA	13"	16mm	2500 units
FDU8876	FDU8876	TO-251AA	Tube	N/A	75 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 35\text{A}, V_{GS} = 10\text{V}$	-	0.0066	0.0082	Ω
		$I_D = 35\text{A}, V_{GS} = 4.5\text{V}$	-	0.008	0.010	
		$I_D = 35\text{A}, V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$	-	0.011	0.013	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	1700	-	pF
C_{OSS}	Output Capacitance		-	330	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	200	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}, f = 1\text{MHz}$	-	2.2	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	-	34	47	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V to } 5\text{V}$	-	18	26	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 1\text{V}$	$V_{DD} = 15\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$	1.4	1.9	nC
Q_{gs}	Gate to Source Gate Charge	4.2		-	nC	
Q_{gs2}	Gate Charge Threshold to Plateau	2.8		-	nC	
Q_{gd}	Gate to Drain "Miller" Charge	8.0		-	nC	

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 35\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 10\Omega$	-	-	149	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	91	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	44	-	ns
t_f	Fall Time		-	37	-	ns
t_{OFF}	Turn-Off Time		-	-	122	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 35\text{A}$	-	-	1.25	V
		$I_{SD} = 15\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	26	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	12	nC

Notes:

1: Package current limitation is 35A.

2: Starting $T_J = 25^\circ\text{C}$, $L = 0.24\text{mH}$, $I_{AS} = 28\text{A}$, $V_{DD} = 27\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

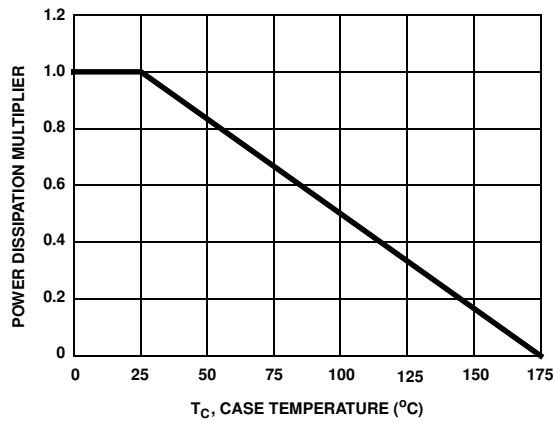


Figure 1. Normalized Power Dissipation vs Case Temperature

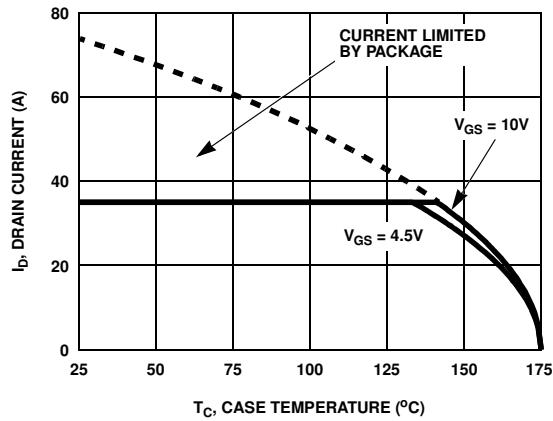


Figure 2. Maximum Continuous Drain Current vs Case Temperature

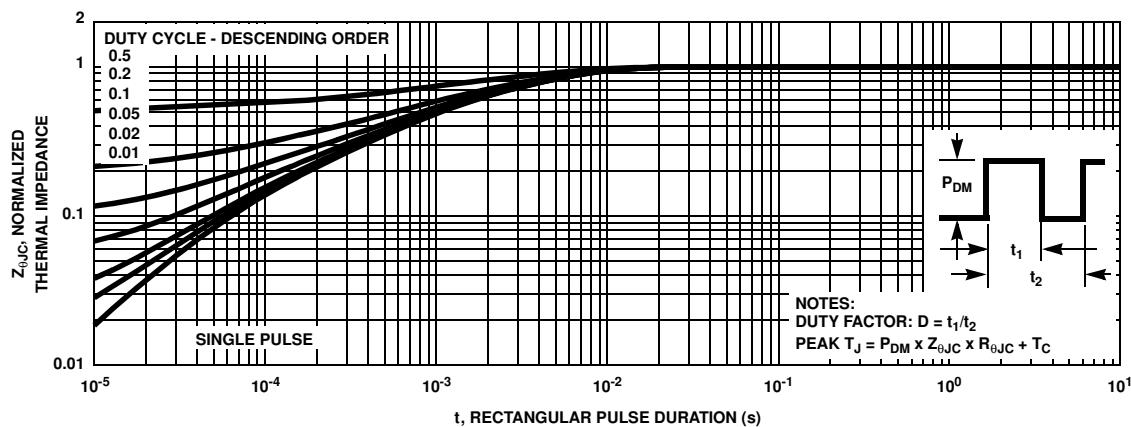


Figure 3. Normalized Maximum Transient Thermal Impedance

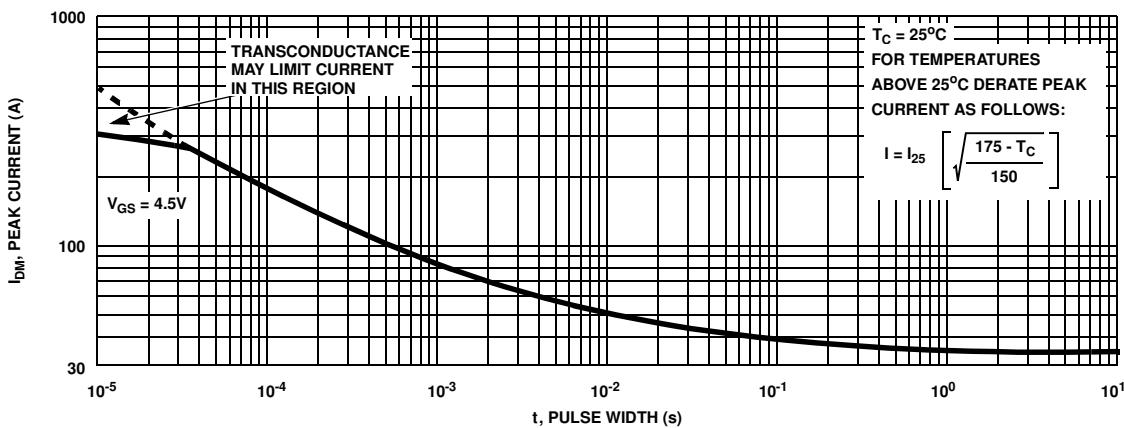


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

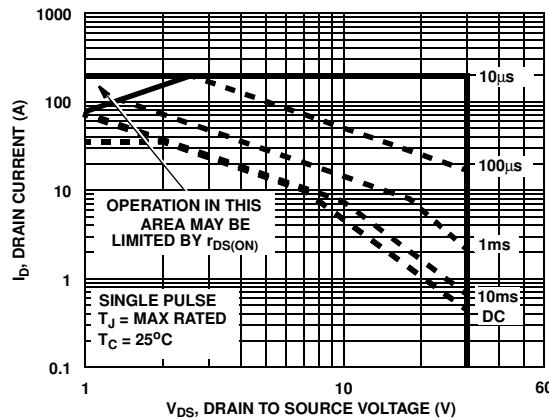
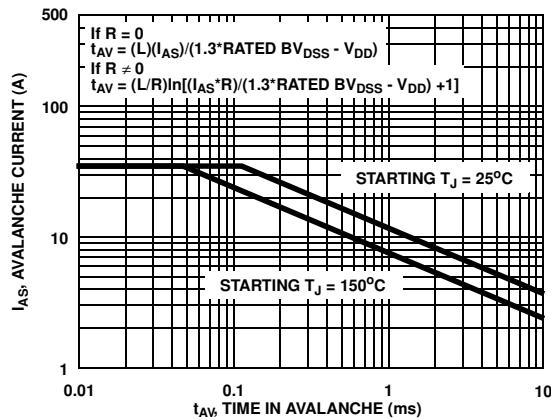


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

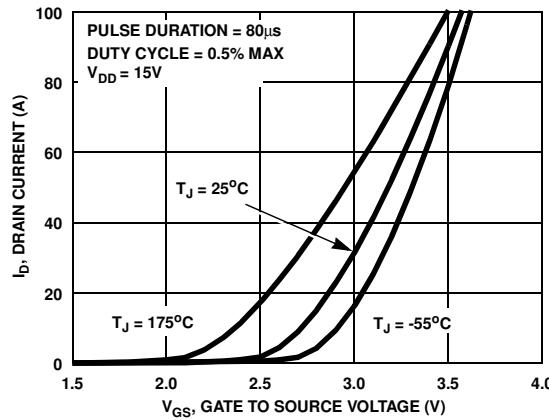


Figure 7. Transfer Characteristics

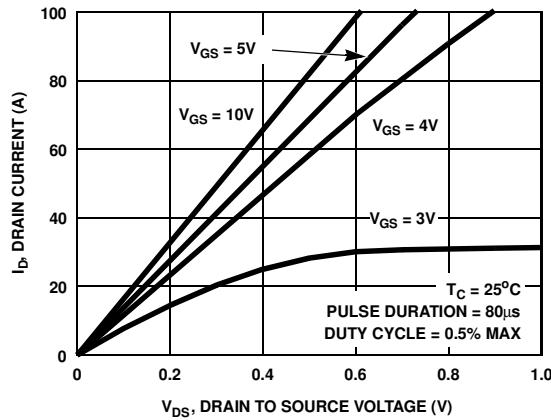


Figure 8. Saturation Characteristics

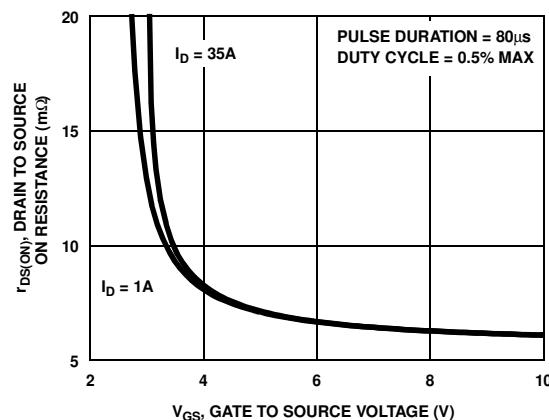


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

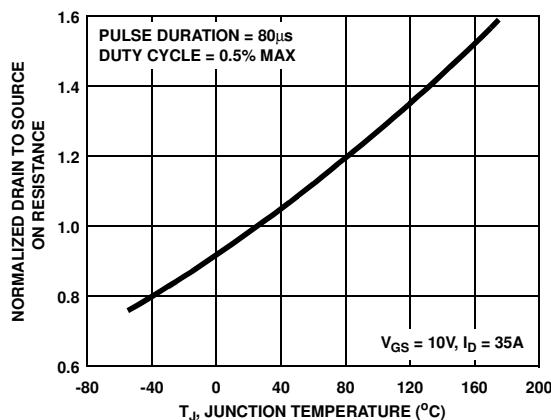


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

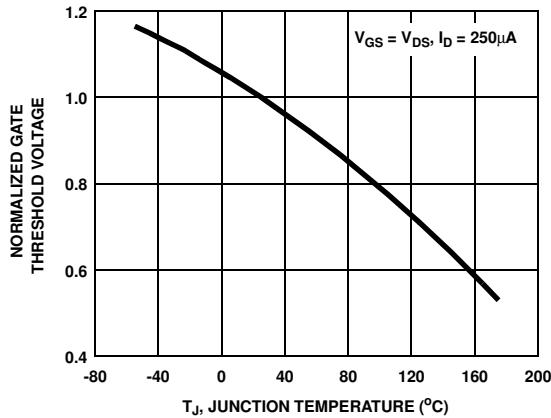


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

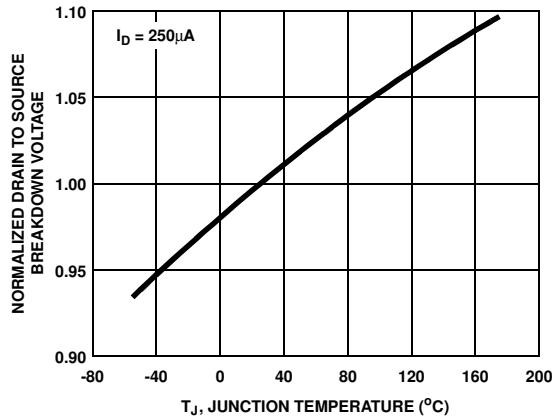


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

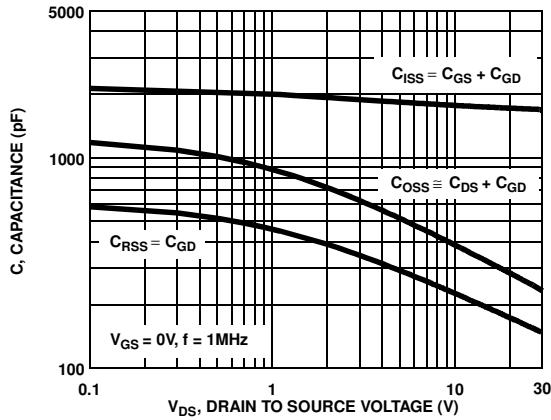


Figure 13. Capacitance vs Drain to Source Voltage

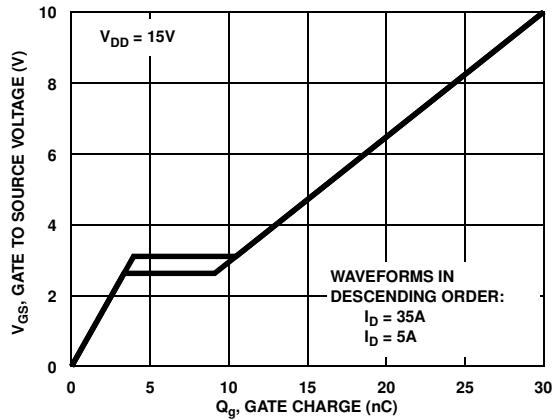


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

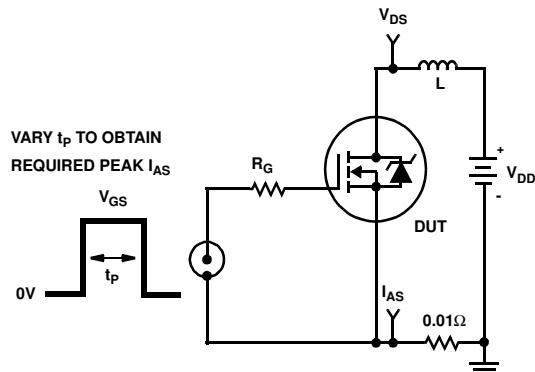


Figure 15. Unclamped Energy Test Circuit

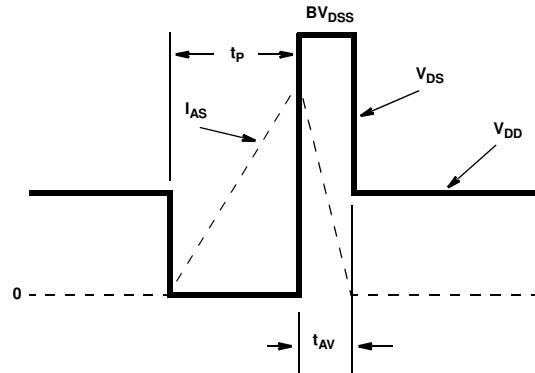


Figure 16. Unclamped Energy Waveforms

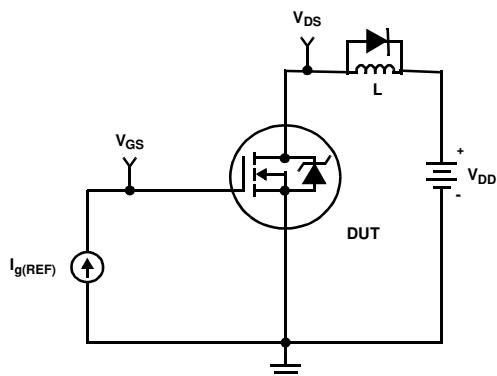


Figure 17. Gate Charge Test Circuit

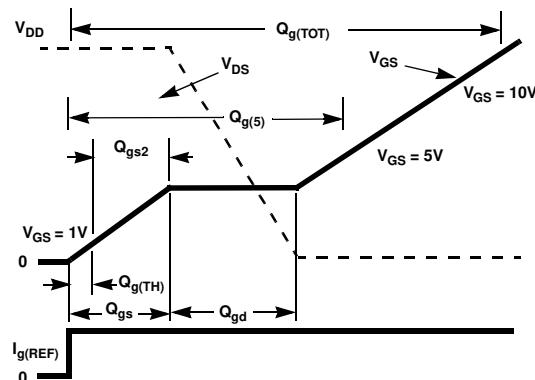


Figure 18. Gate Charge Waveforms

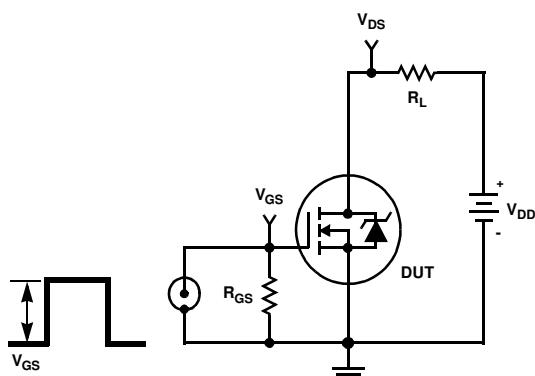


Figure 19. Switching Time Test Circuit

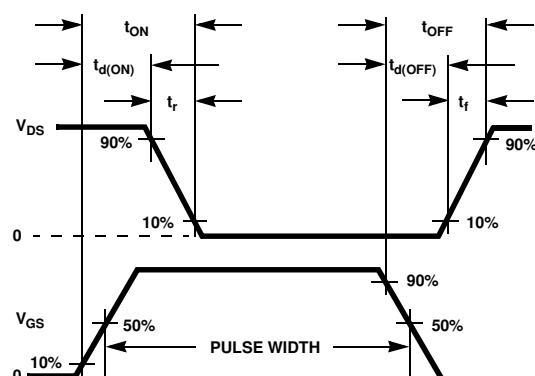


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}$ C), and thermal resistance $R_{\theta JA}$ ($^{\circ}$ C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + \text{Area})} \quad (\text{EQ. 2})$$

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + \text{Area})} \quad (\text{EQ. 3})$$

Area in Centimeters Squared

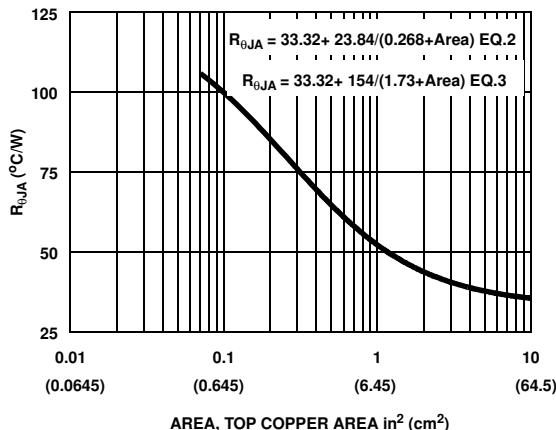


Figure 21. Thermal Resistance vs Mounting Pad Area

SABER Electrical Model

```

rev January 2004
template FDD8876 n2,n1,n3 =m_temp
electrical n2,n1,n3
number m_temp=25
{
var i iscl
dp..model dbodymod = (isl=3e-12,ikf=10,nl=1.01,rs=3.4e-3,trs1=8e-4,trs2=2e-7,cjo=6.3e-10,m=0.57,tt=1e-17,xti=2)
dp..model dbreakmod = (rs=1,trs1=1e-3,trs2=-8.9e-6)
dp..model dplcapmod = (cjo=6.1e-10,isl=10e-30,nl=10,m=0.41)
m..model mmedmod = (type=_n,vto=1.95,kp=10,ls=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=2.45,kp=250,ls=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=1.65,kp=0.05,ls=1e-30,tox=1,rs=0.1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3.5,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2,voff=-1.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-2)
c.ca n12 n8 = 1.9e-9
c.cb n15 n14 = 1.6e-9
c.cin n6 n8 = 1.55e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 33.15
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1
I.igate n1 n9 = 4.7e-9
I.rdrain n2 n5 = 1.0e-9
I.lsourc n3 n7 = 1.7e-9

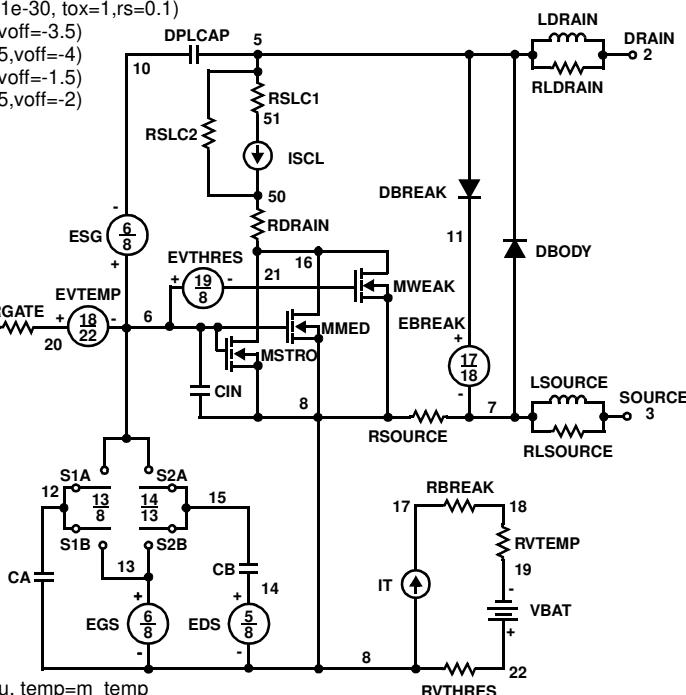
res.rigate n1 n9 = 47
res.rldrain n2 n5 = 10
res.rlsourc n3 n7 = 17

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-8e-7
res.rdrain n50 n16 = 2.9e-3, tc1=1e-4,tc2=8e-6
res.rgate n9 n20 = 2.2
res.rslc1 n5 n51 = 1e-6, tc1=9e-4,tc2=1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 2.7e-3, tc1=7.5e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-1.7e-3,tc2=-8.2e-7
res.rvtemp n18 n19 = 1, tc1=-2.6e-3,tc2=2e-7
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/300))** 10))
}
}

```



PSPICE Thermal Model

REV 23 January 2004

FDD8876T

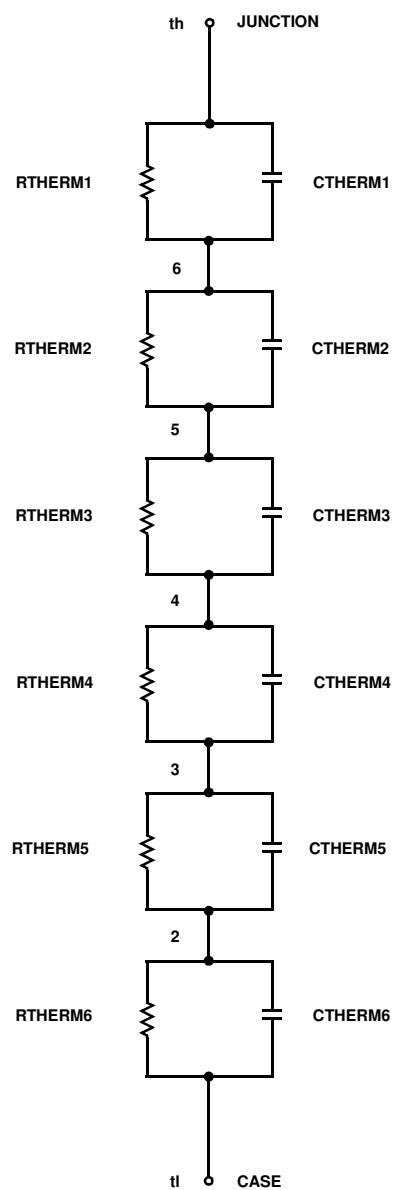
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 CTHERM2 6 5 9e-4
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 CTHERM5 3 2 6e-3
 CTHERM6 2 TL 1.1e-2

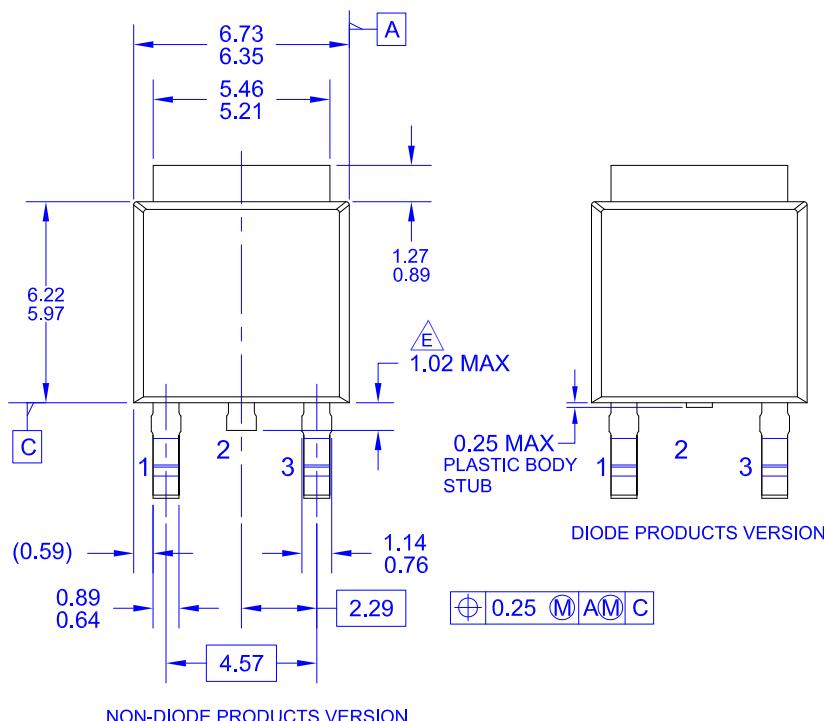
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 RTHERM6 2 TL 5e-1

SABER Thermal ModelSABER thermal model FDD8876T
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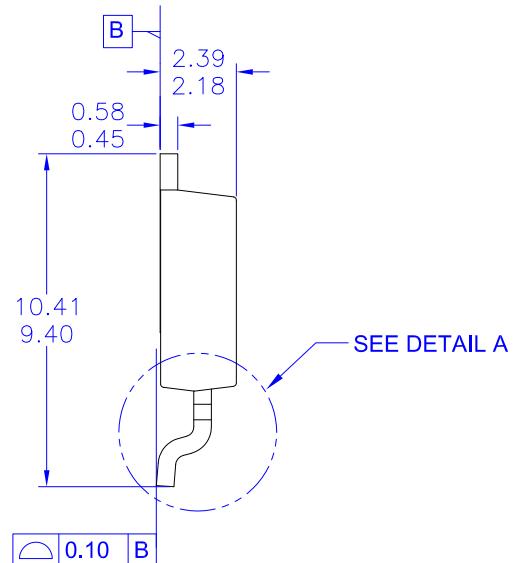
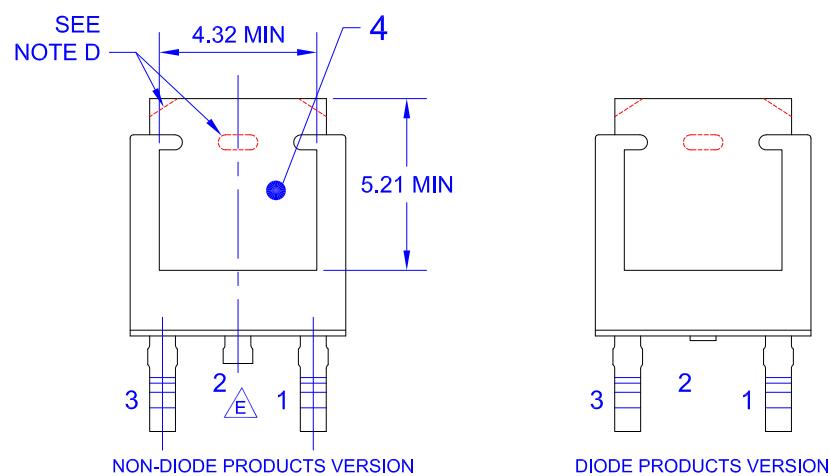
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{
  ctherm.ctherm1 th 6 =7e-4
  ctherm.ctherm2 6 5 =9e-4
  ctherm.ctherm3 5 4 =2e-3
  ctherm.ctherm4 4 3 =2.5e-3
  ctherm.ctherm5 3 2 =6e-3
  ctherm.ctherm6 2 tl =1.1e-2

  rtherm.rtherm1 th 6 =7.0e-2
  rtherm.rtherm2 6 5 =1.1e-1
  rtherm.rtherm3 5 4 =2.2e-1
  rtherm.rtherm4 4 3 =3.2e-1
  rtherm.rtherm5 3 2 =4.9e-1
  rtherm.rtherm6 2 tl =5e-1
}
```





LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252,
ISSUE C, VARIATION AA

B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PFF

- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED

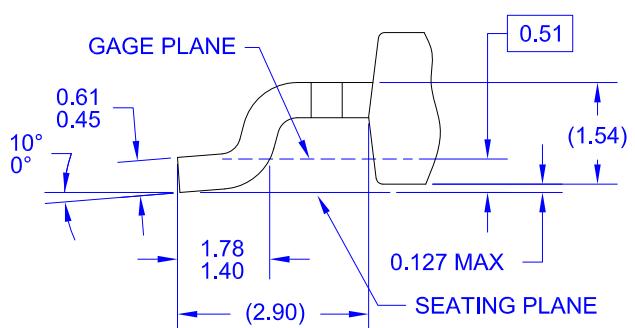
△ CORNERS OR EDGE PROTRUSION.
△ TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD
TO228P991X239-3N.

H) DRAWING NUMBER

47 DRAWING NUMBER AND REVISION HISTORY RELEASES/REVIEWS



DETAIL A
(ROTATED -90°)
SCALE: 12X

The Fairchild logo consists of the word "FAIRCHILD" in a bold, black, sans-serif font, with a registered trademark symbol (TM) at the end. A red, stylized "F" graphic is positioned behind the text, with its top bar extending diagonally upwards and to the right, and its bottom bar forming a diagonal line that meets the text at the letter "A".



TRADEMARKS

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 AttitudeEngine™
 Awinda®
 AX-CAP®*
 BitSiC™
 Build it Now™
 CorePLUS™
 CorePOWER™
 CROSSVOLT™
 CTL™
 Current Transfer Logic™
 DEUXPEED®
 Dual Cool™
 EcosPARK®
 EfficientMax™
 ESBC™
 F®
 Fairchild®
 Fairchild Semiconductor®
 FACT Quiet Series™
 FACT®
 FAST®
 FastvCore™
 FETBench™
 FPS™
 F-PFS™
 FRFET®
 Global Power Resource™
 GreenBridge™
 Green FPS™
 Green FPS™ e-Series™
 Gmax™
 GTO™
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 ISOPLANAR™
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 MegaBuck™
 MICROCOUPLER™
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 QFET®
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 SmartMax™
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 Solutions for Your Success™
 SPM®
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 SuperFET®
 SuperSOT™-3
 SuperSOT™-6
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 SupreMOS®
 SyncFET™
 Sync-Lock™

SYSTEM GENERAL®
 TinyBoost®
 TinyBuck®
 TinyCalc™
 TinyLogic®
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 TinyPower™
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