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FAIRCHILD SEMICONDUCTOR TM

August 2001

# FDFS2P102A

## Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

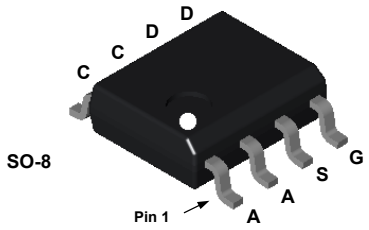
### General Description

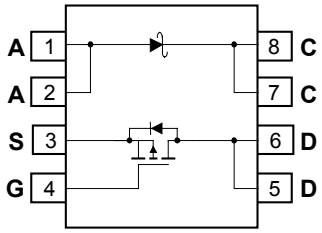
The FDFS2P102A combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SO-8 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

### Features

- –3.3 A, –20V $R_{DS(ON)}$ = 125 mΩ @ $V_{GS}$ = –10 V
  $R_{DS(ON)}$ = 200 mΩ @ $V_{GS}$ = –4.5 V
- $V_F$ < 0.39 V @ 1 A ($T_J$ = 125°C)
  $V_F$ < 0.47 V @ 1 A
  $V_F$ < 0.58 V @ 2 A
- Schottky and MOSFET incorporated into single power surface mount SO-8 package
- Electrically independent Schottky and MOSFET pinout for design flexibility




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | MOSFET Drain-Source Voltage | | –20 | V |
| $V_{GSS}$ | MOSFET Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | –3.3 | A |
| | – Pulsed | | –10 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2 | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | |
| | | (Note 1b) | 1 | |
| | | (Note 1c) | 0.9 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |
| $V_{RRM}$ | Schottky Repetitive Peak Reverse Voltage | | 20 | V |
| $I_O$ | Schottky Average Forward Current | (Note 1a) | 1 | A |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDFS2P102A | FDFS2P102A | 13'' | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

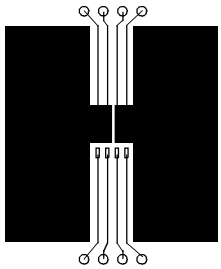
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 μA | –20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 μA,Referenced to 25°C | | –23 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | | | –1 | μA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –20 V, $V_{DS}$ = 0 V | | | –100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | –1 | –1.8 | –3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 μA,Referenced to 25°C | | 4.4 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –10 V, $I_D$ = –3.3 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –2.5 A<br>$V_{GS}$=–10 V, $I_D$ =–3.3A, $T_J$=125°C | | 96<br>152<br>137 | 125<br>200<br>190 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –10 V, $V_{DS}$ = –5 V | –10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5V, $I_D$ = –3.3 A | | 4.6 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 182 | | pF |
| $C_{oss}$ | Output Capacitance | | | 60 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 24 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –10 V, $I_D$ = –1 A, $V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | | 5 | 10 | ns |
| $t_r$ | Turn–On Rise Time | | | 14 | 52 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 11 | 20 | ns |
| $t_f$ | Turn–Off Fall Time | | | 2 | 4 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –10 V, $I_D$ = –3.3 A, $V_{GS}$ = –5 V | | 2.1 | 3.0 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 1.0 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 0.6 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | –1.3 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –1.3 A (Note 2) | | –0.8 | –1.2 | V |
| **Schottky Diode Characteristics** | | | | | | |
| $I_R$ | Reverse Leakage | $V_R$ = 20 V, $T_J$ = 25°C | | | 50 | μA |
| | | $V_R$ = 20 V, $T_J$ = 125°C | | | 18 | mA |
| $V_F$ | Forward Voltage | $I_F$ = 1 A, $T_J$ = 25°C | | | 0.47 | V |
| | | $I_F$ = 1 A, $T_J$ = 125°C | | | 0.39 | |
| | | $I_F$ = 2 A, $T_J$ = 25°C | | | 0.58 | |
| | | $I_F$ = 2 A, $T_J$ = 125°C | | | 0.53 | |

## Thermal Characteristics

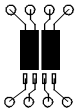
| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

**Notes:**

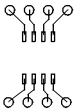
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a $0.5in^2$ pad of 2 oz copper



b) 125°C/W when mounted on a $0.02\ in^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Characteristics

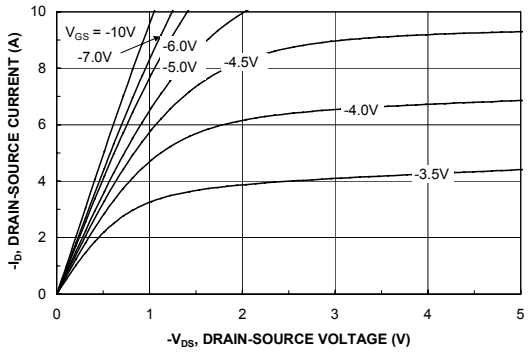



**Figure 1. On-Region Characteristics.**

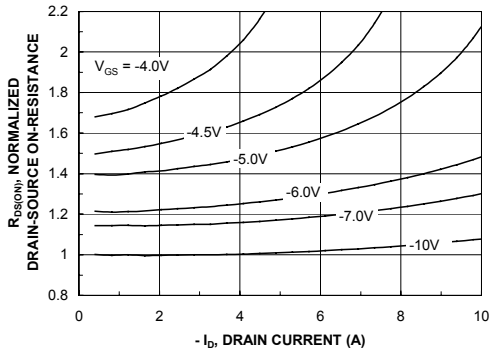



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

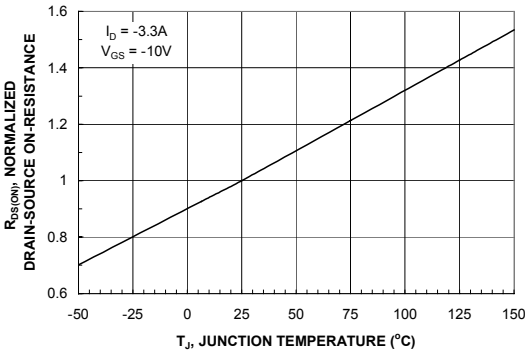



**Figure 3. On-Resistance Variation with Temperature.**

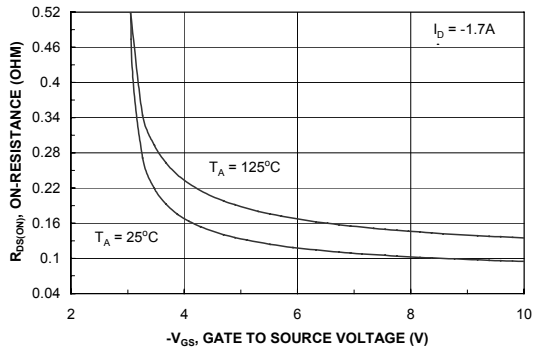



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

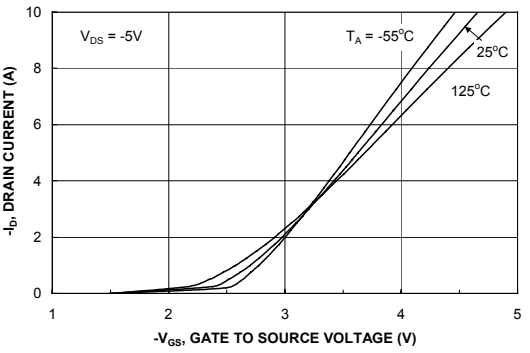



**Figure 5. Transfer Characteristics.**

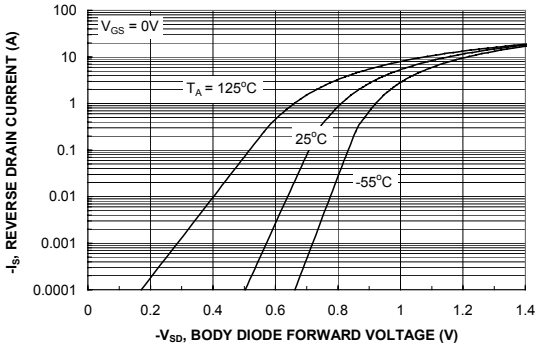



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

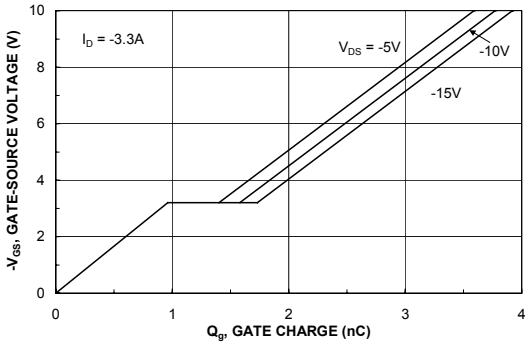



**Figure 7. Gate Charge Characteristics.**

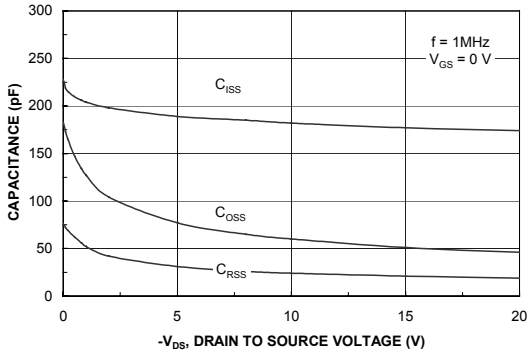



**Figure 8. Capacitance Characteristics.**

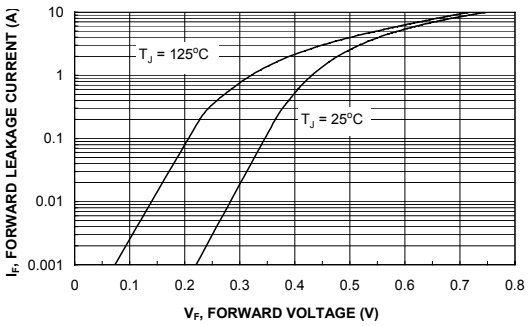



**Figure 9. Schottky Diode Forward Voltage.**

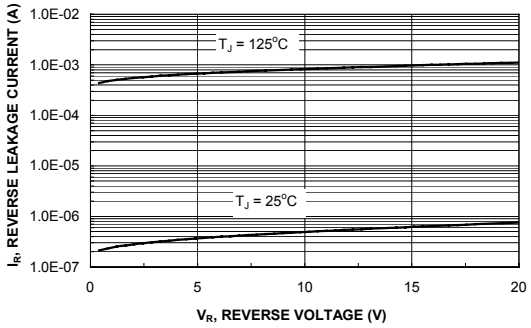



**Figure 10. Schottky Diode Reverse Current.**

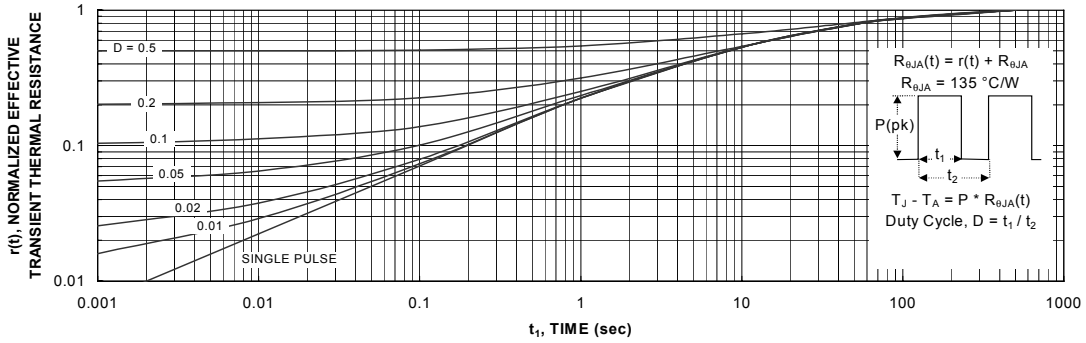



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

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