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FDG1024NZ Dual N-Channel PowerTrench[®] MOSFET 20 V, 1.2 A, 175 m Ω

Features

- Max $r_{DS(on)}$ = 175 m Ω at V_{GS} = 4.5 V, I_D = 1.2 A
- Max $r_{DS(on)}$ = 215 m Ω at V_{GS} = 2.5 V, I_D = 1.0 A
- Max $r_{DS(on)} = 270 \text{ m}\Omega$ at $V_{GS} = 1.8 \text{ V}$, $I_D = 0.9 \text{ A}$
- Max $r_{DS(on)}$ = 389 m Ω at V_{GS} = 1.5 V, I_D = 0.8 A

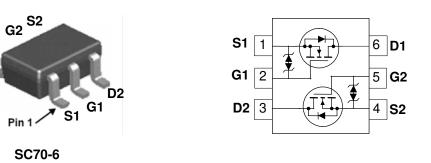
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- HBM ESD protection level >2 kV (Note 3)
- Very low level gate drive requirements allowing operation in 1.5 V circuits (V_{GS(th)} < 1 V)</p>
- Very small package outline SC70-6
- RoHS Compliant



General Description

This dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Para	meter		Ratings	Units
V _{DS}	Drain to Source Voltage			20	V
V _{GS}	Gate to Source Voltage			±8	V
	-Continuous	$T_A = 25^{\circ}C$	(Note 1a)	1.2	٨
D	-Pulsed			6	A
D	Power Dissipation	T _A = 25°C	(Note 1a)	0.36	w
P _D	Power Dissipation	T _A = 25°C	(Note 1b)	0.30	vv
T _J , T _{STG}	Operating and Storage Junction Tempe	erature Range		-55 to +150	°C

Thermal Characteristics

$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	350	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	415	0/11

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.4N	FDG1024NZ	SC70-6	7 "	8 mm	3000 units

June 2010

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0 \ V$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu\text{A}$, referenced to 25 °C		14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8 V, V_{DS} = 0 V$			±10	μA

Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$	0.4	0.8	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu\text{A}$, referenced to 25 °C		-3		mV/°C
	DS(on) Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 1.2 \text{ A}$		160	175	
		$V_{GS} = 2.5 \text{ V}, I_D = 1.0 \text{ A}$		185	215	
r		$V_{GS} = 1.8 \text{ V}, I_D = 0.9 \text{ A}$		232	270	mΩ
DS(on)		$V_{GS} = 1.5 \text{ V}, \ I_D = 0.8 \text{ A}$		321	389	- 11152
		V _{GS} = 4.5 V, I _D = 1.2 A, T _J =125 °C		220	259	
9 _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 1.2 A		4		S

Dynamic Characteristics

C _{iss}	Input Capacitance		115	150	pF
Coss	Output Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	25	35	pF
C _{rss}	Reverse Transfer Capacitance		20	25	pF
Rg	Gate Resistance		4.6		Ω

Switching Characteristics

	5				
t _{d(on)}	Turn-On Delay Time		3.7	10	ns
t _r	Rise Time	V _{DD} = 10 V, I _D = 1.2 A,	1.7	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 4.5 \text{ V}, \text{ R}_{GEN} = 6 \Omega$	11	19	ns
t _f	Fall Time		1.5	10	ns
Qg	Total Gate Charge	V 45VV 40V	1.8	2.6	nC
Q _{gs}	Gate to Source Charge	$V_{GS} = 4.5 \text{ V}, \text{ V}_{DD} = 10 \text{ V},$ $I_D = 1.2 \text{ A}$	0.3		nC
Q _{gd}	Gate to Drain "Miller" Charge		0.4		nC

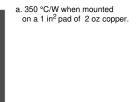
Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain-Source Diode Forward Current				0.3	Α
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 0.3 A$ (Note 2)		0.7	1.2	V
t _{rr}	Reverse Recovery Time	1 1 2 A di/dt 100 A/		10	20	ns
Q _{rr}	Reverse Recovery Charge	I _F = 1.2 A, di/dt = 100 A/μs		1.9	10	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.





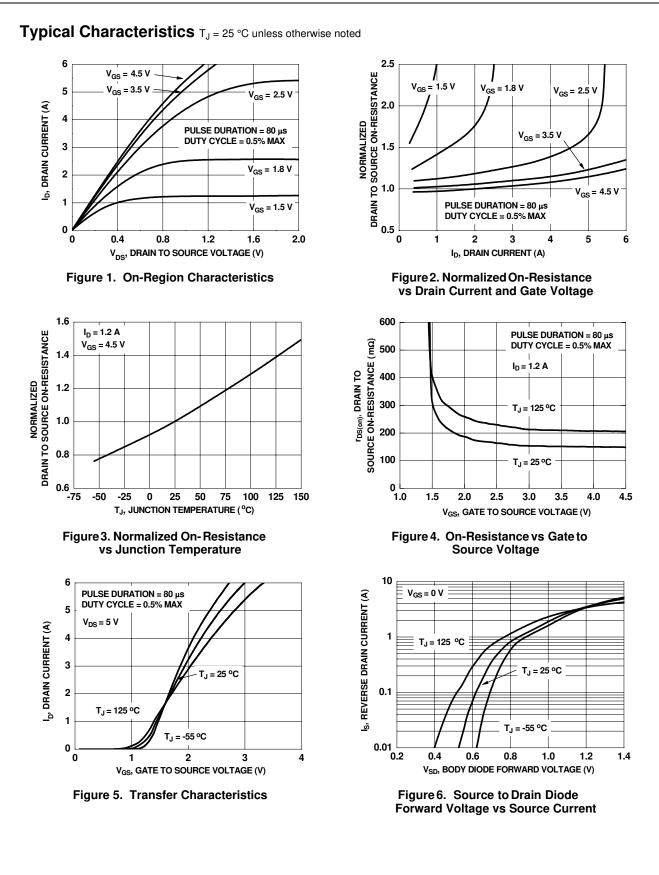
b. 415 °C/W when mounted on a minimum pad of 2 oz copper.



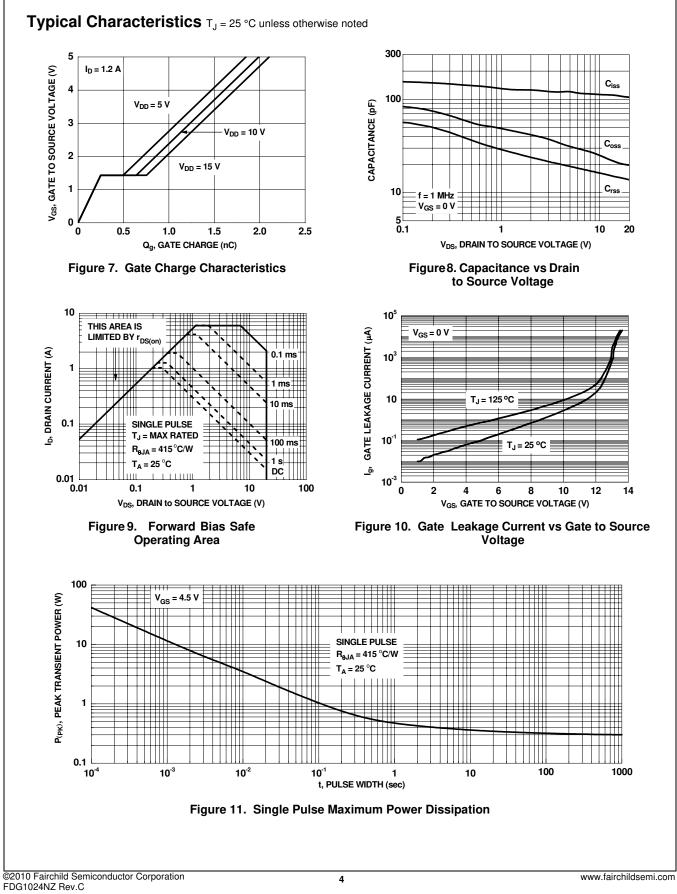
Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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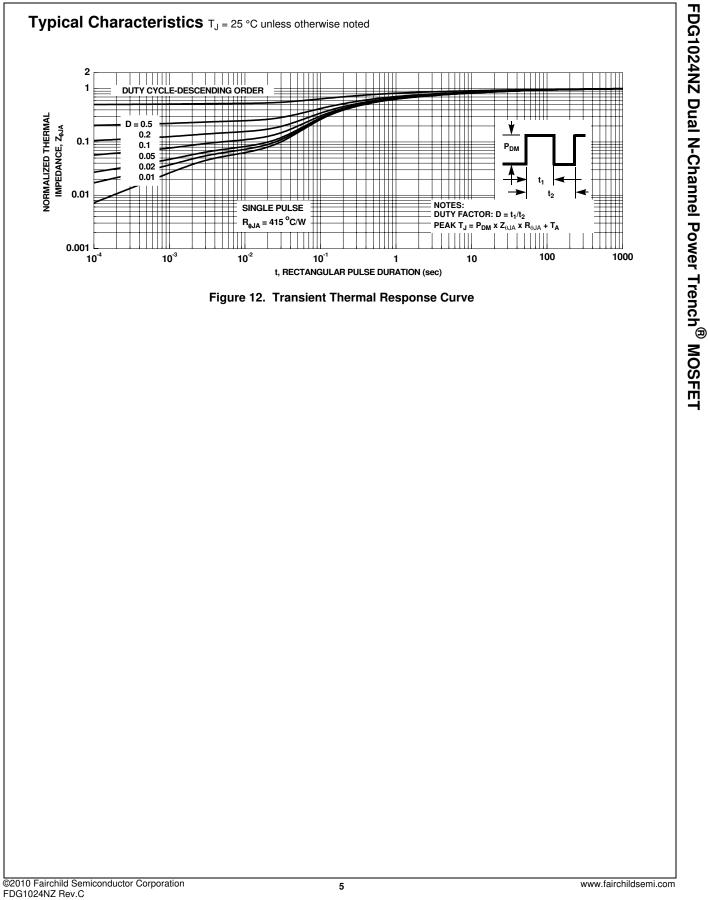
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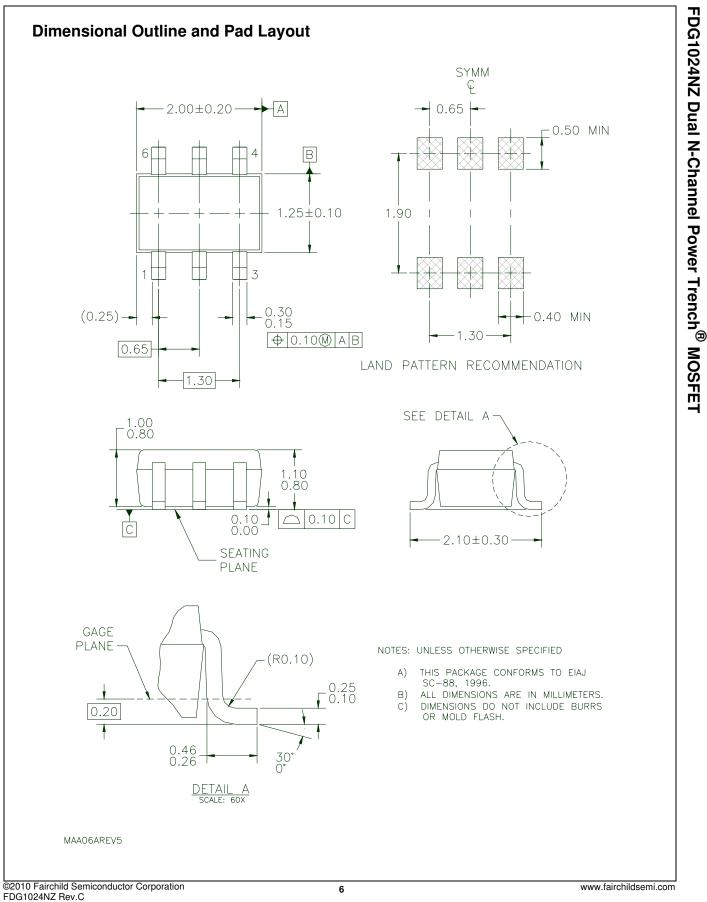


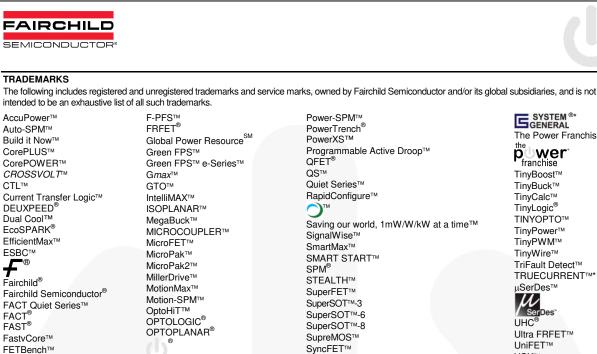
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FDG1024NZ Dual N-Channel Power Trench[®] MOSFET







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PDP SPM™

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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