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FDG6304P Dual P-Channel, Digital FET

General Description

These dual P-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs.

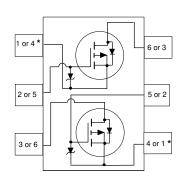
Features

= -25 V, -0.41 A continuous, -1.5 A peak. $R_{\text{DS(ON)}} = 1.1~\Omega~\textcircled{0}~V_{\text{GS}} = -4.5~\text{V}, \\ R_{\text{DS(ON)}} = 1.5~\Omega~\textcircled{0}~V_{\text{GS}} = -2.7~\text{V}.$

- Very low level gate drive requirements allowing direct operation in 3 V circuits (V_{GS(th)} < 1.5 V).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.

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SC70-6	SOT-23	SuperSOT [™] -6	SuperSOT™-8	SO-8	SOT-223





^{*}The pinouts are symmetrical; pin 1 and 4 are interchangeable.

Units inside the carrier can be of either orientation and will not affect the functionality of the device.

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	FDG6304P	Units
V _{DSS}	Drain-Source Voltage	-25	V
V_{GSS}	Gate-Source Voltage	-8	V
I _D	Drain/Output Current - Continuous	-0.41	A
	- Pulsed	-1.5	
P_{D}	Maximum Power Dissipation (Note 1)	0.3	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6.0	kV
THERMA	L CHARACTERISTICS		·
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	°C/W

Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHAR	ACTERISTICS	•		'		•
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-25			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		-22		mV /°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = -20 \text{ V}, \ V_{GS} = 0 \text{ V}$			-1	μΑ
		T _J = 55°C			-10	μΑ
GSS	Gate - Body Leakage Current	$V_{GS} = -8 \text{ V}, \ V_{DS} = 0 \text{ V}$			-100	nA
ON CHARAC	CTERISTICS (Note 2)	·		•		
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-0.65	-0.82	-1.5	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp.Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		2		mV /°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -4.5 \text{ V}, \ I_D = -0.41 \text{ A}$		0.85	1.1	Ω
		T _J =125°C		1.2	1.9	
		$V_{GS} = -2.7 \text{ V}, I_D = -0.25 \text{ A}$		1.15	1.5	
D(ON)	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, \ V_{DS} = -5 \text{ V}$	-1.5			Α
9 _{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}, \ I_{D} = -0.41 \text{ A}$		0.9		S
DYNAMIC CI	HARACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = 10 \text{ V}, \ V_{GS} = 0 \text{ V}, $ f = 1.0 MHz		62		pF
Coss	Output Capacitance	f = 1.0 MHZ		34		pF
O _{rss}	Reverse Transfer Capacitance			10		pF
SWITCHING	CHARACTERISTICS (Note 2)		•			
D(on)	Turn - On Delay Time	$V_{DD} = -5 \text{ V}, I_{D} = -0.5 \text{ A},$		7	15	ns
r	Turn - On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		8	16	ns
D(off)	Turn - Off Delay Time			55	80	ns
f	Turn - Off Fall Time			35	60	ns
Q_g	Total Gate Charge	$V_{DS} = -5 \text{ V}, I_{D} = -0.41 \text{ A}, V_{GS} = -4.5 \text{ V}$		1.1	1.5	nC
\mathbf{Q}_{gs}	Gate-Source Charge			0.31		nC
Q_{gd}	Gate-Drain Charge			0.29		nC
DRAIN-SOU	RCE DIODE CHARACTERISTICS AND MAXIM	UM RATINGS				
S	Maximum Continuous Source Current				-0.25	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -0.25 \text{ A (Note 2)}$		-0.85	-1.2	V

Notes:

1. R_{b,M} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{b,M} is guaranteed by design while R_{gcA} is determined by the user's board design. $R_{g_0A} = 415^{\circ}\text{C/W}$ on minimum pad mounting on FR-4 board in still air. 2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

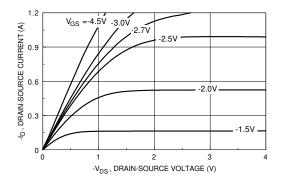


Figure 1. On-Region Characteristics.

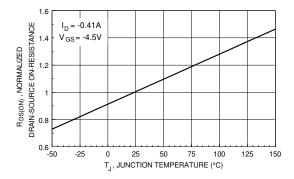


Figure 3. On-Resistance Variation with Temperature.

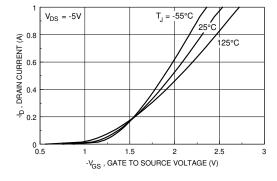


Figure 5. Transfer Characteristics.

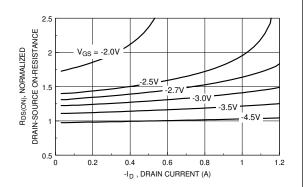


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

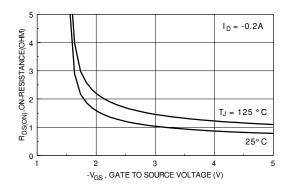


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

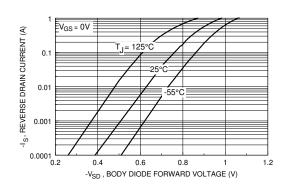


Figure 6. Body Diode Forward Voltage
Variation with Source Current
and Temperature.

Typical Electrical Characteristics

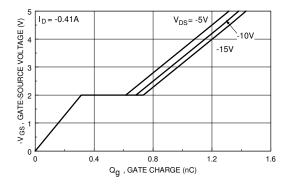


Figure 7. Gate Charge Characteristics.

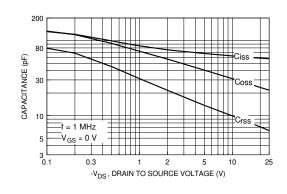


Figure 8. Capacitance Characteristics.

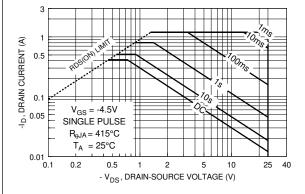


Figure 9. Maximum Safe Operating Area.

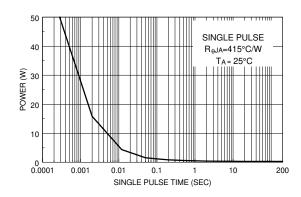


Figure 10. Single Pulse Maximum Power Dissipation.

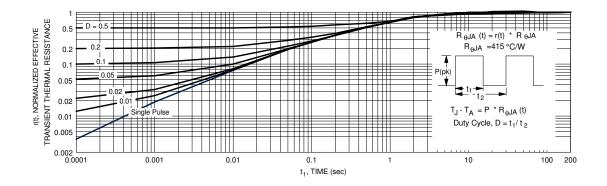


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1. Transient thermalresponse will change depending on the circuit board design.

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