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FAIRCHILD SEMICONDUCTOR®

August 2006

# FDJ1028N
# N-Channel 2.5 Vgs Specified PowerTrench® MOSFET

## Features

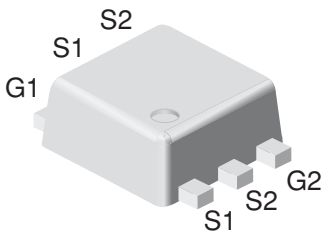
- 3.2 A, 20 V. $R_{DS(ON)}$ = 90 mΩ @ $V_{GS}$ = 4.5 V
  $R_{DS(ON)}$ = 130 mΩ @ $V_{GS}$ = 2.5 V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- FLMP SC75 package: Enhanced thermal performance in industry-standard package size

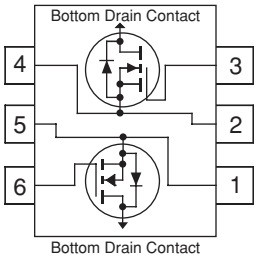
## Applications

- Battery management

## General Description

This dual N-Channel 2.5V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. Packaged in FLMP SC75, the $R_{DS(ON)}$ and thermal properties of the device are optimized for battery power management applications.




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | ±12 | V |
| $I_D$ | Drain Current – Continuous (Note 1a) | 3.2 | A |
| | – Pulsed | 12 | |
| $P_D$ | Power Dissipation for single Operation (Note 1a) | 1.5 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | –55 to +150 | °C |
| **Thermal Characteristics** | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1a) | 80 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 5 | |

## Packge Marking and Ordering Information

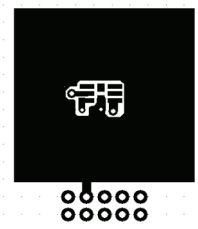
| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| .F | FDJ1028N | 7" | 8mm | 3000 units |

## Electrical Characteristics $T_A$ = 25°C unless otherwise noted

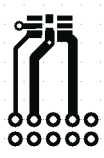
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | 13 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 0.6 | 1.0 | 1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | –3 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 3.2 A<br>$V_{GS}$ = 2.5 V, $I_D$ = 2.7 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 3.2A, $T_J$ = 125°C | | 70<br>100<br>83 | 90<br>130<br>132 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 3.2 A | | 7.5 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 200 | | pF |
| $C_{oss}$ | Output Capacitance | | | 50 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 30 | | pF |
| $R_G$ | Gate Resistance | f = 1.0 MHz | | 3 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 10 V, $I_D$ = 1 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 6 Ω | | 7 | 14 | ns |
| $t_r$ | Turn–On Rise Time | | | 8 | 16 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 11 | 20 | ns |
| $t_f$ | Turn–Off Fall Time | | | 2 | 4 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 10 V, $I_D$ = 3.2 A, $V_{GS}$ = 4.5 V | | 2 | 3 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 0.4 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 1.0 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 1.25 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.25 A (Note 2) | | 0.8 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 3.2 A, $d_{iF}/d_t$ = 100 A/μs | | 11 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 2.5 | | nC |

**Notes:**

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 80°C/W when mounted on a $1in^2$ pad of 2 oz copper (Single Operation).



b) 140°C/W when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Characteristics

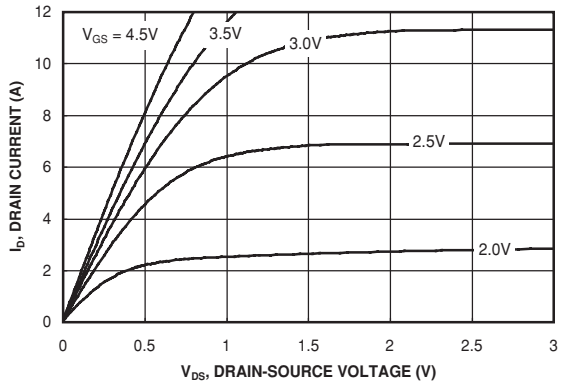



**Figure 1. On-Region Characteristics.**

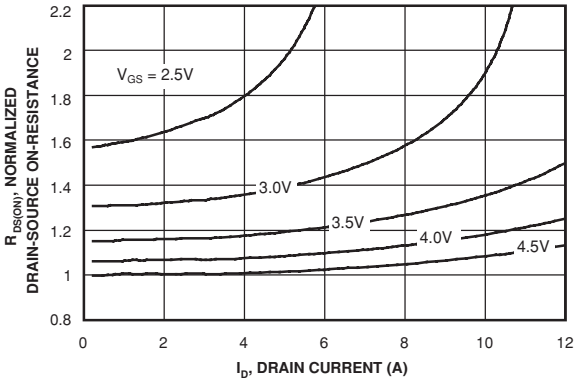



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

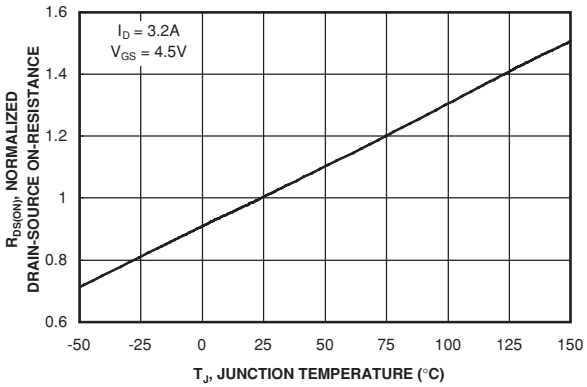



**Figure 3. On-Resistance Variation with Temperature.**

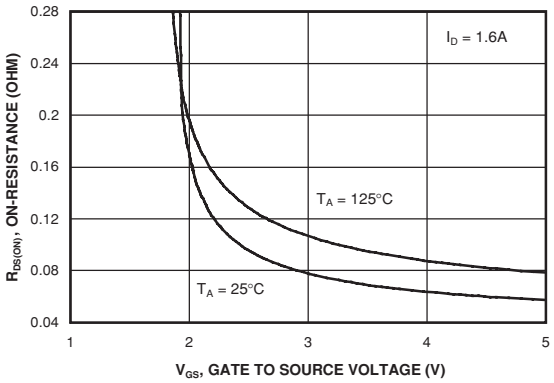



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

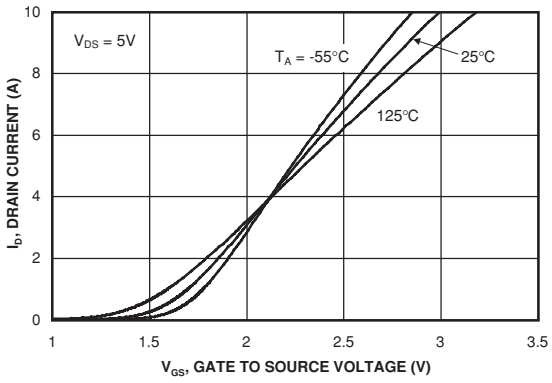



**Figure 5. Transfer Characteristics.**

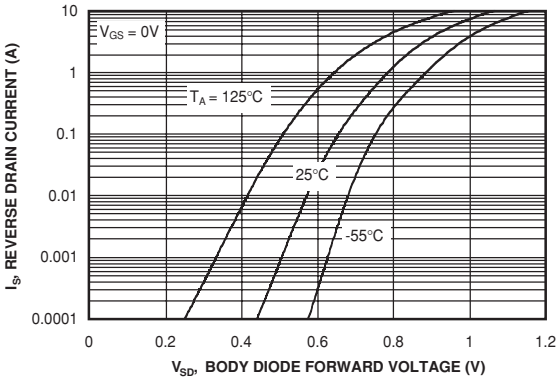



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

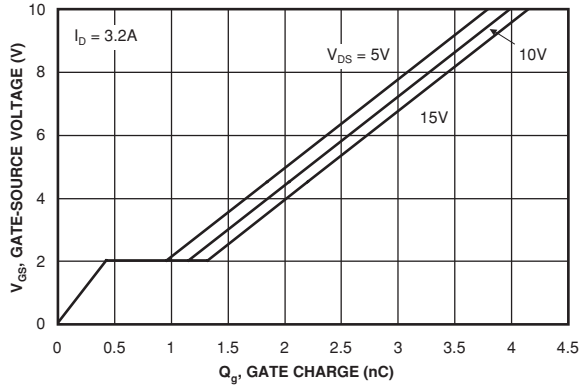



**Figure 7. Gate Charge Characteristics.**

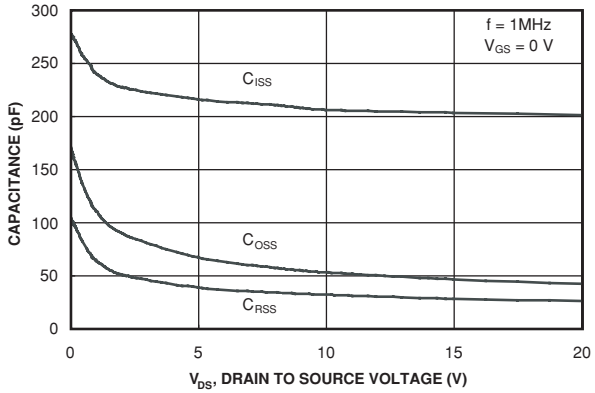



**Figure 8. Capacitance Characteristics.**

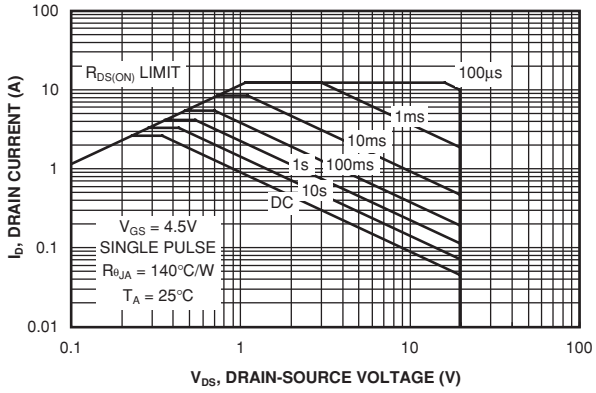



**Figure 9. Maximum Safe Operating Area.**

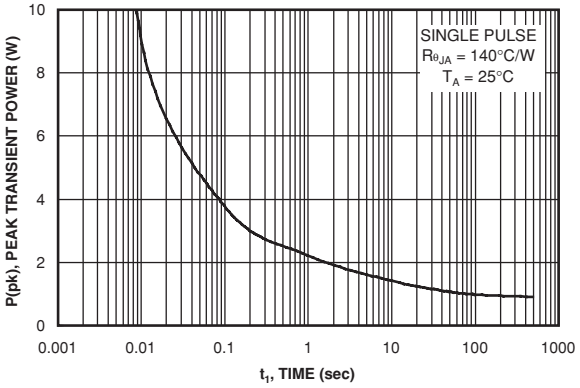



**Figure 10. Single Pulse Maximum Power Dissipation.**

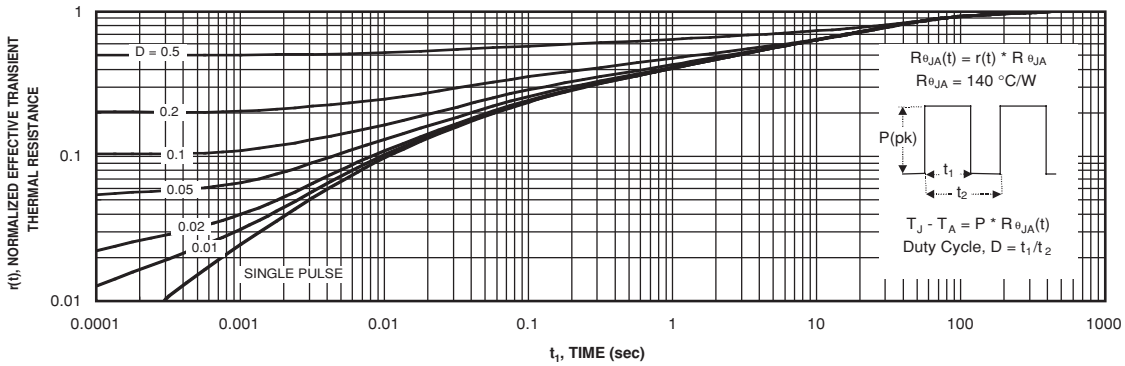
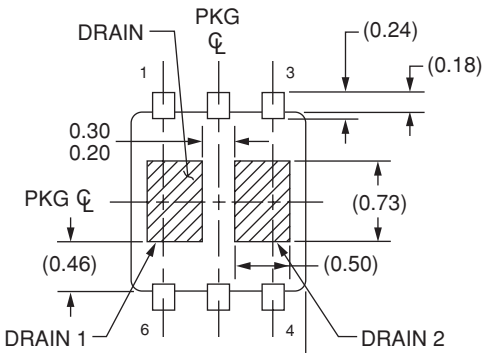


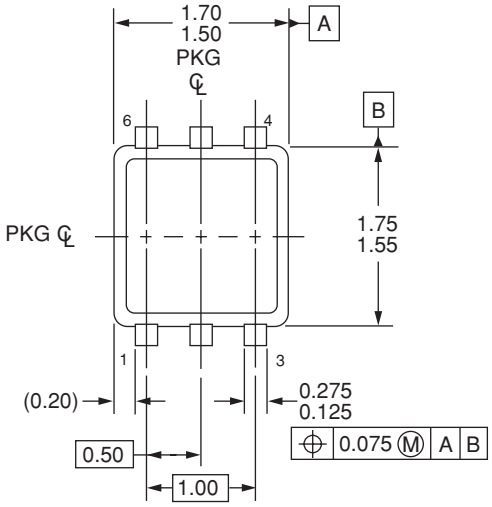

**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1b.**
**Transient thermal response will change depending on the circuit board design.**

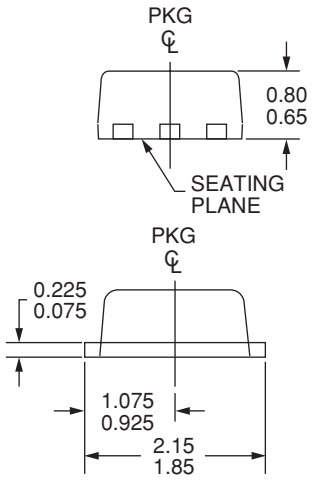
## Dimensional Outline and Pad Layout

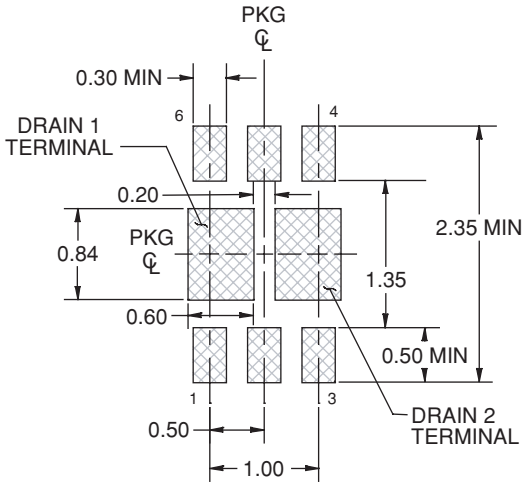



**Bottom View**




**Top View**




**Recommended Landing Pattern**

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