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# FDMC7208S

## Dual N-Channel PowerTrench® MOSFET

Q1: 30 V, 12 A, 9.0 mΩ Q2: 30 V, 16 A, 6.4 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 9.0 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 12\text{ A}$
- Max  $r_{DS(on)}$  = 11.0 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 11\text{ A}$

Q2: N-Channel

- Max  $r_{DS(on)}$  = 6.4 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 16\text{ A}$
- Max  $r_{DS(on)}$  = 7.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 13.5\text{ A}$
- Termination is Lead-free and RoHS Compliant

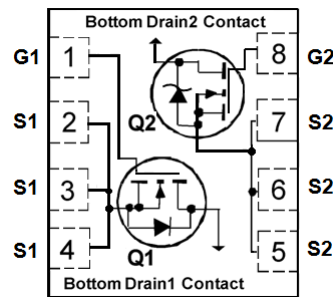
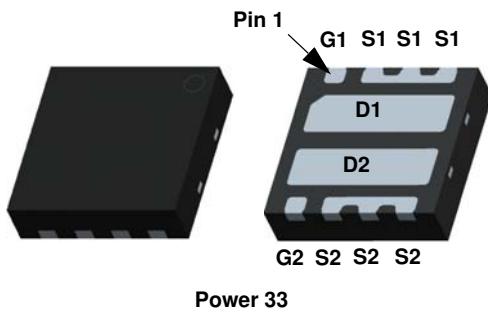


### General Description

This device includes two 30V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

### Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook System



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	±20	±12	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	22	26	A
	-Continuous $T_A = 25\text{ °C}$	12 <sup>1a</sup>	16 <sup>1b</sup>	
	-Pulsed	60	80	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	21	21	mJ
$P_D$	Power Dissipation for Single Operation $T_A = 25\text{ °C}$	1.9 <sup>1a</sup>	1.9 <sup>1b</sup>	W
	Power Dissipation for Single Operation $T_A = 25\text{ °C}$	0.8 <sup>1c</sup>	0.8 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 <sup>1a</sup>	65 <sup>1b</sup>	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	155 <sup>1c</sup>	155 <sup>1d</sup>	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7208S	FDMC7208S	Power 33	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		27 21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = 12\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			100 100	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	1.2 1.2	1.7 1.6	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = 10\text{ mA}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-5 -3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 11\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q1		6.7 8.8 9.2	9.0 11.0 12.4	m $\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 13.5\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	Q2		4.7 5.3 6.4	6.4 7.5 6.8	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 12\text{ A}$ $V_{DS} = 5\text{ V}$ , $I_D = 16\text{ A}$	Q1 Q2		53 80		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1: $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		848 1685	1130 2245	pF
$C_{oss}$	Output Capacitance	Q2: $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		270 432	360 575	pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		36 42	55 65	pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	1.1 1.0	2.5 2.5	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}$ , $I_D = 12\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$ Q2: $V_{DD} = 15\text{ V}$ , $I_D = 16\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		6 7	12 14	ns	
$t_r$	Rise Time		Q1 Q2		2 3	10 10	ns	
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		16 23	29 36	ns	
$t_f$	Fall Time		Q1 Q2		2 2	10 10	ns	
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V}$ to $10\text{ V}$	Q1 $V_{DD} = 15\text{ V}$ , $I_D = 12\text{ A}$	Q1 Q2		13 26	18 36	nC
				Q1 Q2		6.7 14	9.4 20	nC
$Q_{gs}$	Gate to Source Gate Charge	Q2 $V_{DD} = 15\text{ V}$ , $I_D = 16\text{ A}$	Q1 Q2		2.3 3.9		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		1.8 2.7		nC	

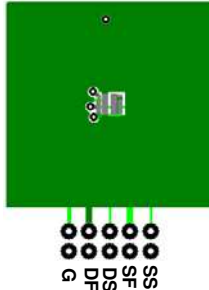


**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

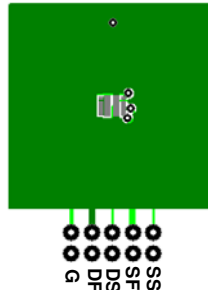
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q1		0.72	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2)	Q1		0.82	1.2	
		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q2		0.70	1.2	
		$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$ (Note 2)	Q2		0.82	1.2	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		21	34	ns
			Q2		21	33	
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = 16\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		6	12	nC
			Q2		16	28	

Notes:

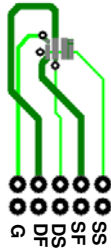
1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 155 °C/W when mounted on a minimum pad of 2 oz copper



d. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Q1:  $E_{AS}$  of 21 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 3\text{ mH}$ ,  $I_{AS} = 5.2\text{ A}$ .

Q1:  $E_{AS}$  of 21 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 3\text{ mH}$ ,  $I_{AS} = 5.4\text{ A}$ .

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted

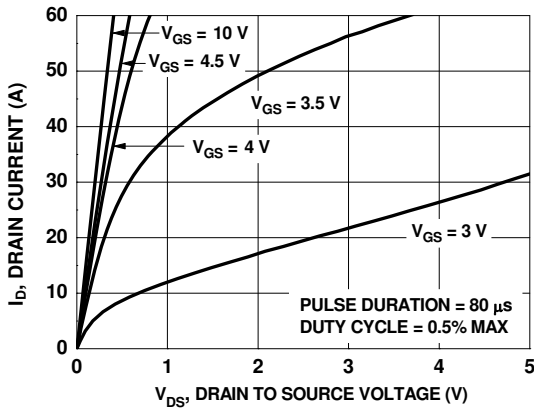


Figure 1. On Region Characteristics

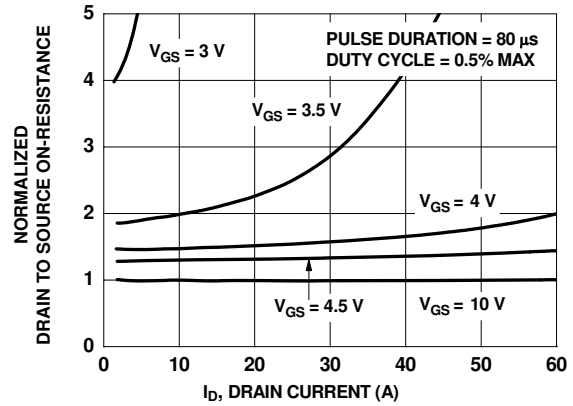


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

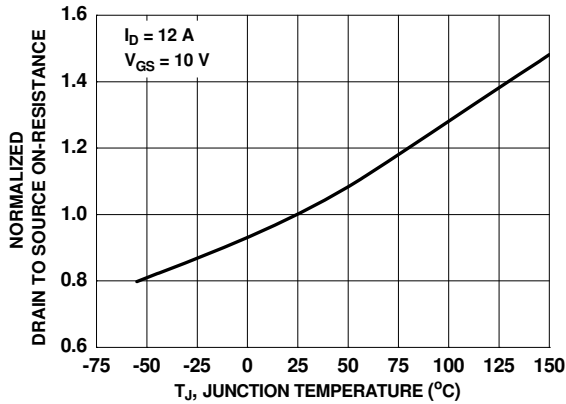


Figure 3. Normalized On Resistance vs Junction Temperature

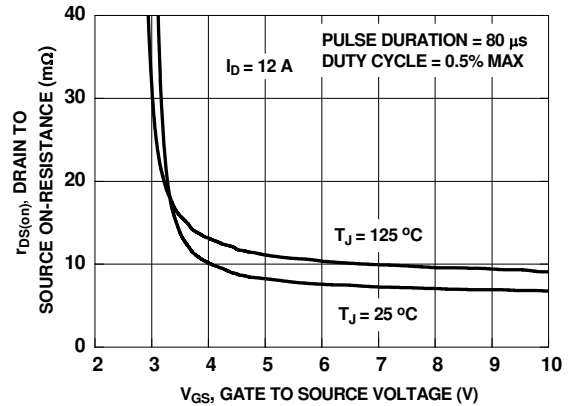


Figure 4. On-Resistance vs Gate to Source Voltage

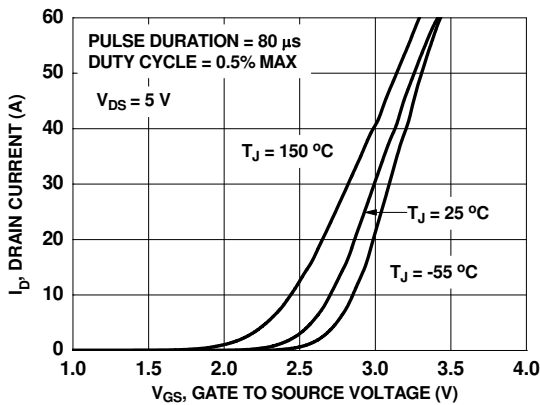


Figure 5. Transfer Characteristics

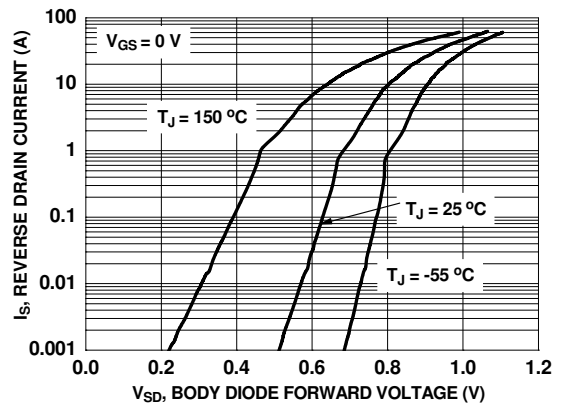
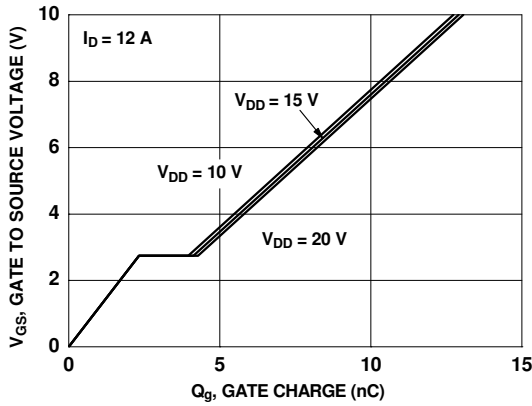
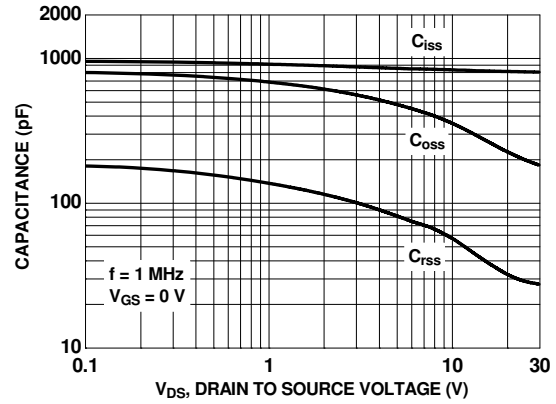


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

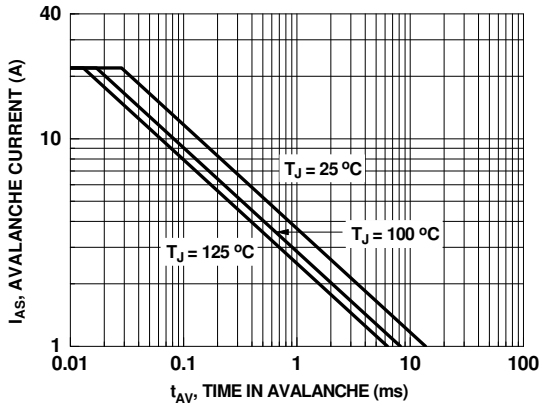
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



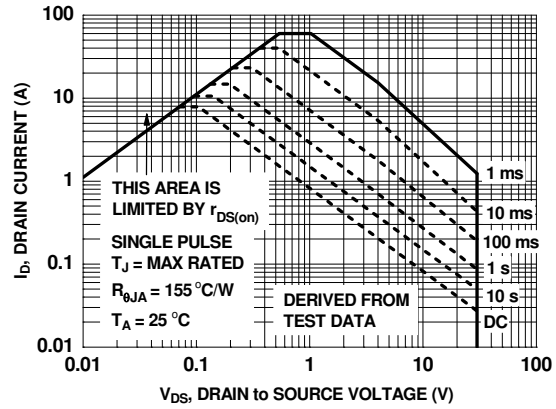
**Figure 7. Gate Charge Characteristics**



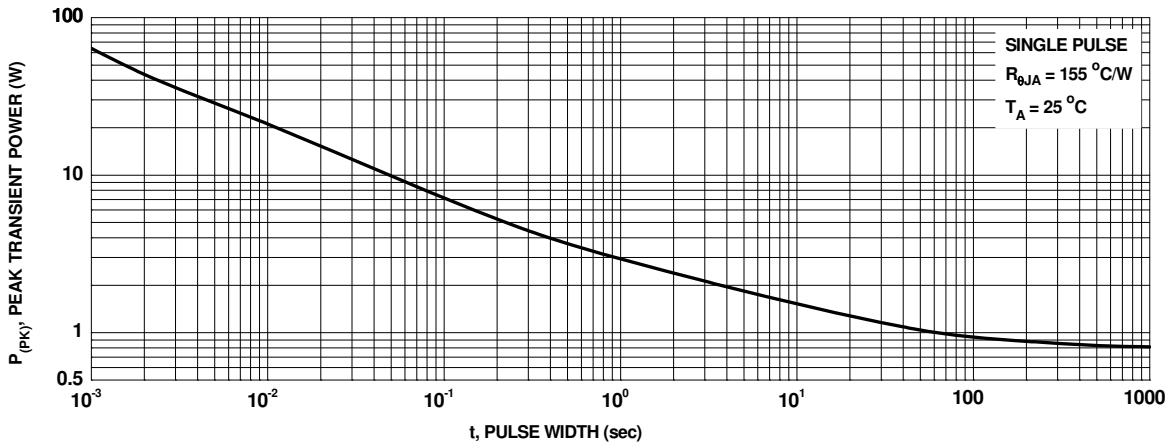
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**

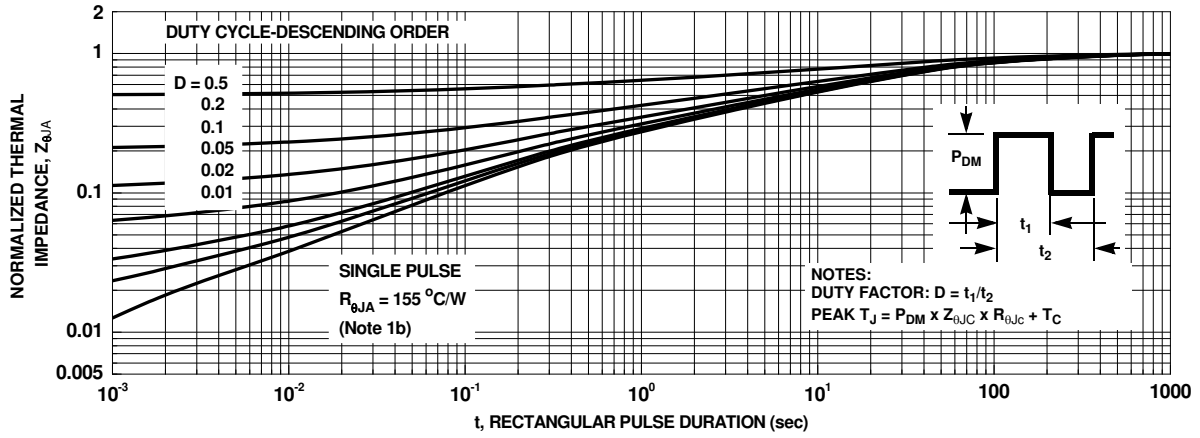


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

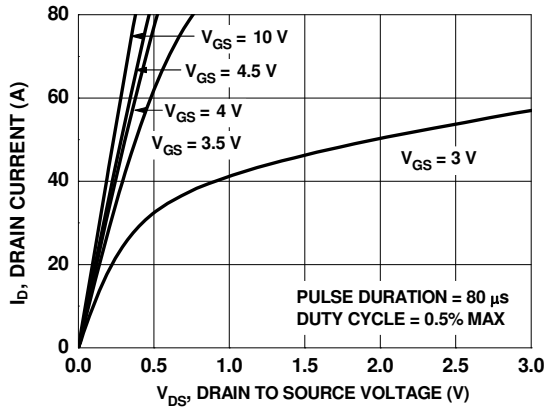
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



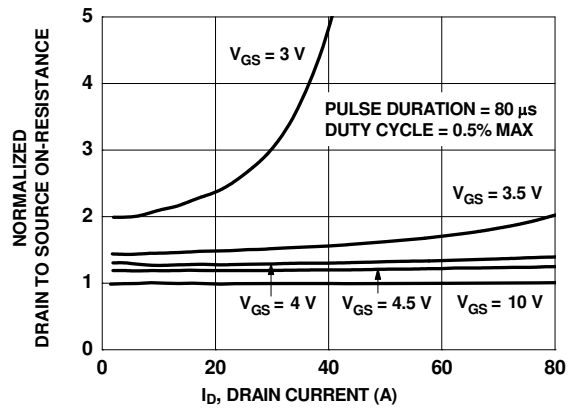
**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**



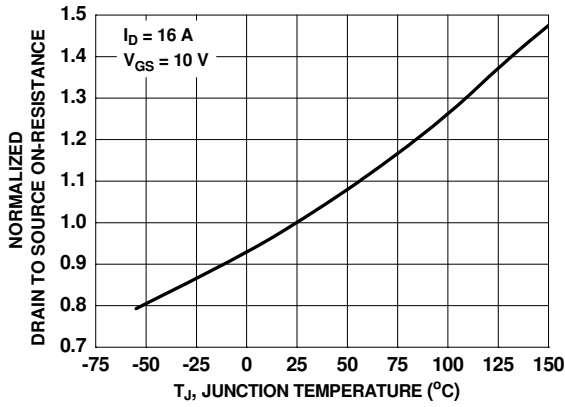
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



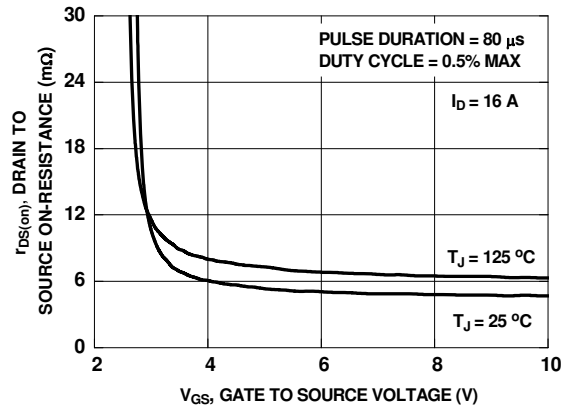
**Figure 14. On-Region Characteristics**



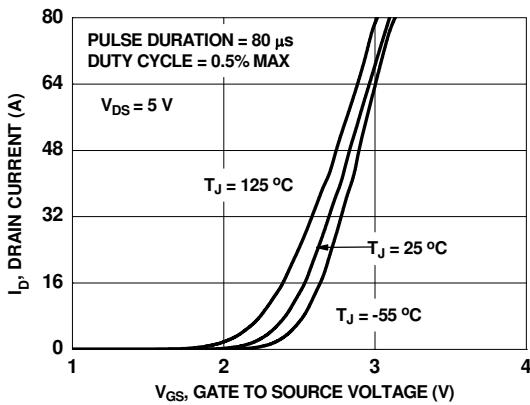
**Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage**



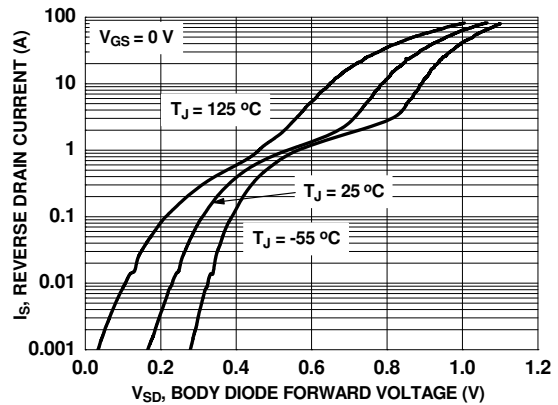
**Figure 16. Normalized On-Resistance vs Junction Temperature**



**Figure 17. On-Resistance vs Gate to Source Voltage**

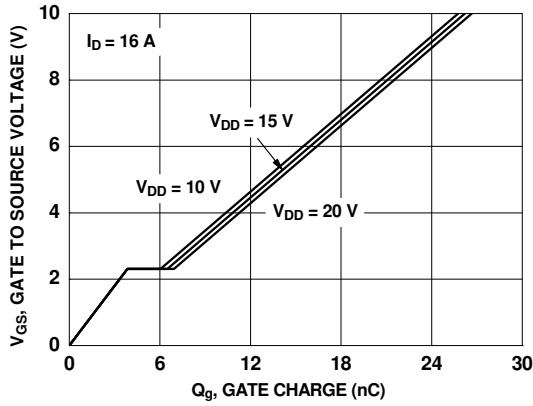


**Figure 18. Transfer Characteristics**

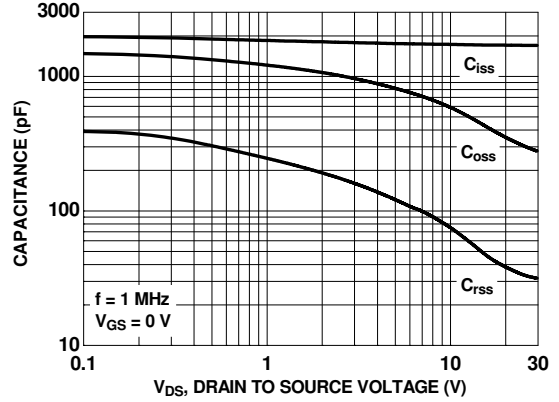


**Figure 19. Source to Drain Diode Forward Voltage vs Source Current**

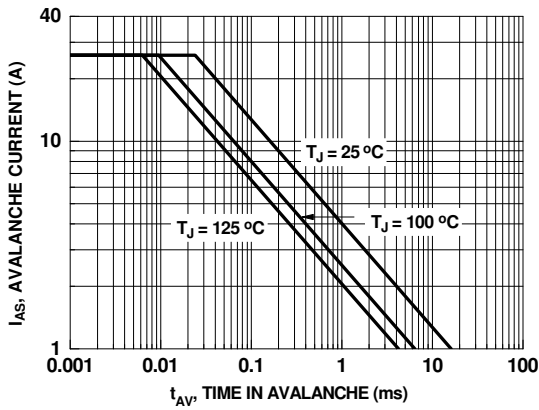
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



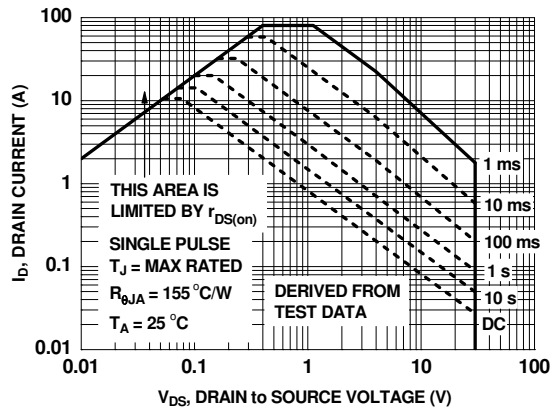
**Figure 20. Gate Charge Characteristics**



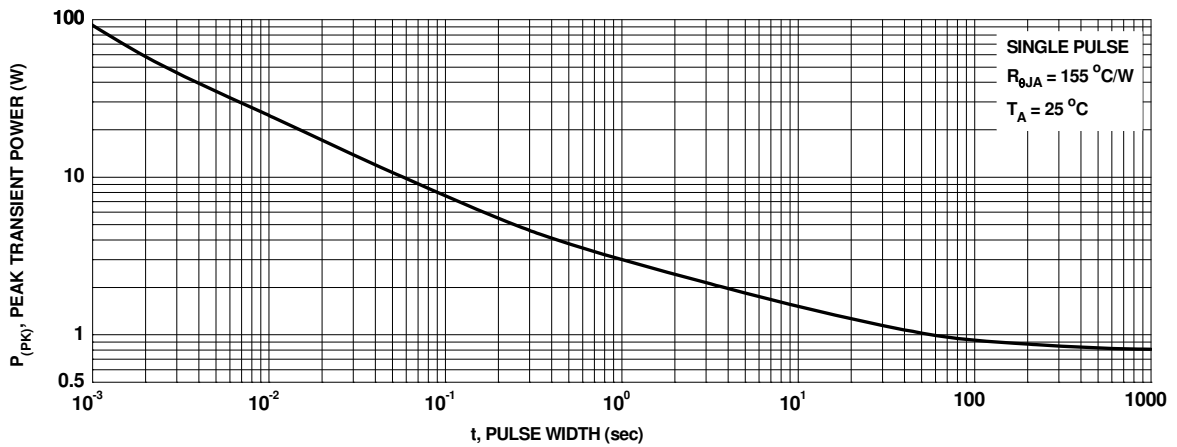
**Figure 21. Capacitance vs Drain to Source Voltage**



**Figure 22. Unclamped Inductive Switching Capability**

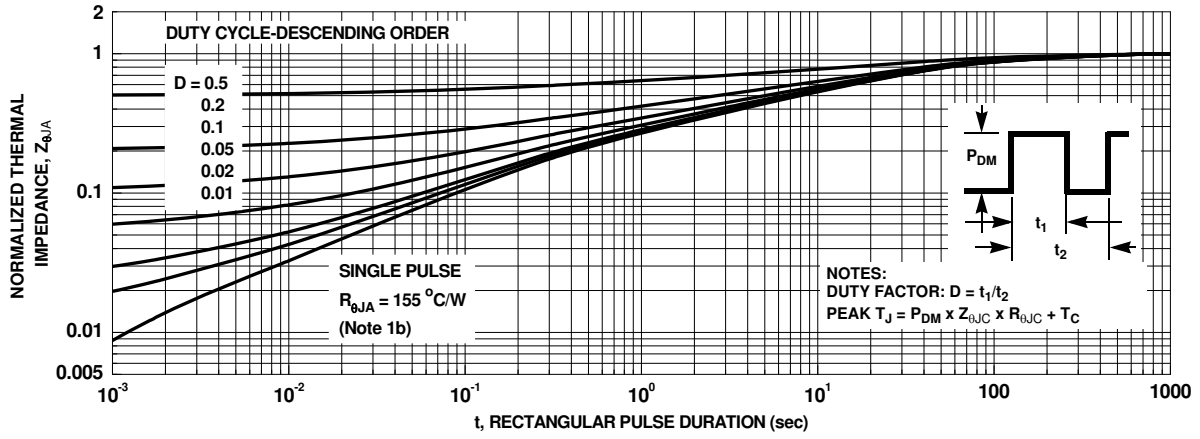


**Figure 23. Forward Bias Safe Operating Area**



**Figure 24. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



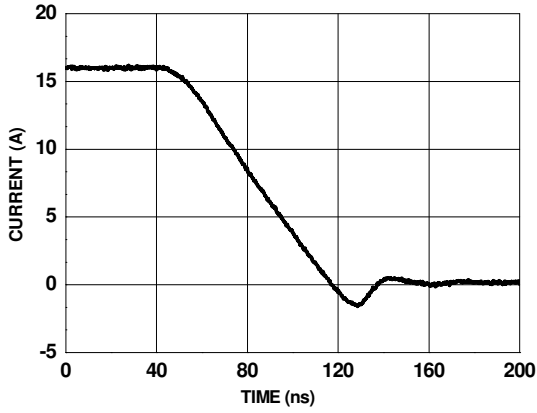
**Figure 26. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (continued)

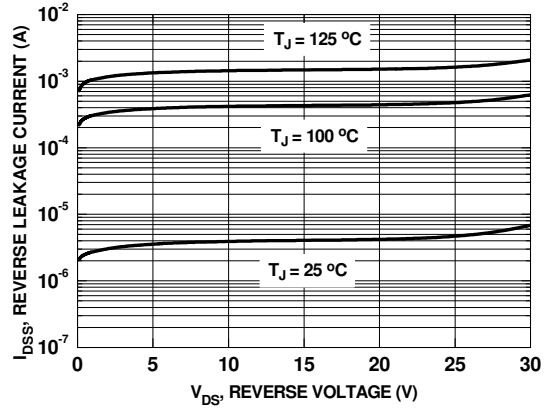
### SyncFET<sup>™</sup> Schottky body diode Characteristics

Fairchild's SyncFET<sup>™</sup> process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMC7208S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

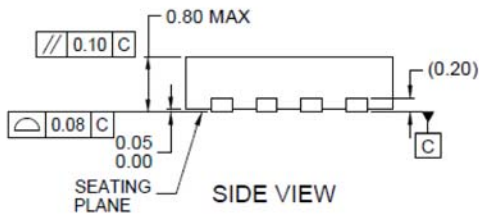
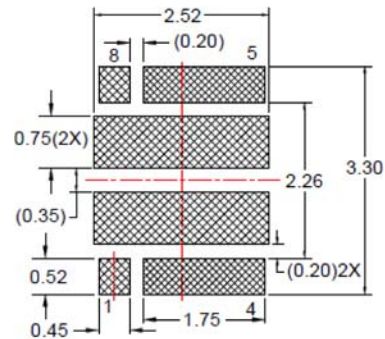
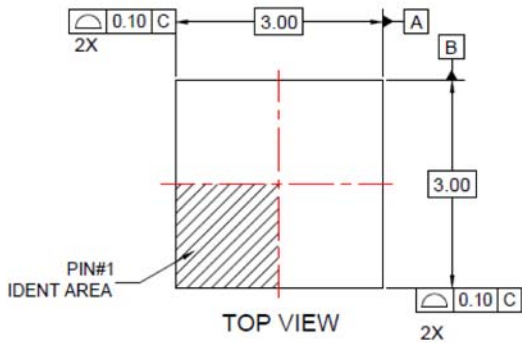


**Figure 27. FDMC7208S SyncFET<sup>™</sup> body diode reverse recovery characteristic**



**Figure 28. SyncFET<sup>™</sup> body diode reverse leakage versus drain-source voltage**

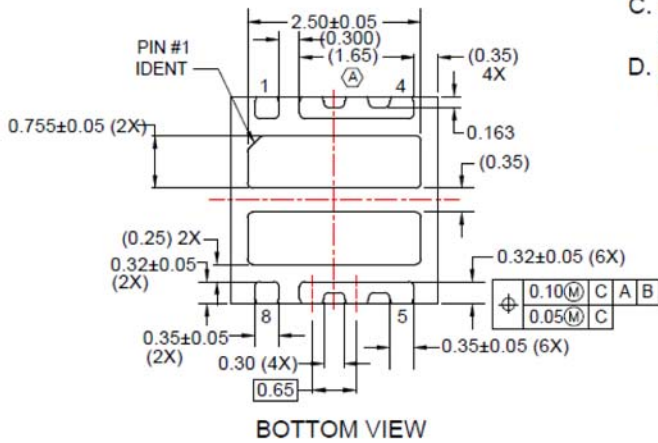
### Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

**NOTES:**


- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY





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| AccuPower™   | F-PFST™   | PowerXS™                              | SYSTEM GENERAL™* |
| AX-CAP®*   | FRFET®  | Programmable Active Droop™            | TinyBoost™       |
| BitSiC™  | Global Power Resource™                          | QFET®                                 | TinyBuck™        |
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