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# FDMC8321L

## N-Channel Power Trench® MOSFET

40 V, 49 A, 2.5 mΩ

### Features

- Max  $r_{DS(on)}$  = 2.5 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 22\text{ A}$
- Max  $r_{DS(on)}$  = 4.1 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 18\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next Generation enhanced body diode technology, engineered for soft recovery
- 100% UIL tested
- RoHS Compliant

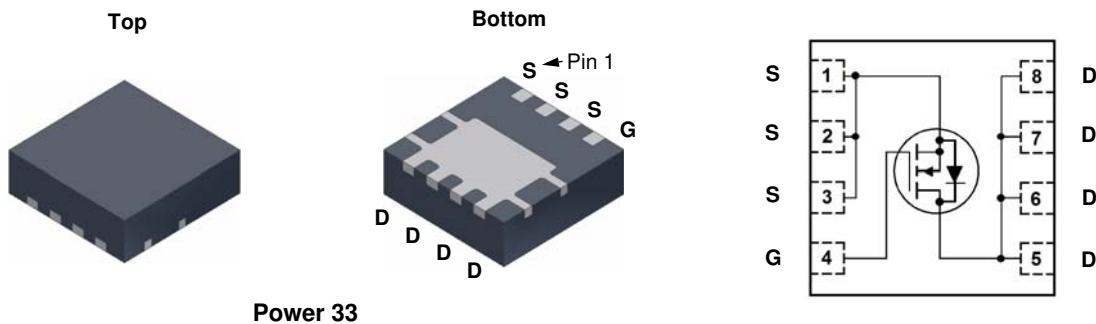


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed body diode reverse recovery performance.

### Applications

- Synchronous rectifier
- Load switch/Orring
- Motor switch



Power 33

### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Conditions	Rated Value	Units
$V_{DS}$	Drain to Source Voltage		40	V
$V_{GS}$	Gate to Source Voltage		±20	V
$I_D$	Drain Current	-Continuous $T_C = 25\text{ °C}$	49	A
		-Continuous $T_A = 25\text{ °C}$ (Note 1a)	22	
		-Pulsed	100	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	86	mJ
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	40	W
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8321L	FDMC8321L	Power33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		22		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 22\text{ A}$		1.9	2.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 18\text{ A}$		2.7	4.1	
		$V_{GS} = 10\text{ V}$ , $I_D = 22\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		2.8	3.7	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 22\text{ A}$		114		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		2930	3900	pF
$C_{oss}$	Output Capacitance			1000	1330	pF
$C_{rss}$	Reverse Transfer Capacitance			60	90	pF
$R_g$	Gate Resistance		0.1	0.7	2.5	$\Omega$

### Switching Characteristics

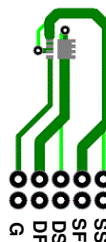
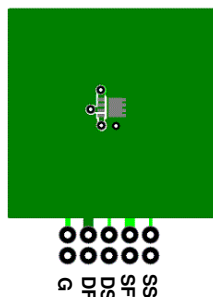
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$ , $I_D = 22\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		12	22	ns
$t_r$	Rise Time			6.1	12	ns
$t_{d(off)}$	Turn-Off Delay Time			32	51	ns
$t_f$	Fall Time			4.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{DD} = 20\text{ V}$ , $I_D = 22\text{ A}$		44	61	nC
$Q_{g(TOT)}$	Total Gate Charge at 5 V			21	32	nC
$Q_{gs}$	Total Gate Charge			7.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.8		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.69	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 22\text{ A}$ (Note 2)		0.77	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 22\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		41	65	ns
$Q_{rr}$	Reverse Recovery Charge			20	33	nC

#### Notes:

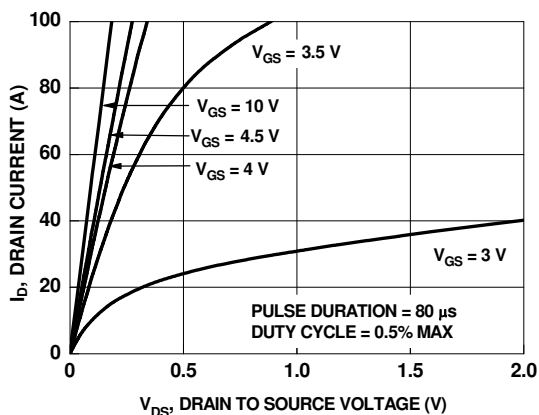
1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



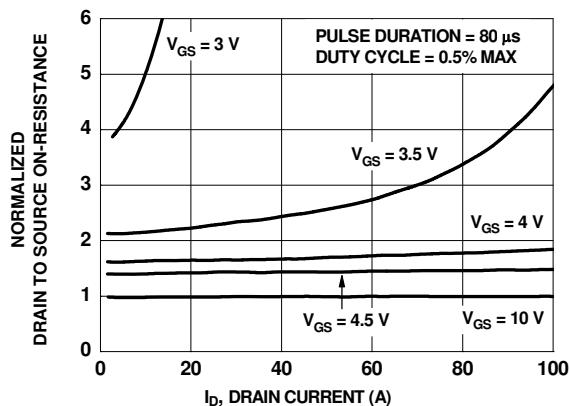
2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 0.3\text{ mH}$ ,  $I_{AS} = 24\text{ A}$ ,  $V_{DD} = 36\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

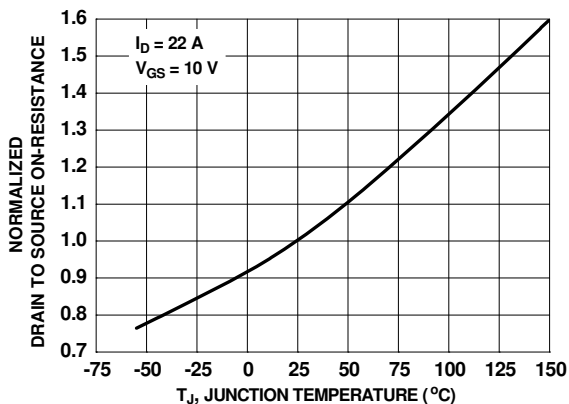
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



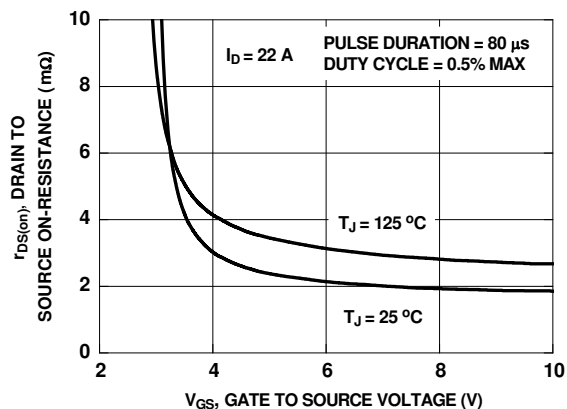
**Figure 1. On Region Characteristics**



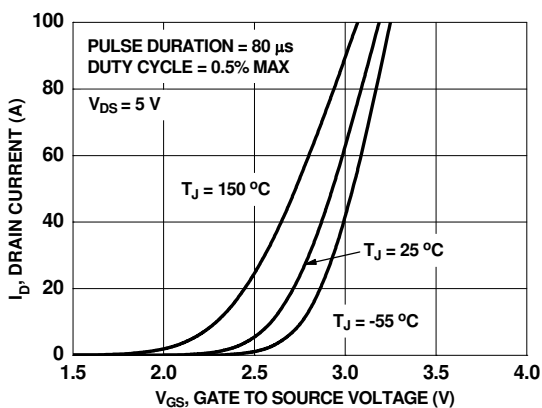
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



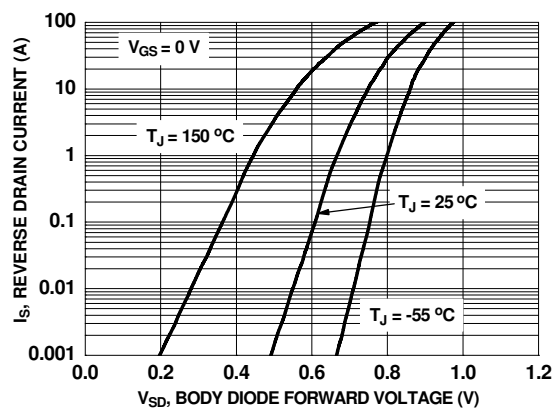
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

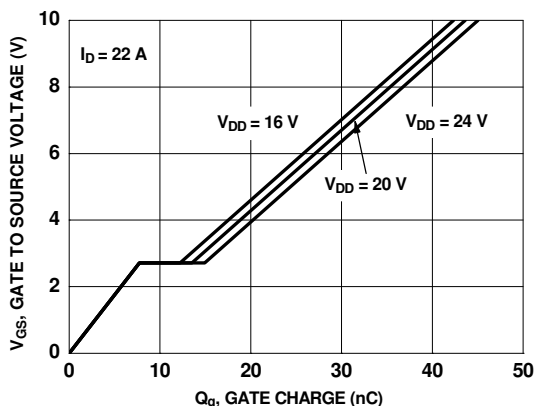


**Figure 5. Transfer Characteristics**

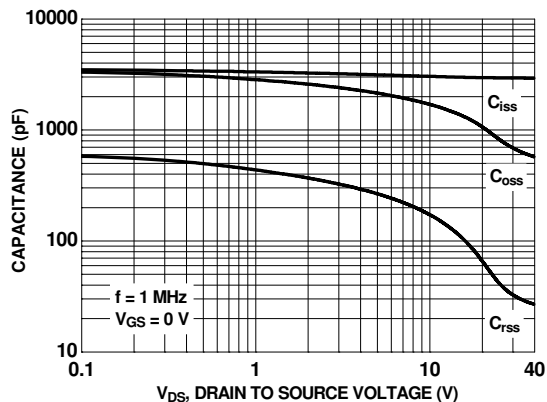


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

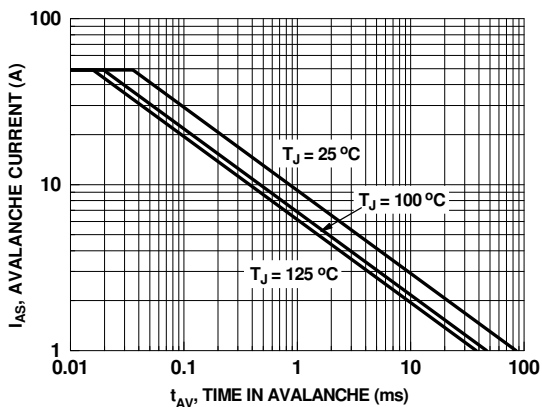
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



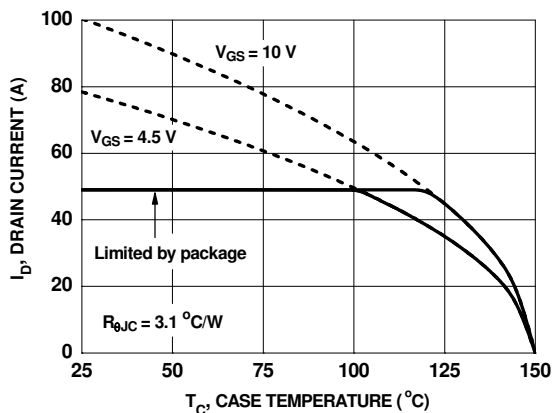
**Figure 7. Gate Charge Characteristics**



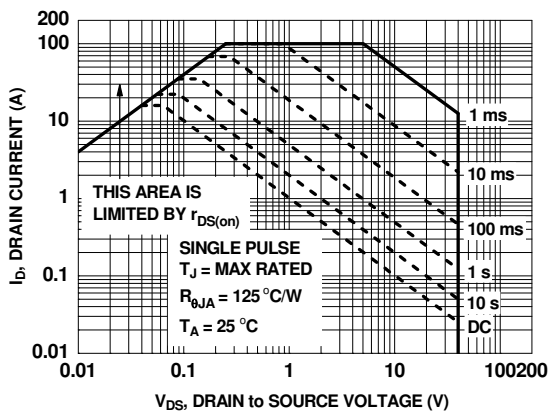
**Figure 8. Capacitance vs Drain to Source Voltage**



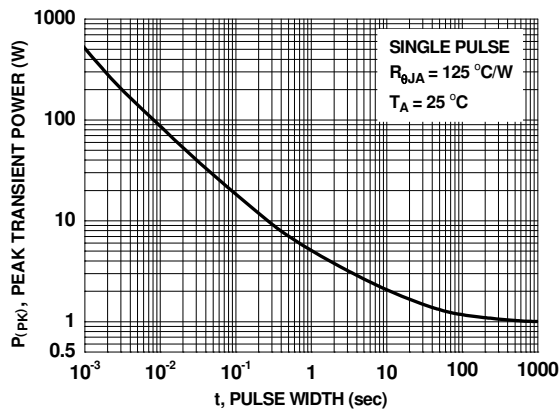
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

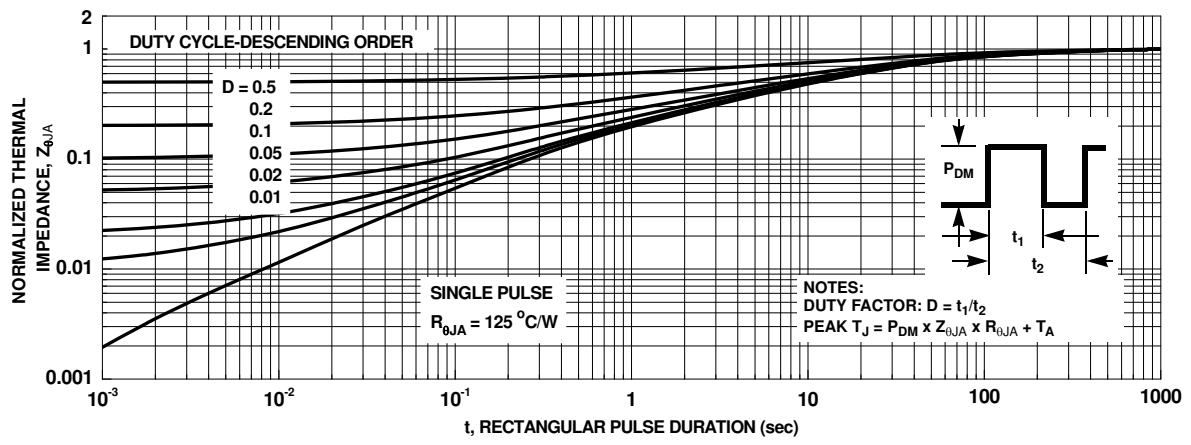


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**





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