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August 2016

# FDMC89521L

# **Dual N-Channel PowerTrench** MOSFET 60 V, 8.2 A, 17 m $\Omega$

#### **Features**

- Max  $r_{DS(on)} = 17 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.2 \text{ A}$
- Max  $r_{DS(on)} = 27 \text{ m}\Omega$  at  $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 6.7 \text{ A}$
- Termination is Lead-free
- RoHS Compliant

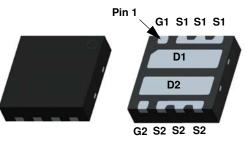
## **General Description**

This device includes two 60 V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

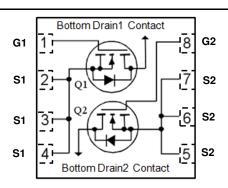
## **Applications**

- Battery Protection
- Load Switching
- Bridge Topologies





Power 33



# **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted.

Symbol	Para	ameter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			60	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	8.2	۸
'D	-Pulsed			40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	32	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25 °C		16	w
	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	1.9	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temp	perature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case		8.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	155	

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC89521L	FDMC89521L	Power 33	13 "	12 mm	3000 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units			
Off Characteristics									
$BV_DSS$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60			V			
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C		30		mV/°C			
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	μΑ			
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA			

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-6		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 8.2 \text{ A}$		13	17	mΩ
		$V_{GS} = 4.5 \text{ V}, I_D = 6.7 \text{ A}$		21	27	
		$V_{GS} = 10 \text{ V}, I_D = 8.2 \text{ A},$ $T_J = 125 \text{ °C}$		20	26	
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 8.2 \text{ A}$		28		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 00 V V 0 V	1228	1635	pF
Coss	Output Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz	243	325	рF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1 1011 12	10	15	рF
R <sub>q</sub>	Gate Resistance		0.7		Ω

#### **Switching Characteristics**

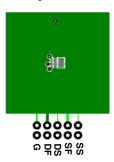
t <sub>d(on)</sub>	Turn-On Delay Time		7.9	16	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 30 \text{ V, } I_D = 8.2 \text{ A,}$	2.1	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	18	33	ns
t <sub>f</sub>	Fall Time		1.7	10	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	17	24	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V} V_{DD} = 30 \text{ V},$	7.9	12	nC
Q <sub>gs</sub>	Gate to Source Charge	I <sub>D</sub> = 8.2 A	3.8		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		1.9		nC

#### **Drain-Source Diode Characteristics**

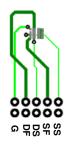
V <sub>SD</sub>	Source-Drain Dioge Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 8.2 A (Note 2)	0.85	1.3	V
		$V_{GS} = 0 \text{ V}, I_S = 1.6 \text{ A}$ (Note 2)	0.75	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 8.2 A, di/dt = 100 A/μs	25	40	ns
$Q_{rr}$	Reverse Recovery Charge	IF = 0.2 A, α//αι = 100 A/μs	11	20	nC

#### Notes:

<sup>1.</sup> R<sub>0,IA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0,IC</sub> is guaranteed by design while R<sub>0,CA</sub> is determined by the user's board design.



 a. 65 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 155 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0%.
- 3. EAS of 32 mJ is based on starting  $T_J = 25$  °C, L = 1 mH,  $I_{AS} = 8$  A,  $V_{DD} = 54$  V,  $V_{GS} = 10$  V. 100% tested at L = 3 mH,  $I_{AS} = 5.4$  A.

# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted.

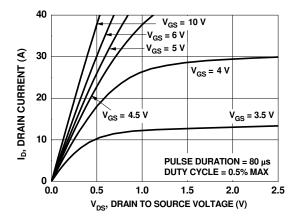


Figure 1. On Region Characteristics

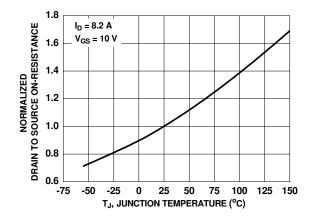


Figure 3. Normalized On Resistance vs. Junction Temperature

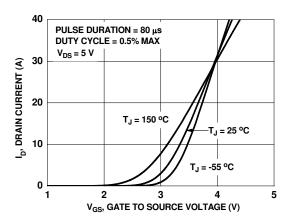


Figure 5. Transfer Characteristics

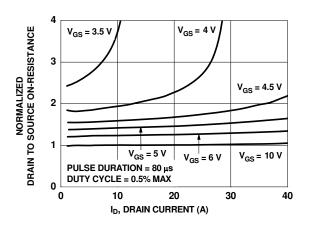


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

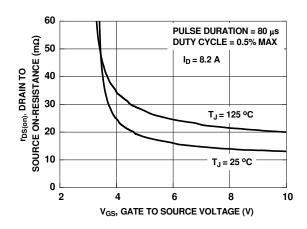


Figure 4. On-Resistance vs. Gate to Source Voltage

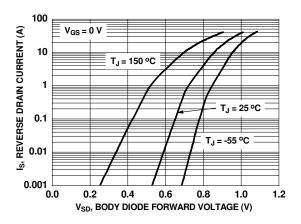


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

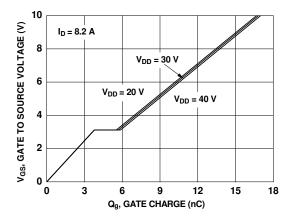


Figure 7. Gate Charge Characteristics

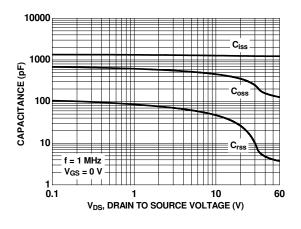


Figure 8. Capacitance vs. Drain to Source Voltage

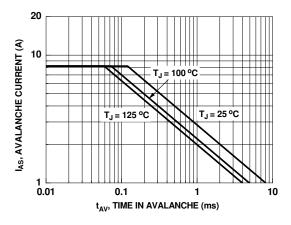


Figure 9. Unclamped Inductive Switching Capability

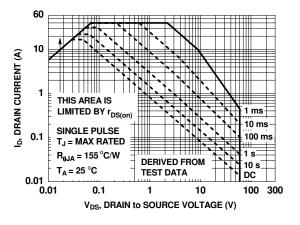


Figure 10. Forward Bias Safe Operating Area

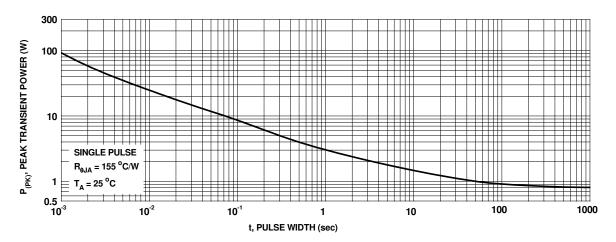


Figure 11. Single Pulse Maximum Power Dissipation

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted.

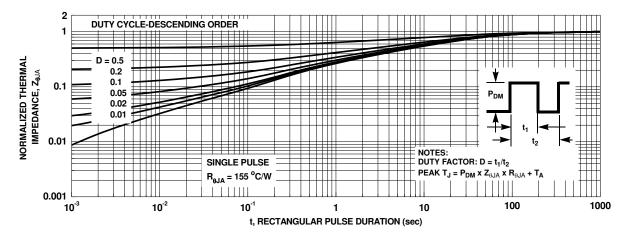
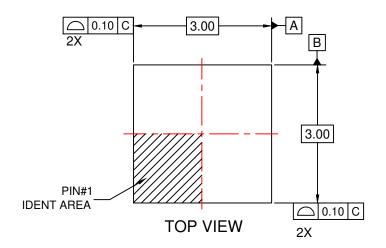
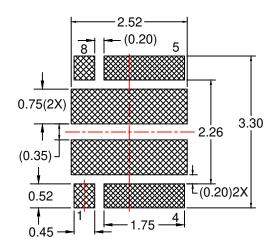
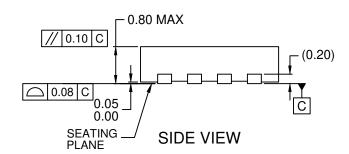


Figure 12. Junction-to-Ambient Transient Thermal Response Curve







#### 2.50±0.05 -0.30 (2X) **PIN #1** (0.35) 4X (1.65)**IDENT** $\langle A \rangle$ 0.755±0.05 (2X)-<sup>L</sup>0.163 (0.35)(0.25) 2X·0.32±0.05 (6X) 0.32±0.05 (2X) 0.10M C A B 0.05M C 5 0.35±0.05 0.35±0.05 (6X) (2X) 0.30 (4X) 0.65 **BOTTOM VIEW**

#### RECOMMENDED LAND PATTERN

#### NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
  - D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
  - E. DRAWING FILE NAME: MKT-MLP08Xrev2.

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