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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

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June 2014

FDMD82100L

Dual N-Channel PowerTrench[®] MOSFET

100 V, 24 A, 19.5 mΩ

Features

- Max $r_{DS(on)}$ = 19.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$
- Max $r_{DS(on)}$ = 30 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 5.7\text{ A}$
- Ideal for flexible layout in primary side of bridge topology
- Termination is Lead-free and RoHS Compliant
- 100% UIL tested
- Kelvin High Side MOSFET drive pin-out capability

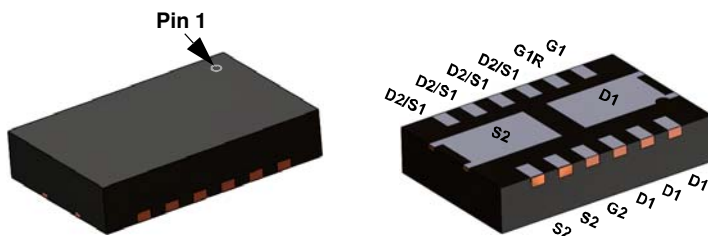


General Description

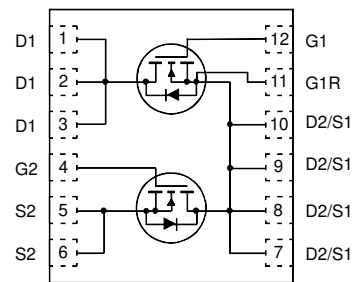
This device includes two 100V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$ /Qg FOM silicon.

Applications

- Synchronous Buck : Primary Switch of Half / Full bridge converter for telecom
- Motor Bridge : Primary Switch of Half / Full bridge converter for BLDC motor
- MV POL : 48V Synchronous Buck Switch



Power 3.3 x 5



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous	$T_C = 25\text{ °C}$	24
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	7
	-Pulsed	$T_A = 25\text{ °C}$ (Note 4)	80
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	150
P_D	Power Dissipation	$T_C = 25\text{ °C}$	38
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.1
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1b)	1
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.3	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)		60
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)		130

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
82100L	FDMD82100L	Power 3.3 x 5	13 "	12 mm	3000 units

FDMD82100L Dual N-Channel PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		70		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 7\ \text{A}$		13.5	19.5	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 5.7\ \text{A}$		17.9	30	
		$V_{GS} = 10\ \text{V}, I_D = 7\ \text{A}, T_J = 125^\circ\text{C}$		25	36	
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 7\ \text{A}$		29		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$		1130	1585	pF
C_{oss}	Output Capacitance			173	245	pF
C_{riss}	Reverse Transfer Capacitance			8.1	15	pF
R_g	Gate Resistance		0.1	1.8	3.6	Ω

Switching Characteristics

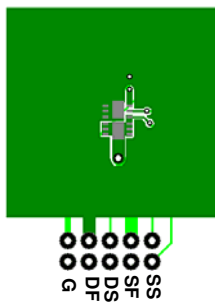
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 7\ \text{A}$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		7.9	16	ns
t_r	Rise Time			2.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			21	34	ns
t_f	Fall Time			2.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 10\ \text{V}$		17	24
	Total Gate Charge	$V_{GS} = 0\ \text{V to } 4.5\ \text{V}$	$V_{DD} = 50\ \text{V}$ $I_D = 7\ \text{A}$	8	12	nC
Q_{gs}	Gate to Source Charge			3		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.3		nC

Drain-Source Diode Characteristics

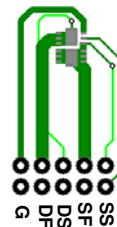
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 7\ \text{A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 7\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		42	67	ns
Q_{rr}	Reverse Recovery Charge			39	62	nC

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 130 °C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.
- E_{AS} of 150 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\ \text{mH}$, $I_{AS} = 10\ \text{A}$, $V_{DD} = 90\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% tested at $L = 0.1\ \text{mH}$, $I_{AS} = 31\ \text{A}$.
- Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics (N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

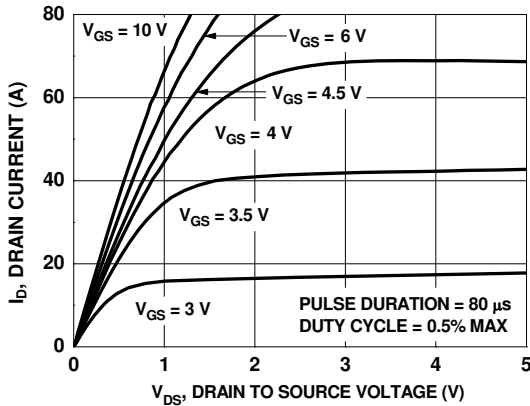


Figure 1. On Region Characteristics

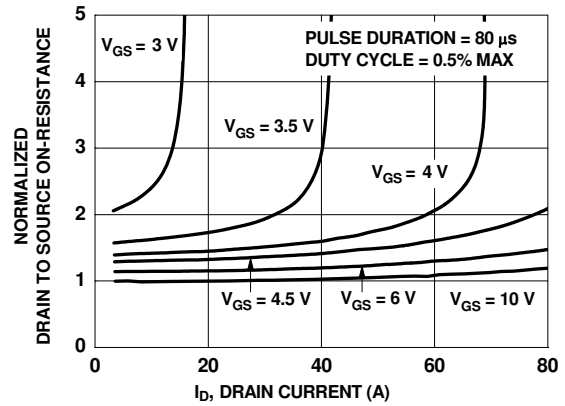


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

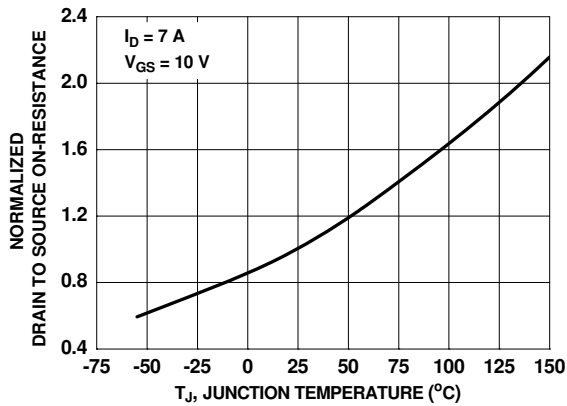


Figure 3. Normalized On Resistance vs Junction Temperature

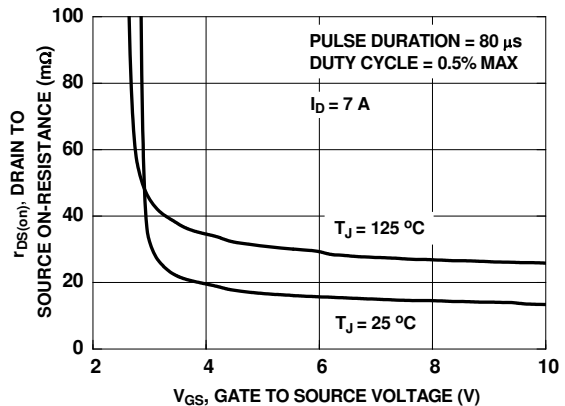


Figure 4. On-Resistance vs Gate to Source Voltage

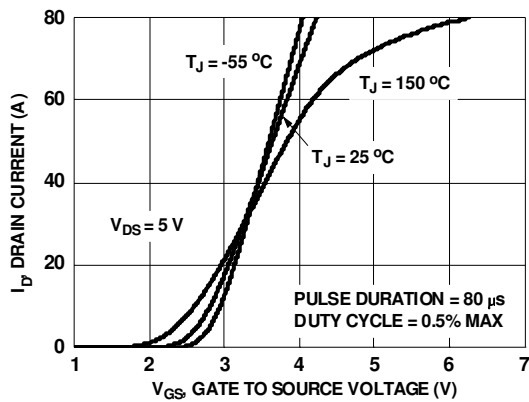


Figure 5. Transfer Characteristics

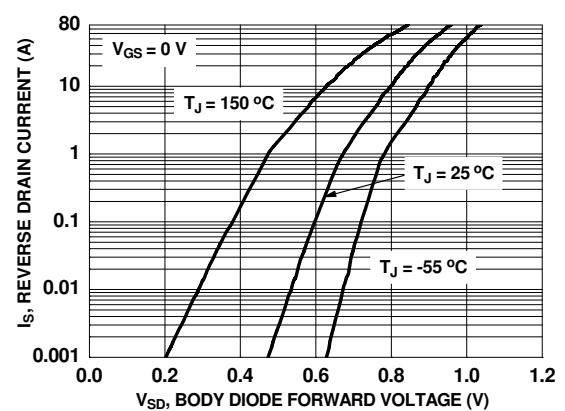


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

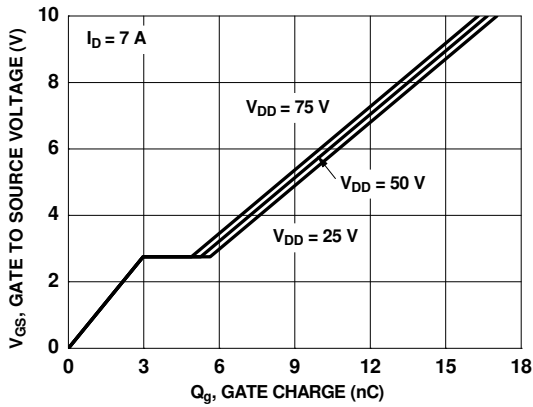


Figure 7. Gate Charge Characteristics

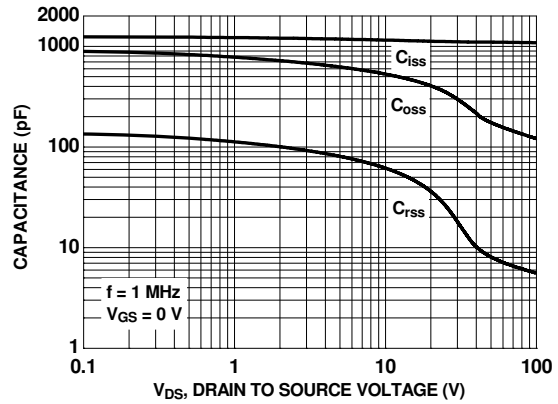


Figure 8. Capacitance vs Drain to Source Voltage

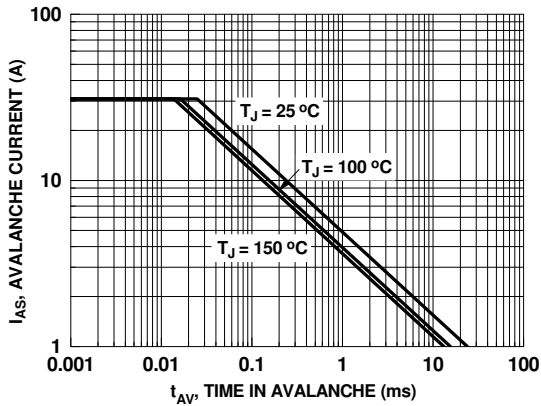


Figure 9. Unclamped Inductive Switching Capability

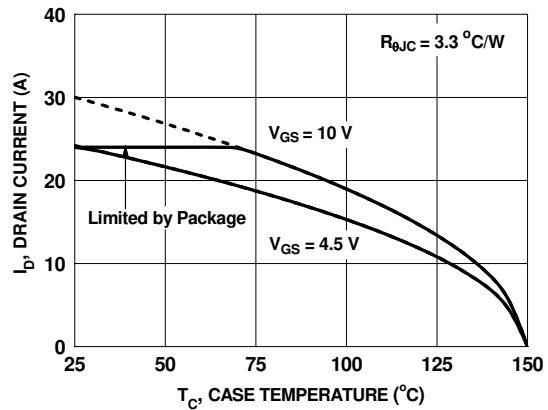


Figure 10. Maximum Continuous Drain Current vs Case Temperature

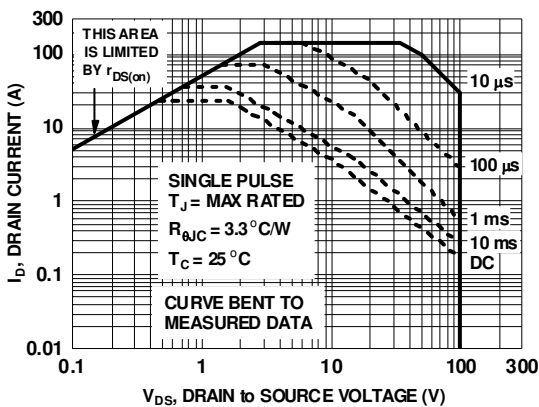


Figure 11. Forward Bias Safe Operating Area

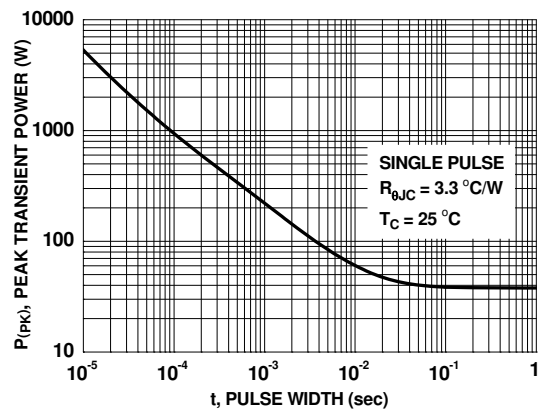


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

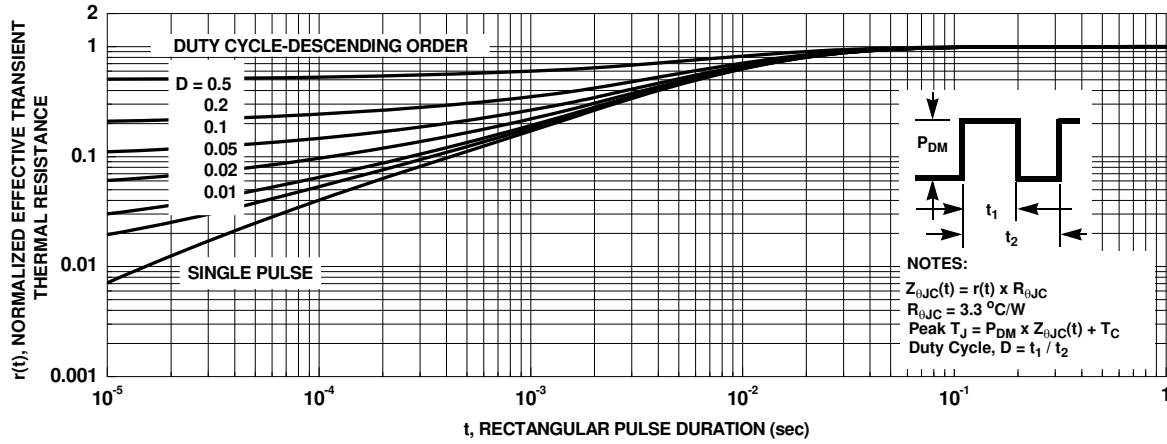
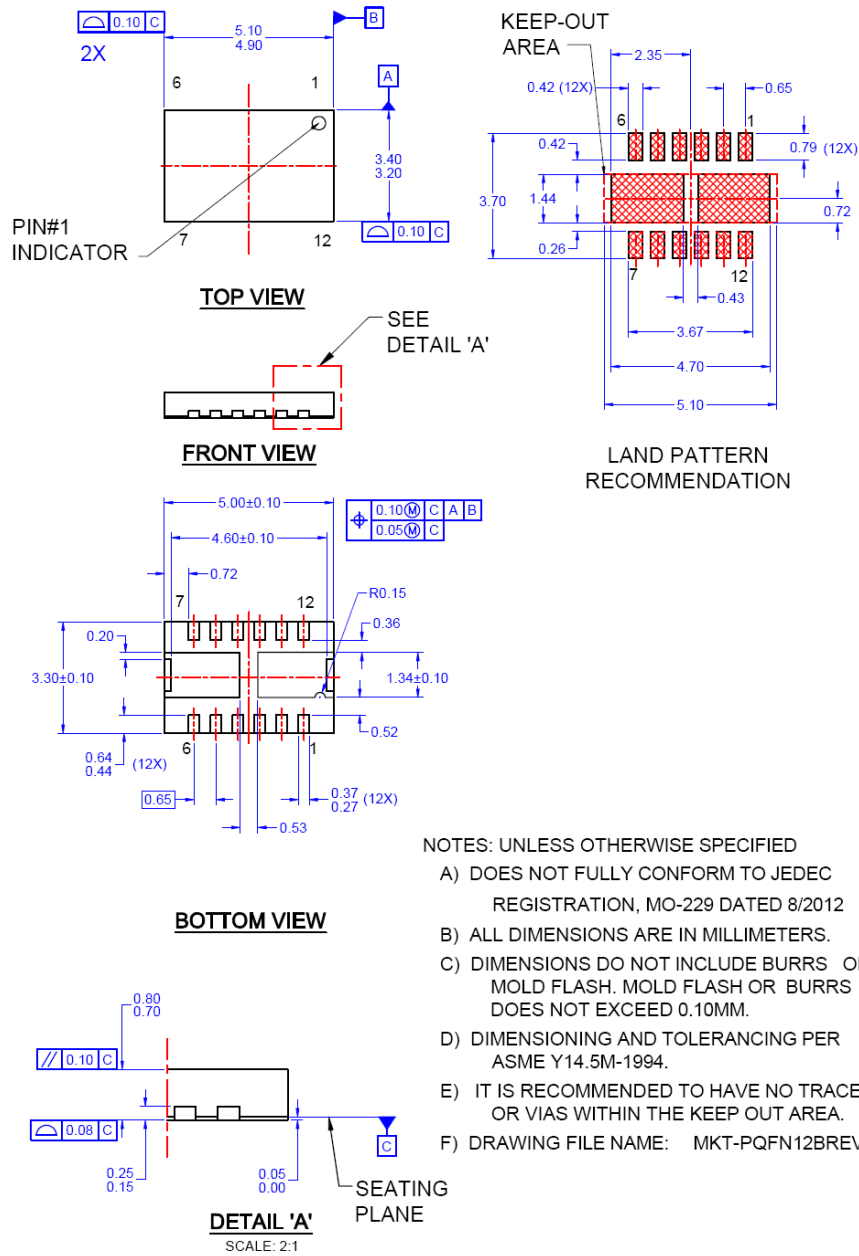


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout




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