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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





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# FDMD8580

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

Q1: 80 V, 82 A, 4.6 mΩ Q2: 80 V, 82 A, 4.6 mΩ

### Features

- Q1: N-Channel
  - Max  $r_{DS(on)}$  = 4.6 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 16\text{ A}$
  - Max  $r_{DS(on)}$  = 6.0 mΩ at  $V_{GS} = 8\text{ V}$ ,  $I_D = 14\text{ A}$
- Q2: N-Channel
  - Max  $r_{DS(on)}$  = 4.6 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 16\text{ A}$
  - Max  $r_{DS(on)}$  = 6.0 mΩ at  $V_{GS} = 8\text{ V}$ ,  $I_D = 14\text{ A}$
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- RoHS Compliant

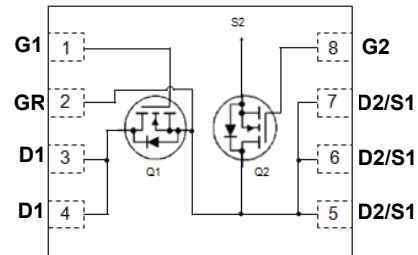
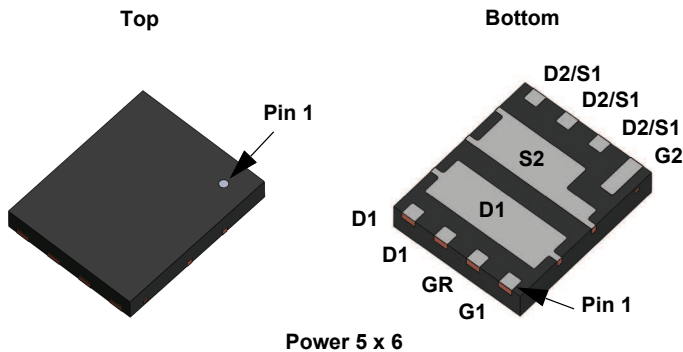


### General Description

This device includes two 80V N-Channel MOSFETs in a dual power (5 mm X 6 mm) package. HS source and LS drain internally connected for half/full bridge, low source inductance package, low  $r_{DS(on)}$ /Qg FOM silicon.

### Applications

- Synchronous Buck: Primary Switch of Half / Full Bridge Converter for Telecom
- Motor Bridge: Primary Switch of Half / Full Bridge Converter for BLDC Motor
- MV POL: 48V Synchronous Buck Switch
- Half/Full Bridge Secondary Synchronous Rectification



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	80	80	V
$V_{GS}$	Gate to Source Voltage	±20	±20	V
$I_D$	Drain Current -Continuous $T_C = 25\text{ °C}$ (Note 5)	82	82	A
	-Continuous $T_C = 100\text{ °C}$ (Note 5)	52	52	
	-Continuous $T_A = 25\text{ °C}$	16 <sup>1a</sup>	16 <sup>1b</sup>	
	-Pulsed (Note 4)	482	482	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	337	337	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	59	59	W
	Power Dissipation $T_A = 25\text{ °C}$	2.3 <sup>1a</sup>	2.3 <sup>1b</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.1	2.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	55 <sup>1a</sup>	55 <sup>1b</sup>	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD8580	FDMD8580	Power 5 x 6	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	80 80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		50 50		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	Q1 Q2	2.0 2.0	3.4 3.4	4.5 4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-10 -10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$	Q1		3.5	4.6	m $\Omega$
		$V_{GS} = 8\text{ V}$ , $I_D = 14\text{ A}$			4.2	6.0	
		$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$			5.3	7.0	
		$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$	Q2		3.5	4.6	
		$V_{GS} = 8\text{ V}$ , $I_D = 14\text{ A}$			4.2	6.0	
		$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$			5.3	7.0	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{ V}$ , $I_D = 16\text{ A}$	Q1 Q2		51 51		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	Q1 Q2		4195 4195	5875 5875	pF
$C_{oss}$	Output Capacitance		Q1 Q2		602 602	845 845	pF
$C_{rss}$	Reverse Transfer Capacitance		Q1 Q2		19 19	38 38	pF
$R_g$	Gate Resistance		Q1 Q2	0.1 0.1	1.7 1.7	3.5 3.5	$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$ , $I_D = 16\text{ A}$ $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		25 25	40 40	ns
$t_r$	Rise Time		Q1 Q2		19 19	34 34	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		31 31	50 50	ns
$t_f$	Fall Time		Q1 Q2		10 10	20 20	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$	Q1 Q2		57 57	80 80
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 40\text{ V}$ , $I_D = 16\text{ A}$	Q1 Q2		21 21		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		12 12		nC



**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

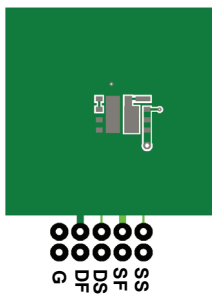
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
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**Drain-Source Diode Characteristics**

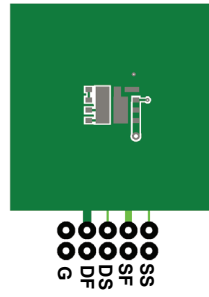
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$ (Note 2)	Q1 Q2		0.8 0.8	1.3 1.3	V
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)	Q1 Q2		0.7 0.7	1.2 1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 16\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		46 46	73 73	ns
$Q_{rr}$	Reverse Recovery Charge		Q1 Q2		34 34	55 55	nC

NOTES:

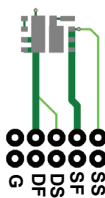
- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



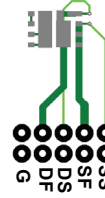
a. 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 155 °C/W when mounted on a minimum pad of 2 oz copper



d. 155 °C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.
- Q1:  $E_{AS}$  of 337 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 15\text{ A}$ ,  $V_{DD} = 80\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{mH}$ ,  $I_{AS} = 49\text{ A}$ .  
Q2:  $E_{AS}$  of 337 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 15\text{ A}$ ,  $V_{DD} = 80\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{mH}$ ,  $I_{AS} = 49\text{ A}$ .
- Pulsed Id please refer to Fig 11 and Fig 24 SOA graph for more details.
- Computed continuous current limited to max junction temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

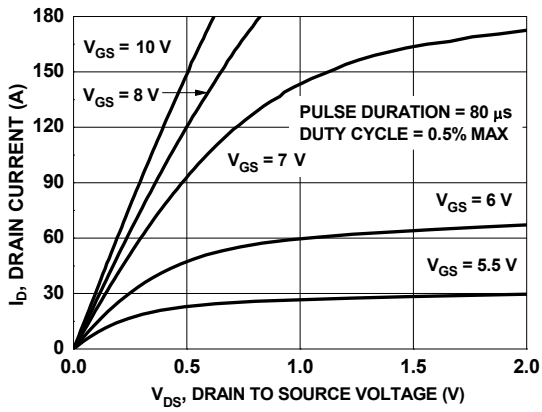


Figure 1. On Region Characteristics

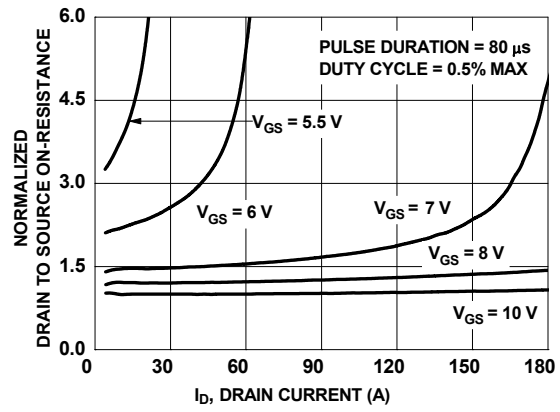


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

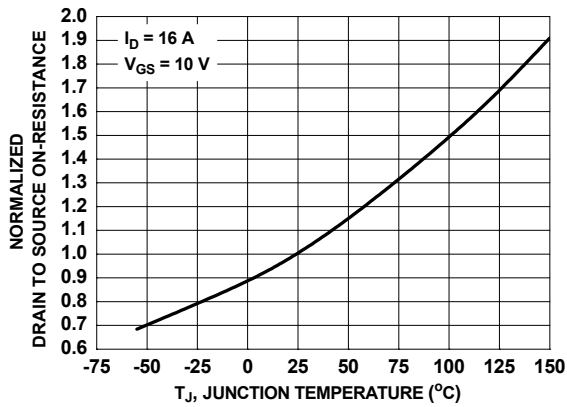


Figure 3. Normalized On Resistance vs. Junction Temperature

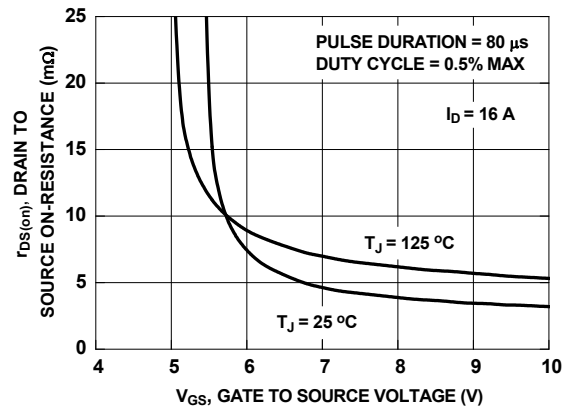


Figure 4. On-Resistance vs. Gate to Source Voltage

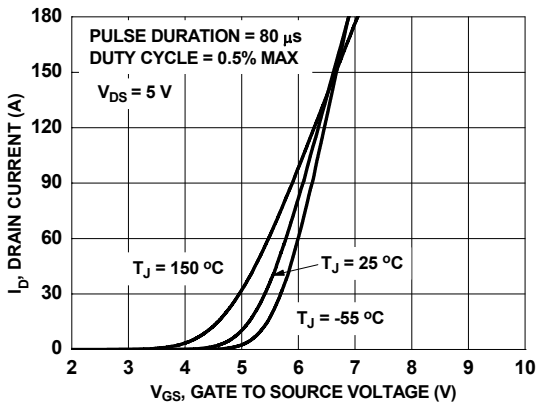


Figure 5. Transfer Characteristics

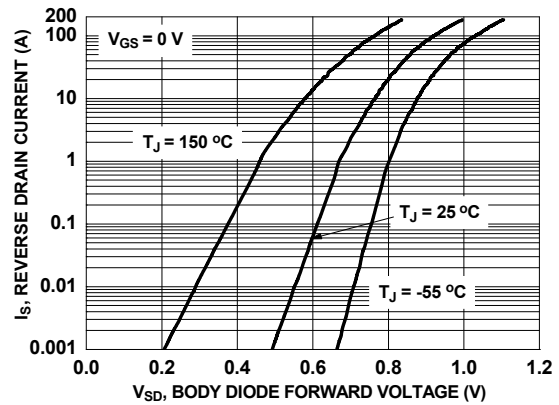
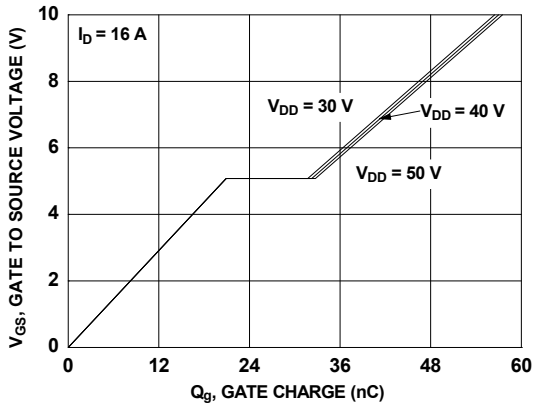
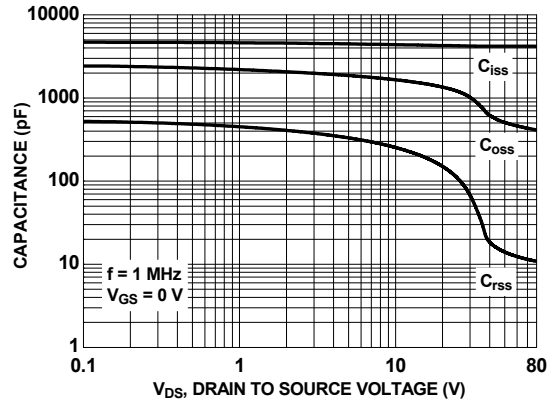


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

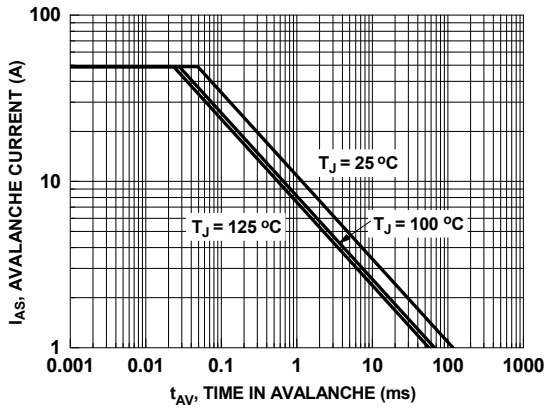
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



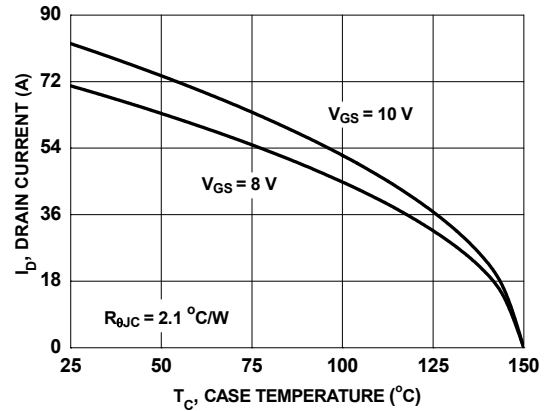
**Figure 7. Gate Charge Characteristics**



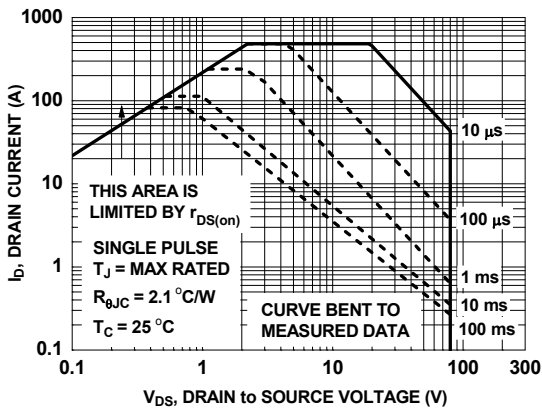
**Figure 8. Capacitance vs. Drain to Source Voltage**



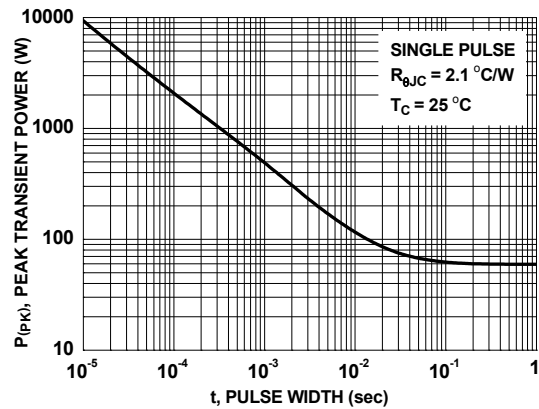
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

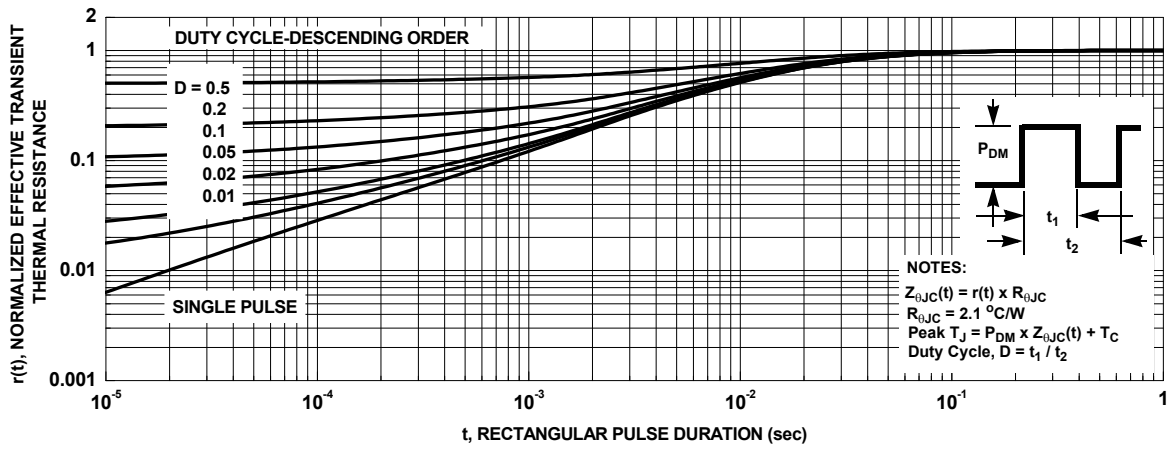


Figure 13. Junction-to-Case Transient Thermal Response Curve



**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

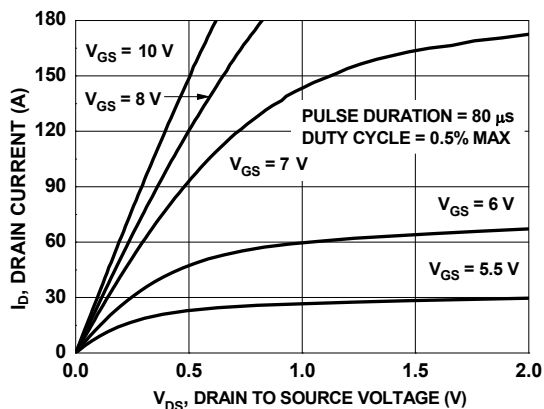


Figure 14. On-Region Characteristics

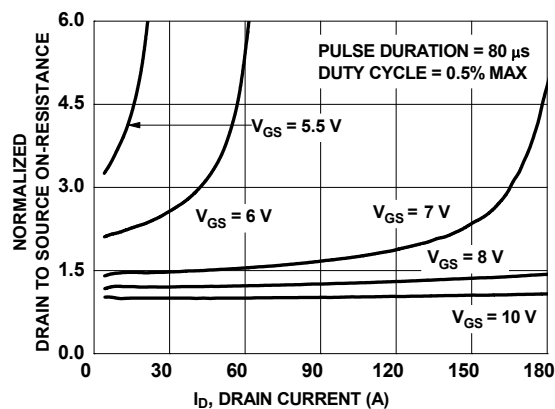


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

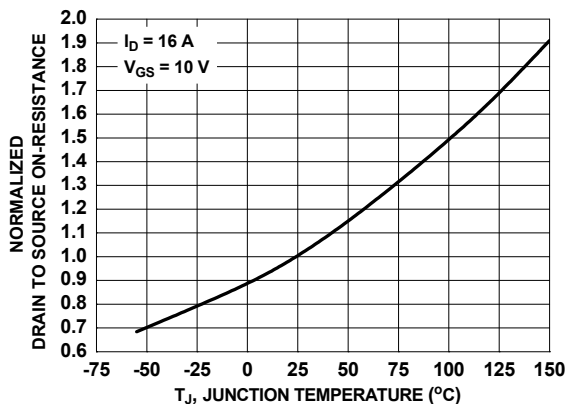


Figure 16. Normalized On-Resistance vs. Junction Temperature

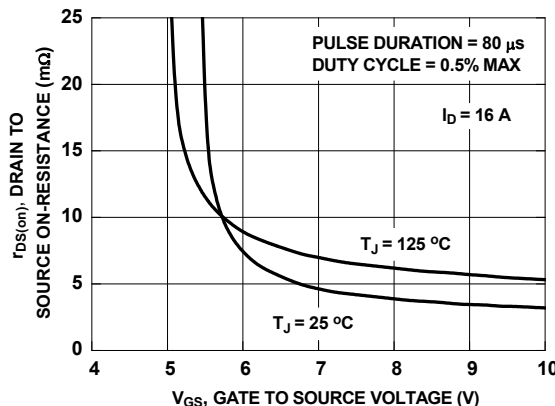


Figure 17. On-Resistance vs. Gate to Source Voltage

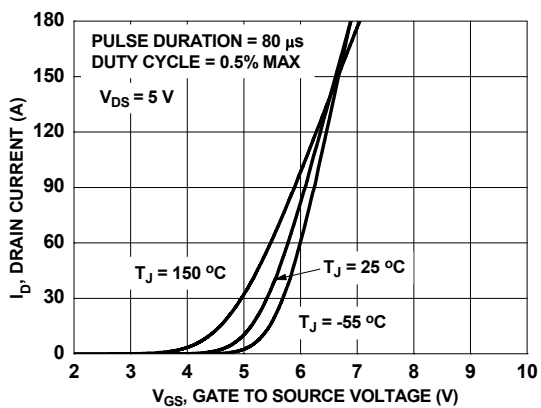


Figure 18. Transfer Characteristics

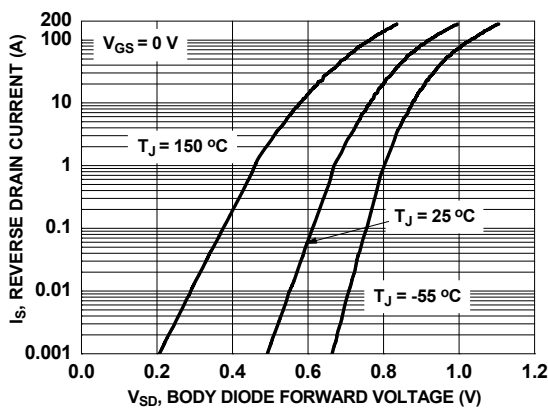
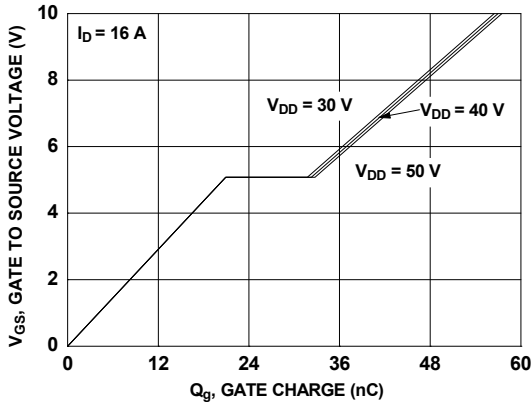
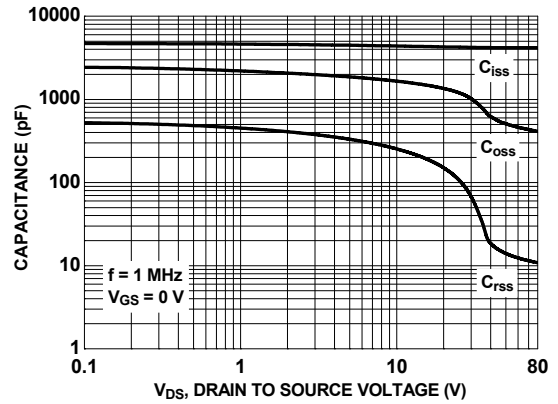


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

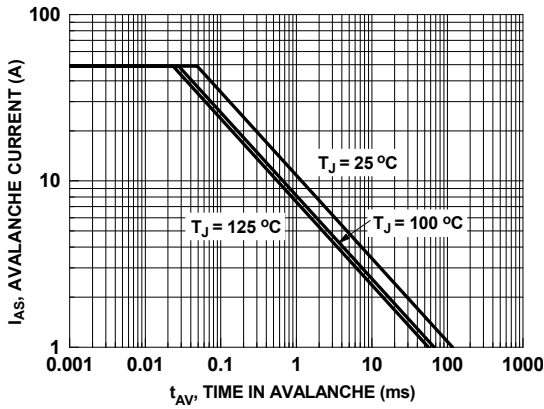
**Typical Characteristics (Q2 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



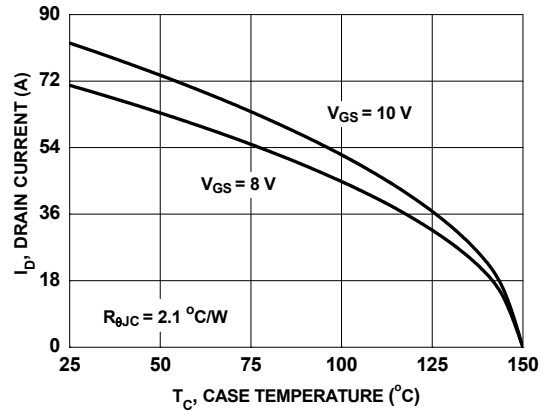
**Figure 20. Gate Charge Characteristics**



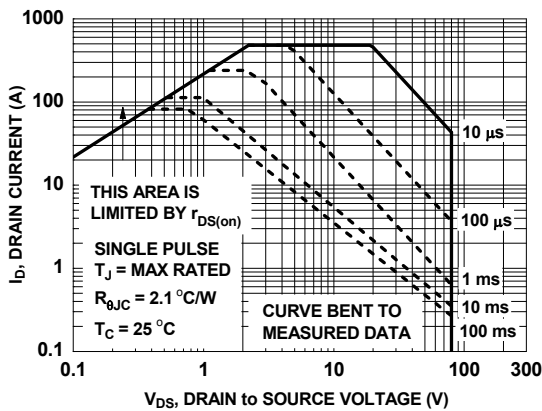
**Figure 21. Capacitance vs. Drain to Source Voltage**



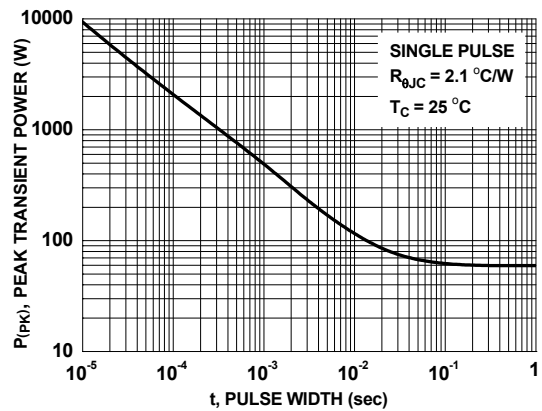
**Figure 22. Unclamped Inductive Switching Capability**



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**

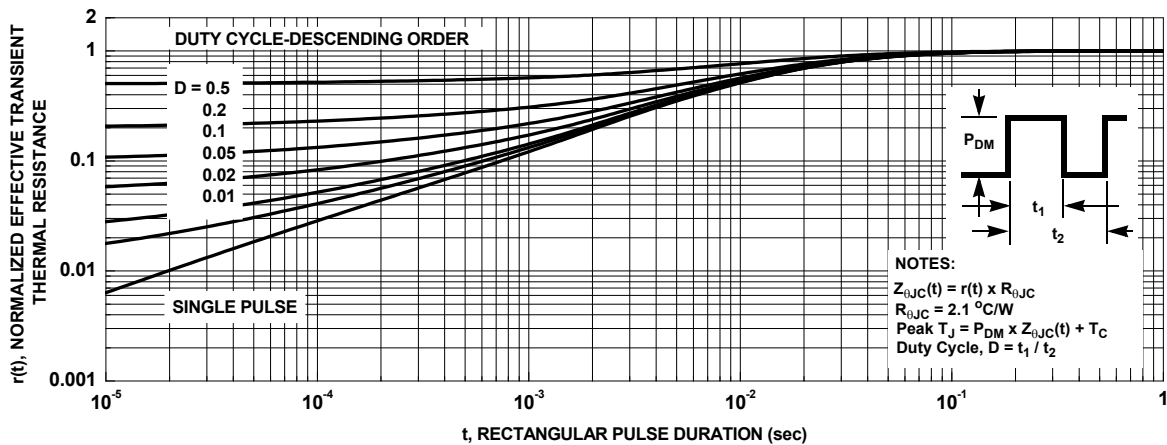


**Figure 24. Forward Bias Safe Operating Area**

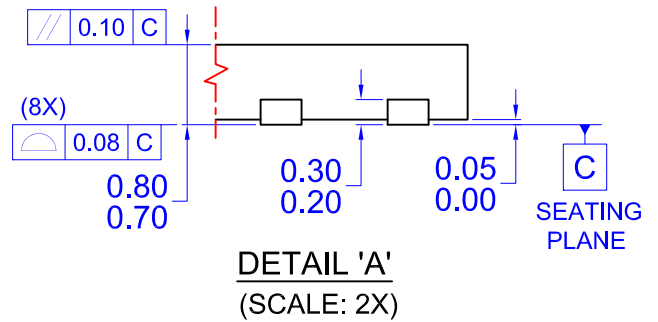
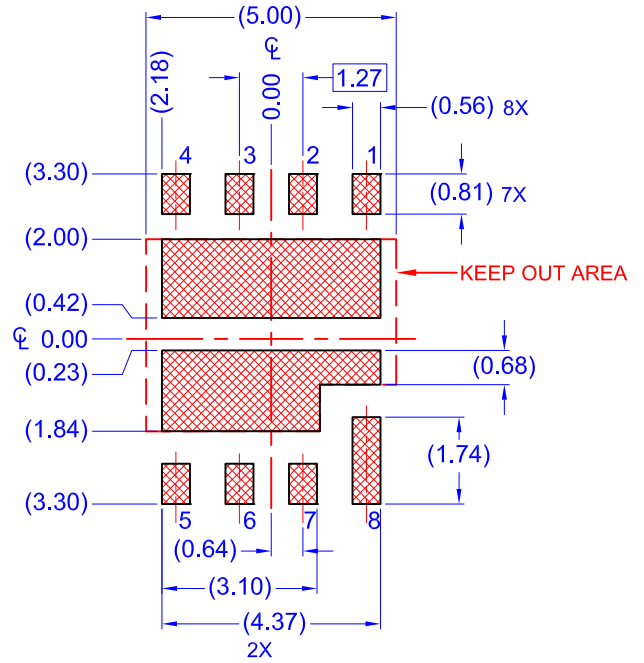
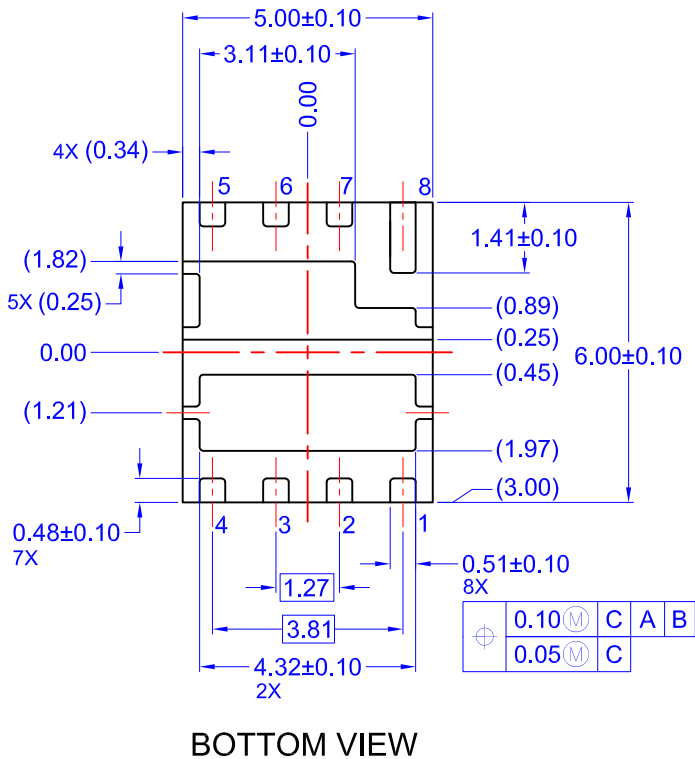
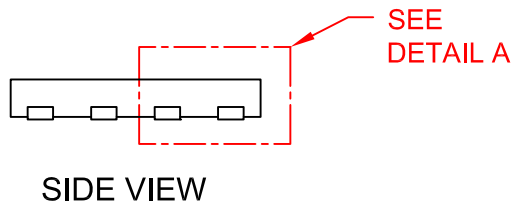
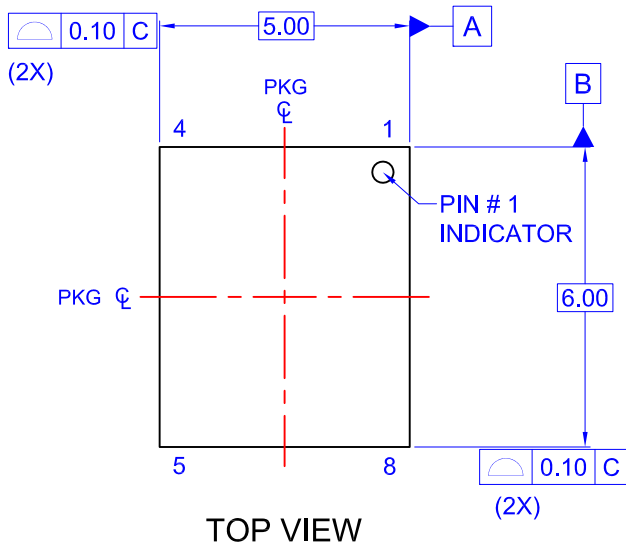


**Figure 25. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q2 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 26. Junction-to-Case Transient Thermal Response Curve**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME: MKT-PQFN08QREV2



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