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FDMS3572
N-Channel UltraFET Trench® MOSFET
80V, 22A, 16.5mΩ

Features

■ Max $r_{DS(on)}$ = 16.5mΩ at V_{GS} = 10V, I_D = 8.8A

■ Max $r_{DS(on)}$ = 24mΩ at V_{GS} = 6V, I_D = 8.4A

■ Typ Qg = 28nC at V_{GS} = 10V

■ Low Miller Charge

■ Optimized efficiency at high frequencies
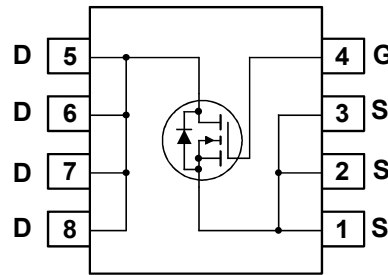
■ RoHS Compliant

General Description

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Application

■ DC - DC Conversion

Pin 1 → S S S G

D D D D
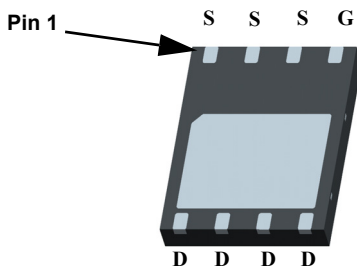
Power 56 (Bottom view)

D **5**   **4** G
D **6**   **3** S
D **7**   **2** S
D **8**   **1** S

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		80	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C		22	A
	-Continuous (Silicon limited) T_C = 25°C		48	
	-Continuous T_A = 25°C (Note 1a)		8.8	
	-Pulsed		50	
P_D	Power Dissipation T_C = 25°C		78	W
	Power Dissipation T_A = 25°C (Note 1a)		2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS3572	FDMS3572	Power 56	13''	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		76		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-11		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 8.8A		13.5	16.5	mΩ
		V_{GS} = 6V, I_D = 8.4A		18.3	24	
		V_{GS} = 10V, I_D = 8.8A, T_J = 125°C		22.2	29	
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 8.8A		23		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		1870	2490	pF
C_{oss}	Output Capacitance			275	365	pF
C_{rss}	Reverse Transfer Capacitance			78	120	pF
R_g	Gate Resistance	f = 1MHz		1.3		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40V, I_D = 8.8A V_{GS} = 10V, R_{GEN} = 6Ω		11	20	ns
t_r	Rise Time			13	24	ns
$t_{d(off)}$	Turn-Off Delay Time			24	39	ns
t_f	Fall Time			12	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V V_{DD} = 40V I_D = 8.8A		28	40	nC
Q_{gs}	Gate to Source Gate Charge			9		nC
Q_{gd}	Gate to Drain "Miller" Charge			8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 8.8A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 8.8A, di/dt = 100A/μs		43	65	ns
Q_{rr}	Reverse Recovery Charge			71	107	nC

Notes:
1: $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
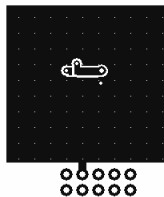
a. 50°C/W when mounted on a 1 in² pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

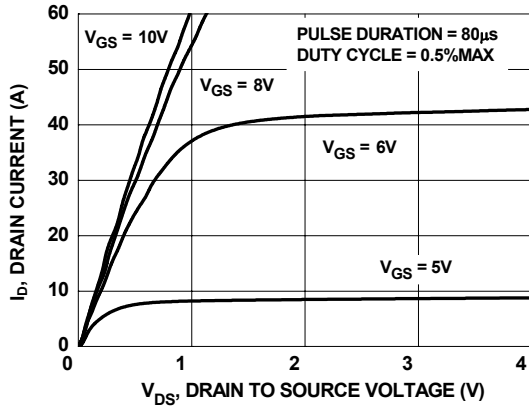## Typical Characteristics T_J = 25°C unless otherwise noted

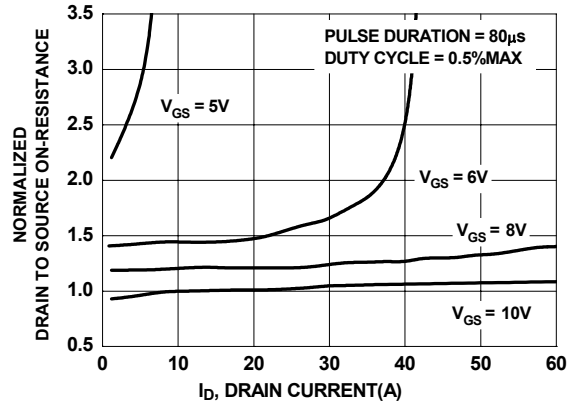**Figure 1. On Region Characteristics**

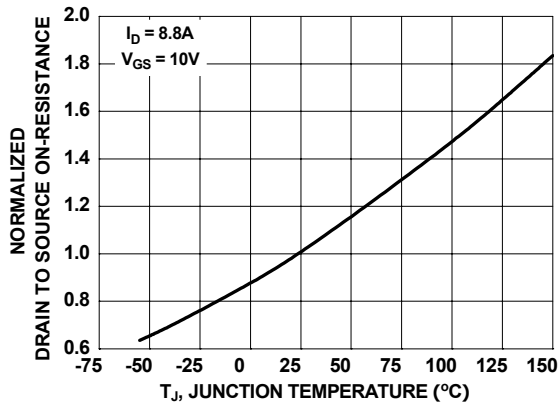**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

Figure 3. Normalized On Resistance vs Junction Temperature
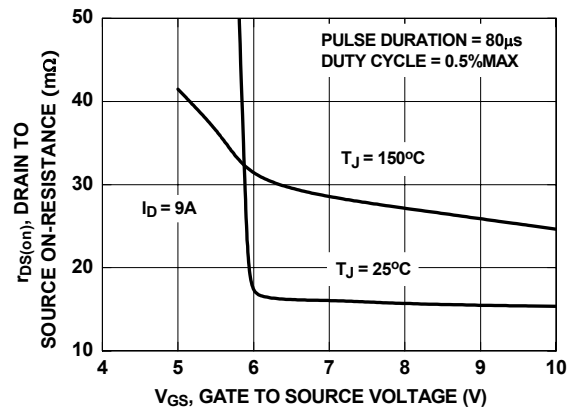

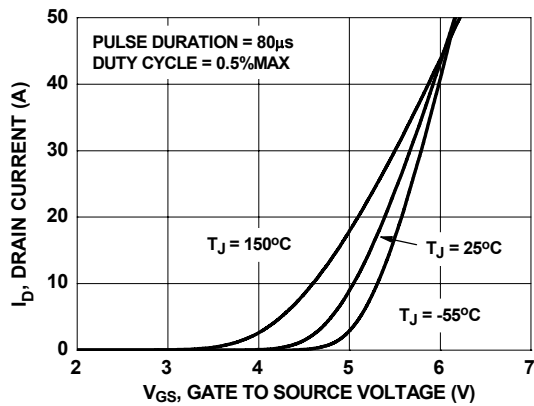**Figure 4. On-Resistance vs Gate to Source Voltage**
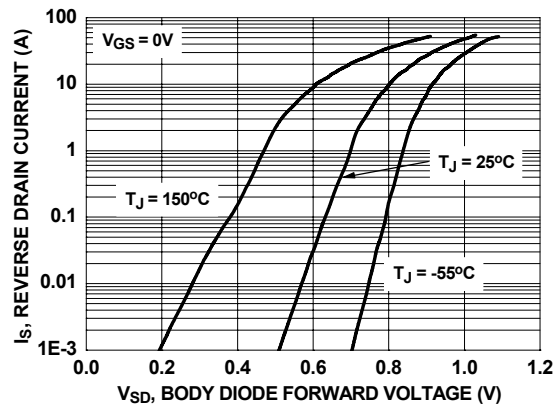

Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted
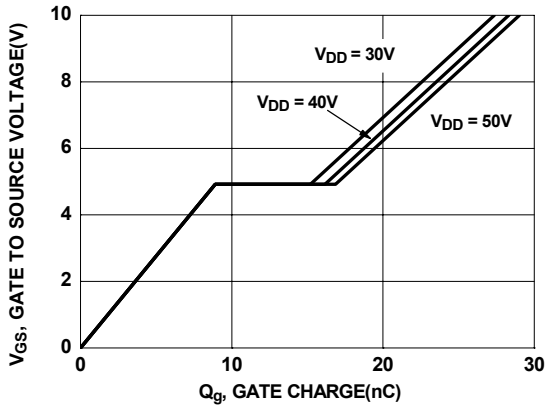
Figure 7. Gate Charge Characteristics

Axis: V_{GS}, GATE TO SOURCE VOLTAGE(V); Q_g, GATE CHARGE(nC); V_{DD} = 30V, V_{DD} = 40V, V_{DD} = 50V
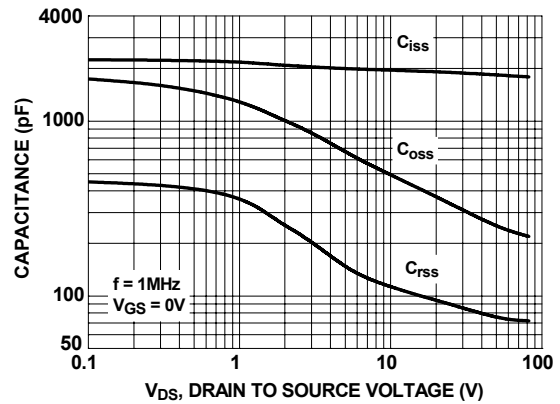
Figure 8. Capacitance vs Drain to Source Voltage

Axis: CAPACITANCE (pF); V_{DS}, DRAIN TO SOURCE VOLTAGE (V); C_{iss}, C_{oss}, C_{rss}; f = 1MHz, V_{GS} = 0V
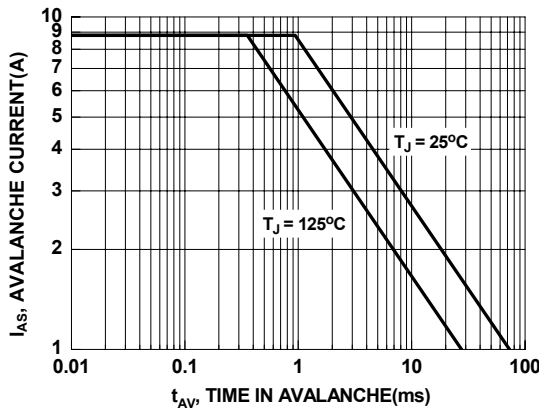
Figure 9. Unclamped Inductive Switching Capability

Axis: I_{AS}, AVALANCHE CURRENT(A); t_{AV}, TIME IN AVALANCHE(ms); T_J = 25°C, T_J = 125°C
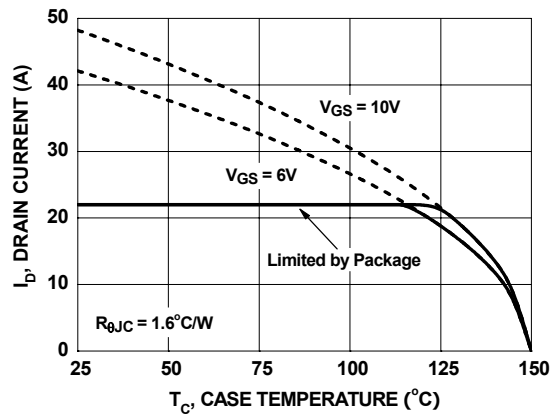
Figure 10. Maximum Continuous Drain Current vs Case Temperature

Axis: I_D, DRAIN CURRENT (A); T_C, CASE TEMPERATURE (°C); V_{GS} = 10V, V_{GS} = 6V; Limited by Package; $R_{\theta JC}$ = 1.6°C/W
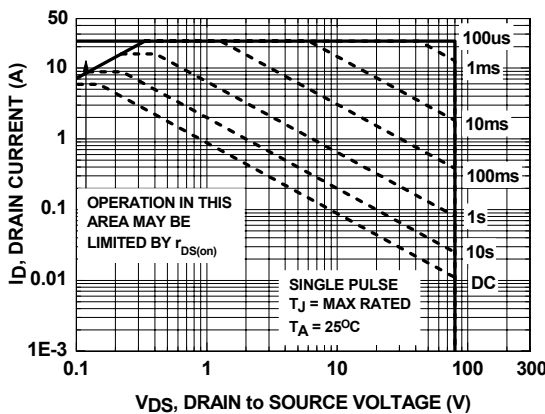
Figure 11. Forward Bias Safe Operating Area

Axis: I_D, DRAIN CURRENT (A); V_{DS}, DRAIN to SOURCE VOLTAGE (V); 100us, 1ms, 10ms, 100ms, 1s, 10s, DC; OPERATION IN THIS AREA MAY BE LIMITED BY $r_{DS(on)}$; SINGLE PULSE T_J = MAX RATED T_A = 25°C
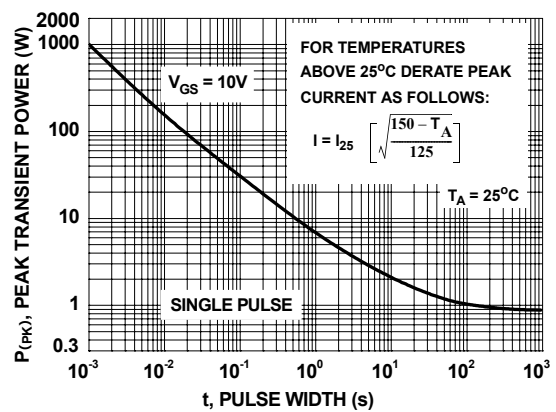
Figure 12. Single Pulse Maximum Power Dissipation

Axis: $P_{(PK)}$, PEAK TRANSIENT POWER (W); t, PULSE WIDTH (s); V_{GS} = 10V; FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_{25}\left[\sqrt{\frac{150 - T_A}{125}}\right]$$

T_A = 25°C; SINGLE PULSE

Typical Characteristics T_J = 25°C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

NOTES:
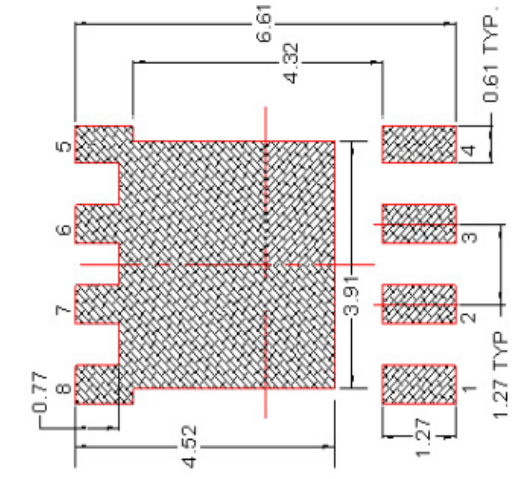DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_A$
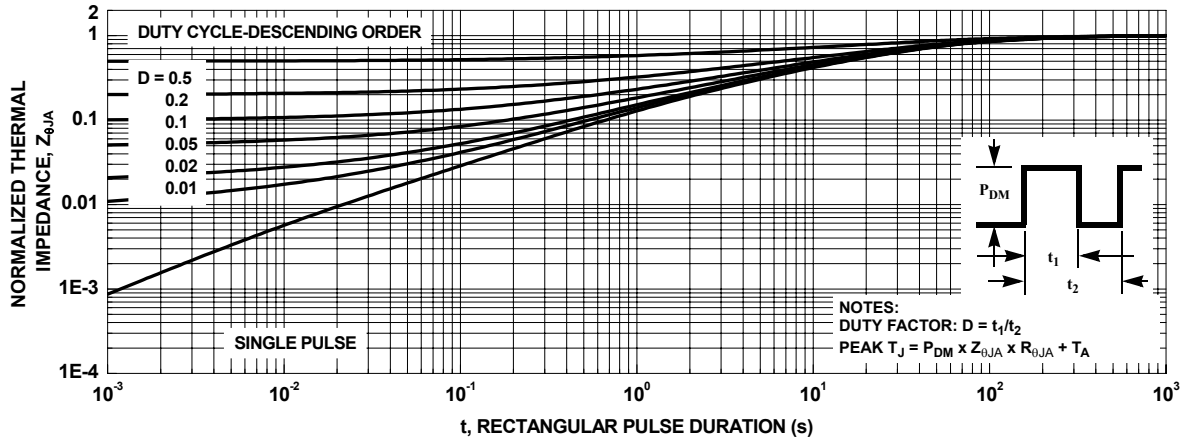
Figure 13. Transient Thermal Response Curve

RECOMMENDED LAND PATTERN

TOP VIEW

SIDE VIEW

SEATING PLANE

BOTTOM VIEW

PIN #1 IDENT

PIN #1 IDENT
(OPTIONAL)
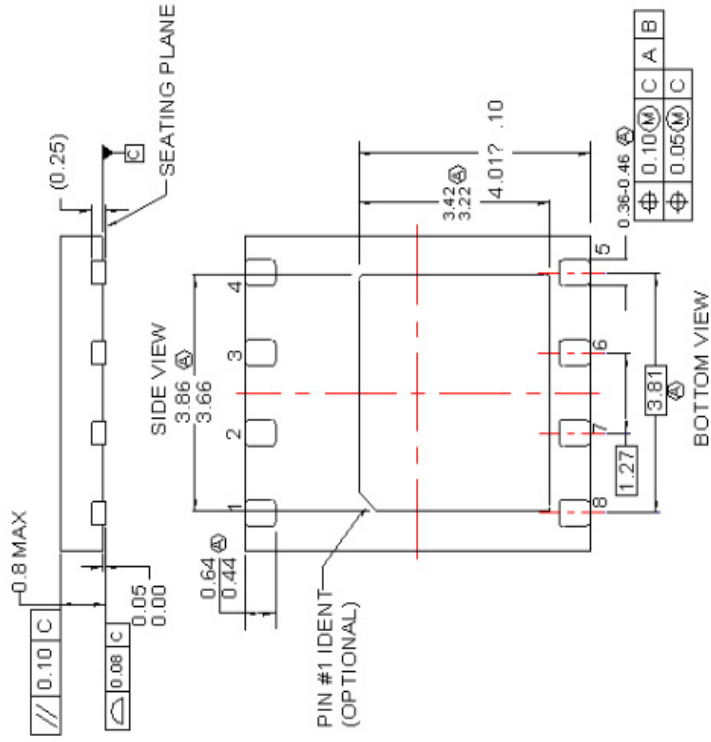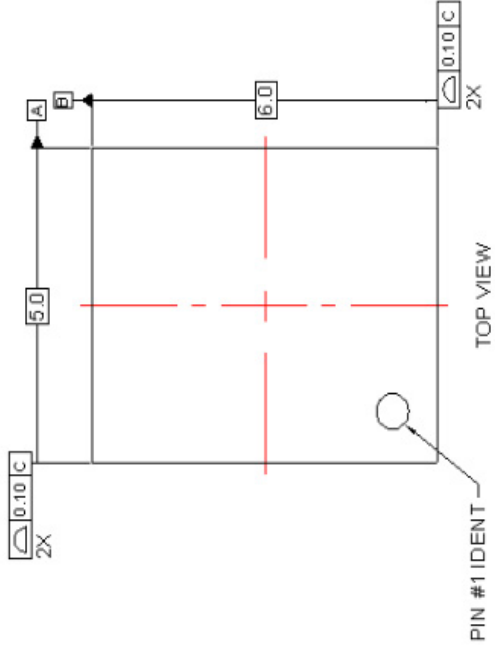
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C. DIMENSIONS AND TOLERANCES PER
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D. TERMINALS 5,6,7 AND 8 ARE TIED
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