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October 2014

# FDMS86105

## N-Channel Shielded Gate PowerTrench® MOSFET

### 100 V, 26 A, 34 mΩ

## Features

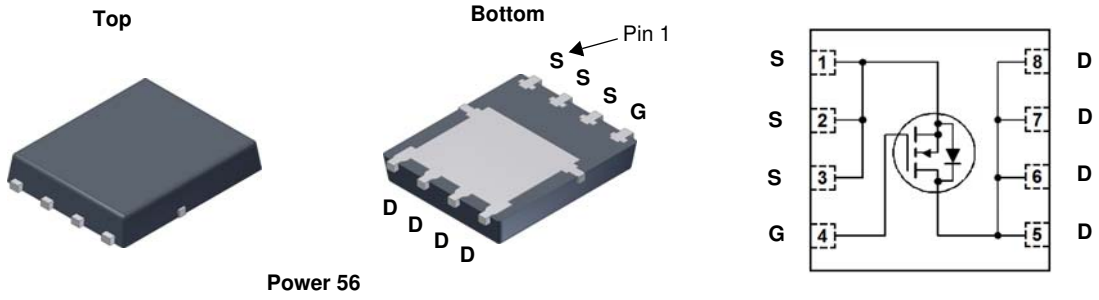
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 34 mΩ at $V_{GS}$ = 10 V, $I_D$ = 6 A
- Max $r_{DS(on)}$ = 54 mΩ at $V_{GS}$ = 6 V, $I_D$ = 4.5 A
- Advanced package and silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

## General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

## Applications

- Primary DC-DC
- Secondary DC-DC
- Load Switch




Power 56

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 100 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | | 26 | A |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | 6 | |
| | -Pulsed | | | 30 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 50 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 48 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 2.6 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50 | |

### Package Marking and Ordering Information

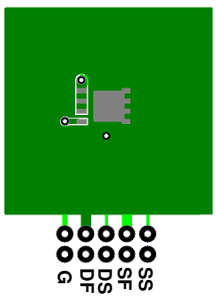
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS86105 | FDMS86105 | Power 56 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

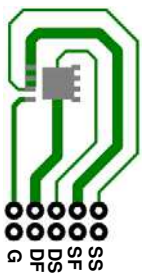
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 100 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 70 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.0 | 2.8 | 4.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -9 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 6 A | | 27 | 34 | mΩ |
| | | $V_{GS}$ = 6 V, $I_D$ = 4.5 A | | 37 | 54 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 6 A, $T_J$ = 125 °C | | 46 | 57 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 6 A | | 15 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | | 483 | 645 | pF |
| $C_{oss}$ | Output Capacitance | | | 114 | 155 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 5 | 10 | pF |
| $R_g$ | Gate Resistance | | | 0.9 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 6 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 6.7 | 14 | ns |
| $t_r$ | Rise Time | | | 2.1 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 12 | 22 | ns |
| $t_f$ | Fall Time | | | 2.4 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 50 V, $I_D$ = 6 A | | 7.5 | 11 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 5 V; $V_{DD}$ = 50 V, $I_D$ = 6 A | | 4.2 | 6 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 50 V, $I_D$ = 6 A | | 2.1 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 1.7 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source-Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2 A (Note 2) | | 0.76 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 6 A (Note 2) | | 0.82 | 1.3 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 6 A, di/dt = 100 A/μs | | 38 | 61 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 32 | 51 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a. 50 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.




b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25 °C, L = 1 mH, $I_{AS}$ = 10 A, $V_{DD}$ = 90 V, $V_{GS}$ = 10 V.

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

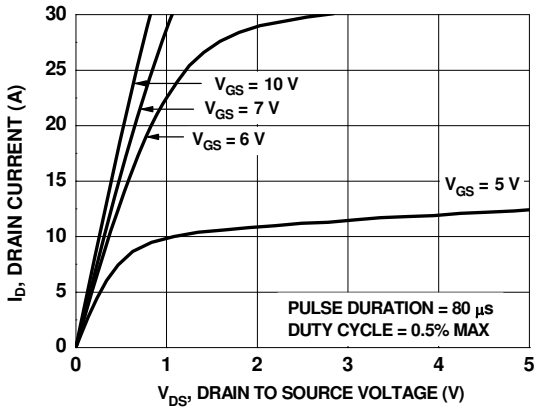



**Figure 1. On Region Characteristics**

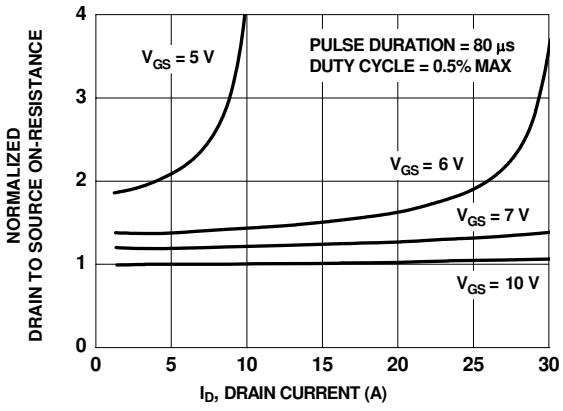



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

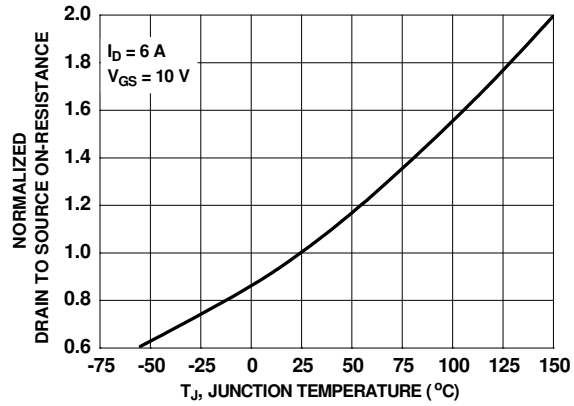



**Figure 3. Normalized On Resistance vs Junction Temperature**

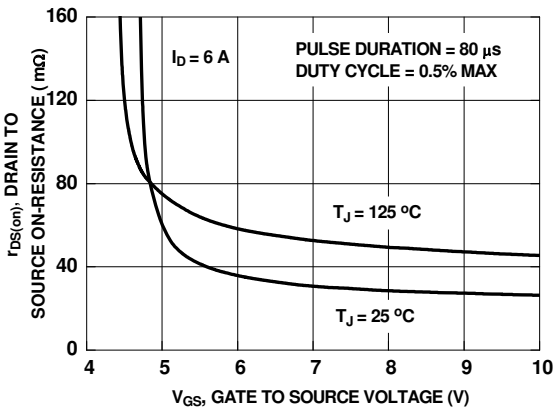



**Figure 4. On-Resistance vs Gate to Source Voltage**

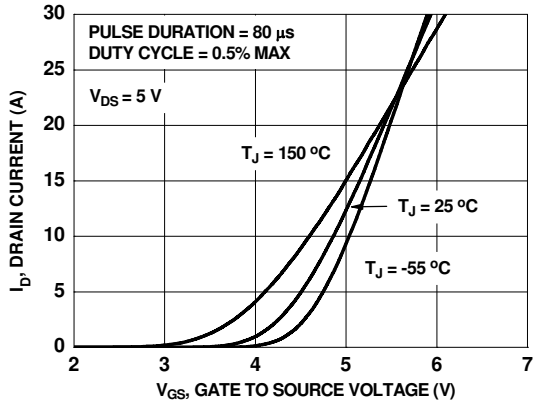



**Figure 5. Transfer Characteristics**

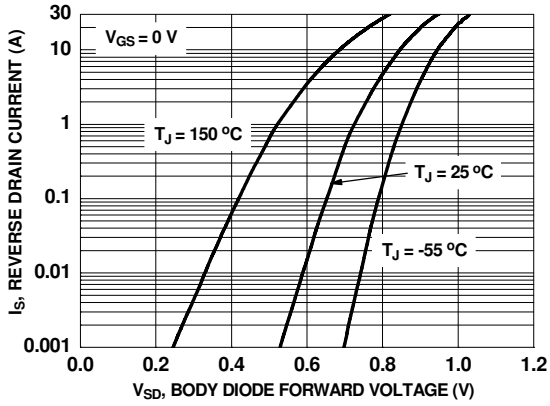



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

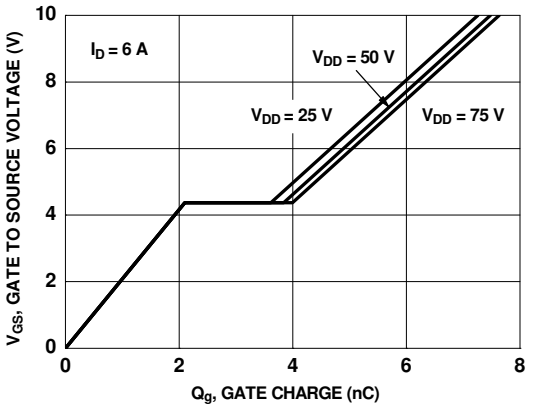



**Figure 7. Gate Charge Characteristics**

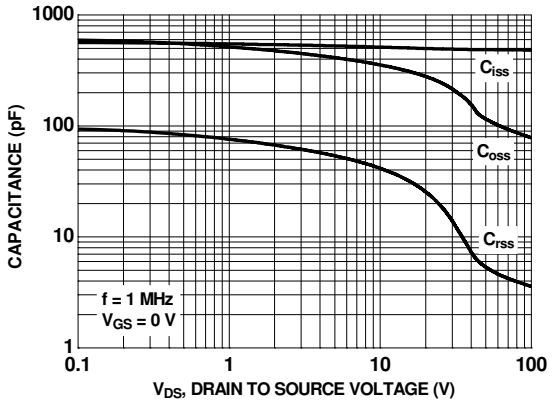



**Figure 8. Capacitance vs Drain to Source Voltage**

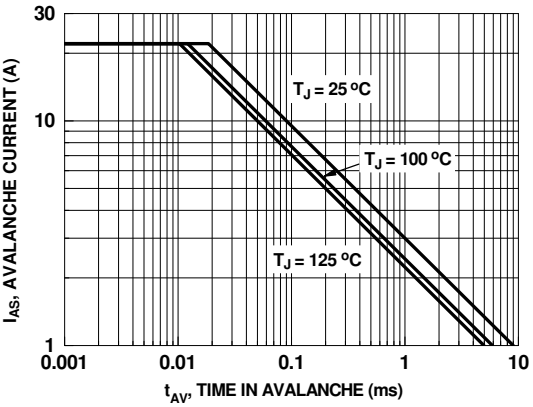



**Figure 9. Unclamped Inductive Switching Capability**

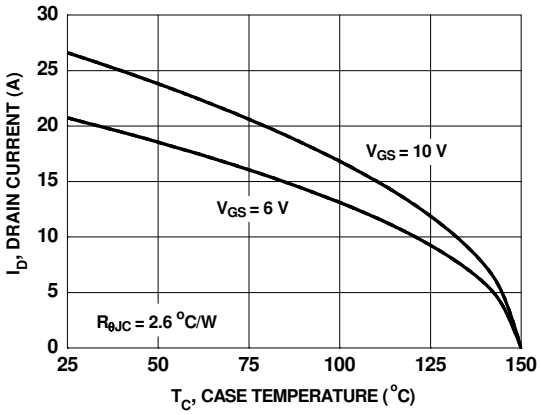



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

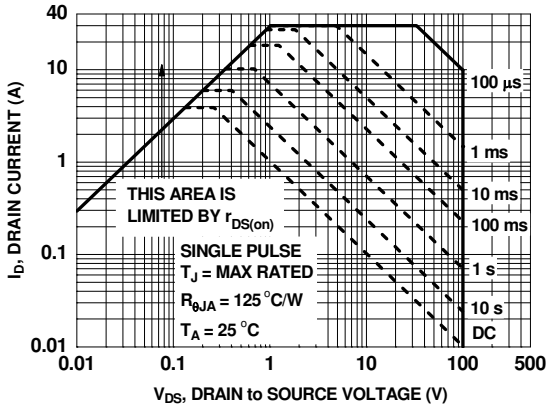



**Figure 11. Forward Bias Safe Operating Area**

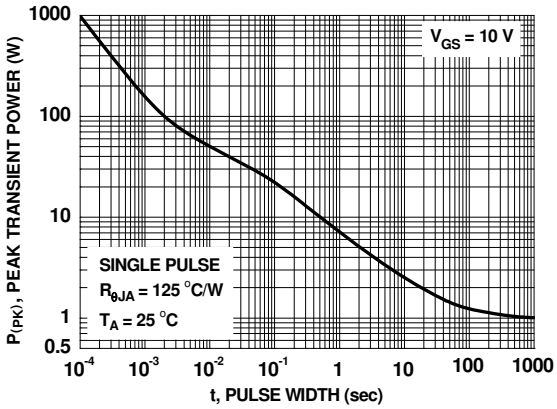



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

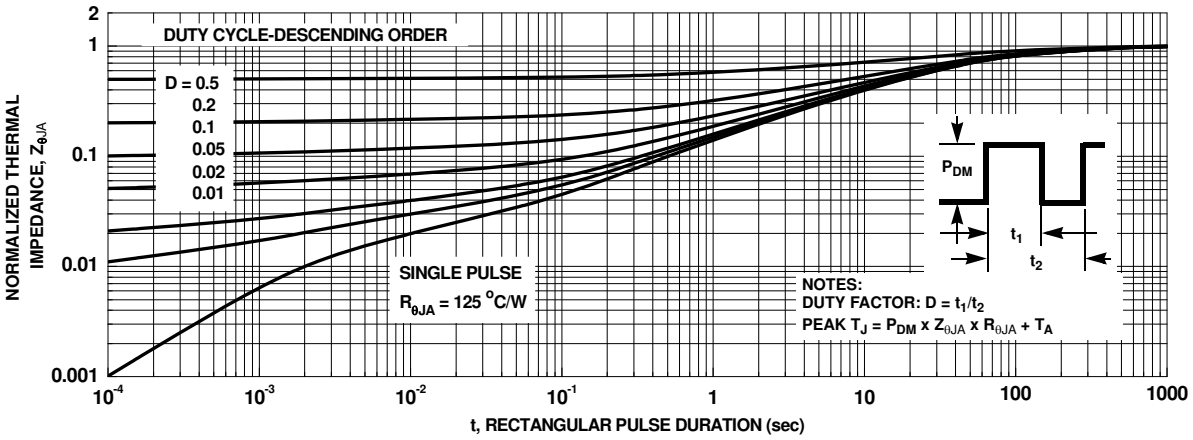
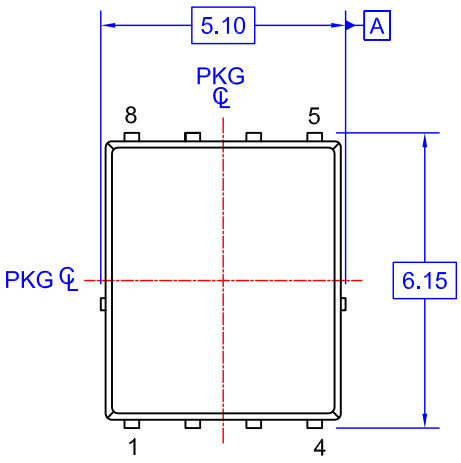
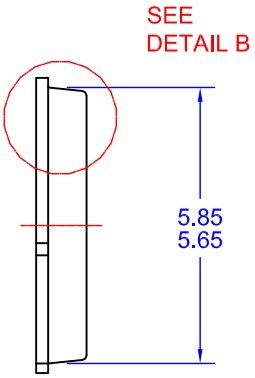
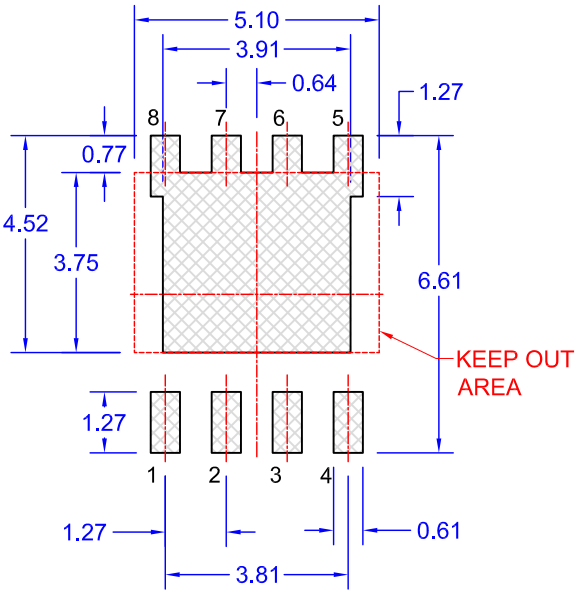



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

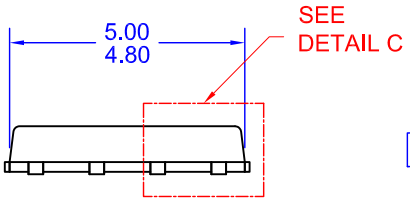



TOP VIEW

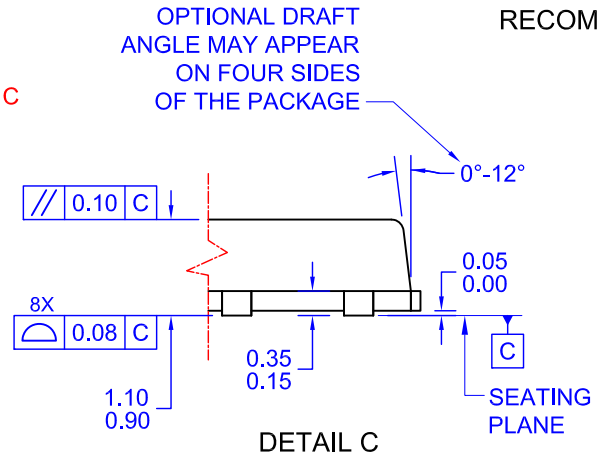


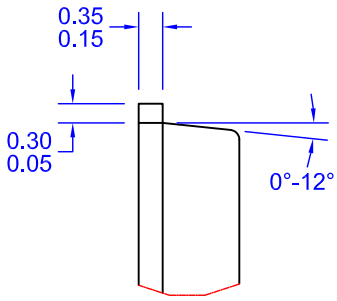

LAND PATTERN
RECOMMENDATION



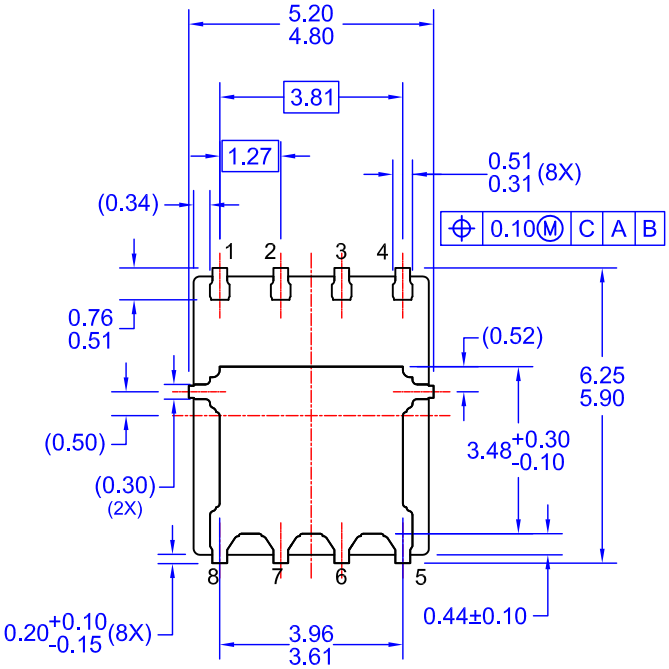

SIDE VIEW




DETAIL C
SCALE: 2:1




DETAIL B
SCALE: 2:1




BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
F. DRAWING FILE NAME: PQFN08AREV10

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