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August 2003

FAIRCHILD SEMICONDUCTOR®

FDQ7698S

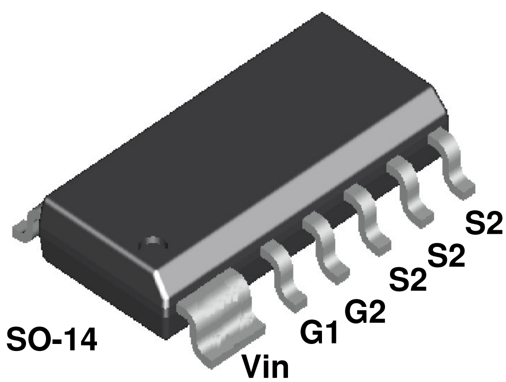
Dual Notebook Power Supply N-Channel PowerTrench® in SO-14 Package

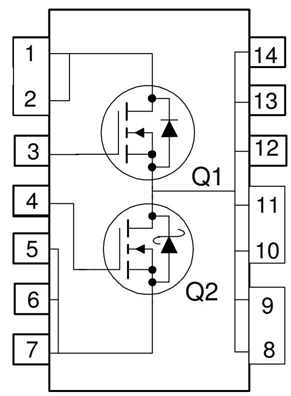
General Description

The FDQ7698S is designed to replace two single SO-8 MOSFETs in DC to DC power supplies The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses using Fairchild's SyncFET ™ technology.

Features

- **Q2**: 15 A, 30V. $R_{DS(on)}$ = 7.5 mΩ @ V_{GS} = 10V
  $R_{DS(on)}$ = 9 mΩ @ V_{GS} = 4.5V
- **Q1**: 12A, 30V. $R_{DS(on)}$ = 12 mΩ @ V_{GS} = 10V
  $R_{DS(on)}$ = 16 mΩ @ V_{GS} = 4.5V





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±16	±16	V
I_D	Drain Current - Continuous	(Note 1a)	15	12	A
	- Pulsed		50	50	
P_D	Power Dissipation for Single Operation	(Note 1a & 1b)	2.4	1.8	W
		(Note 1c & 1d)	1.3	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a & 1b)	52	68	°C/W
		(Note 1c & 1d)	94	118	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDQ7698S	FDQ7698S	13"	16mm	2500 units

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 1$ mA $V_{GS} = –5$ V, $I_D = 1$ mA $V_{GS} = 0$ V, $I_D = 250$ µA	Q2 Q1	30 20 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10$ mA, Referenced to 25°C $I_D = 250$ µA, Referenced to 25°C	Q2 Q1		22 28		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V	Q2 Q1			500 10	µA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 16$ V, $V_{DS} = 0$ V	Q2 Q1			100 100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = –16$ V, $V_{DS} = 0$ V	Q2 Q1			–100 –100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1$ mA $V_{DS} = V_{GS}$, $I_D = 250$ µA	Q2 Q1	1.17 1	1.3 1.3	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 10$ mA, Referenced to 25°C $I_D = 250$ µA, Referenced to 25°C	Q2 Q1		–3 –6		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 15$ A $V_{GS} = 4.5$ V, $I_D = 14$ A $V_{GS} = 10$ V, $I_D = 15$ A, $T_J = 125°C$	Q2		5.3 6 7.7	7.5 9 12	mΩ
		$V_{GS} = 10$ V, $I_D = 12$ A $V_{GS} = 4.5$ V, $I_D = 11$ A $V_{GS} = 10$ V, $I_D = 12$ A, $T_J = 125°C$	Q1		9.4 12.6 17	12 16 21	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10$ V, $V_{DS} = 5$ V	Q2 Q1	50 50			A
g_{FS}	Forward Transconductance	$V_{DS} = 10$ V, $I_D = 15$ A $V_{DS} = 10$ V, $I_D = 12$ A	Q2 Q1		80 38		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, f = 1.0 MHz	Q2 Q1		4814 1324		pF
C_{oss}	Output Capacitance		Q2 Q1		842 300		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		321 98		pF
R_G	Gate Resistance	$V_{GS} = 15$ mVf = 1.0 MHz	Q2 Q1		1.5 1.2		Ω
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10$V, $R_{GEN} = 6$ Ω	Q2 Q1		16 10	29 20	nS
t_r	Turn-On Rise Time		Q2 Q1		14 12	25 22	nS
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		90 28	144 45	nS
t_f	Turn-Off Fall Time		Q2 Q1		32 11	51 20	nS
Q_g	Total Gate Charge	Q2 $V_{DS} = 15$ V, $I_D = 15$ A, $V_{GS} = 5$ V	Q2 Q1		43 12	60 17	nC
Q_{gs}	Gate-Source Charge	Q1	Q2 Q1		8.5 3.6		nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = 15$ V, $I_D = 12$ A, $V_{GS} = 5$ V	Q2 Q1		11 3.7		nC

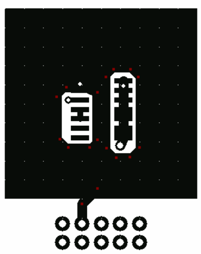
Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			3.5 2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.5 A (Note 2) V_{GS} = 0 V, I_S = 7 A (Note 2) V_{GS} = 0 V, I_S = 2.1 A (Note 2)	Q2 Q1		0.4 0.5 0.7	0.7 1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 15A,	Q2		26		nS
Q_{rr}	Diode Reverse Recovery Charge	d_{iF}/d_t = 300 A/µs (Note 3)			29		nC
t_{rr}	Diode Reverse Recovery Time	I_F = 12A,	Q1		25		nS
Q_{rr}	Diode Reverse Recovery Charge	d_{iF}/d_t = 100 A/µs (Note 3)			14		nC

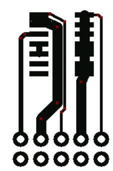
NOTE :

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 68°C/W when mounted on a 1in^2 pad of 2 oz copper (Q1).

b) 52°C/W when mounted on a 1in^2 pad of 2 oz copper (Q2).



c) 118°C/W when mounted on a minimum pad of 2 oz copper (Q1).

d) 94°C/W when mounted on a minimum pad of 2 oz copper (Q2).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

See "SyncFET Schottky diode characteristics" below.

Typical Characteristics : Q2

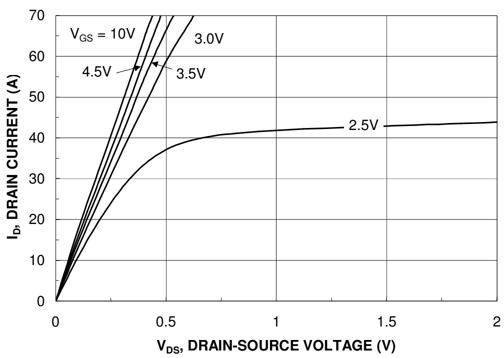


Figure 1. On-Region Characteristics.

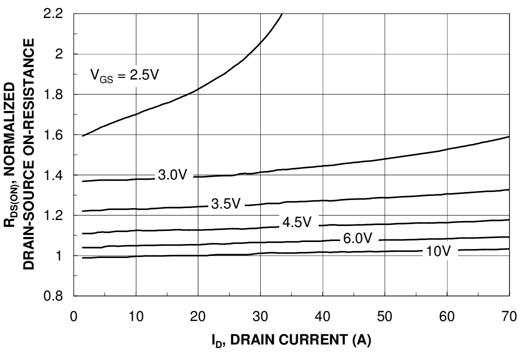


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

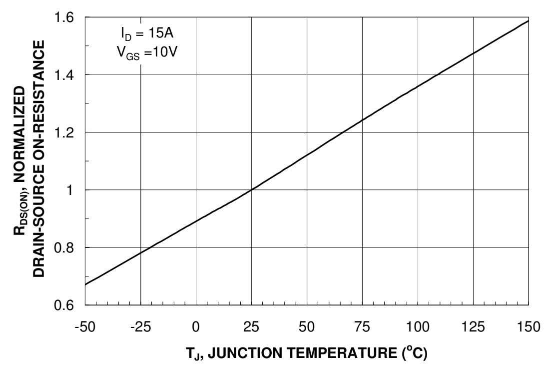


Figure 3. On-Resistance Variation with Temperature.

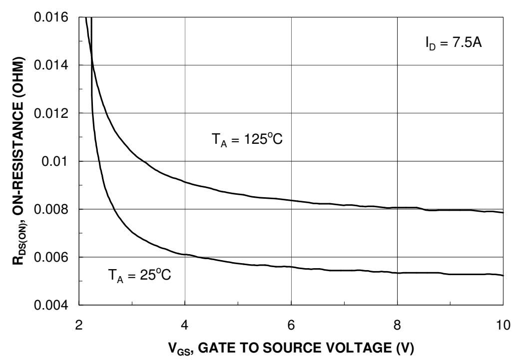


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

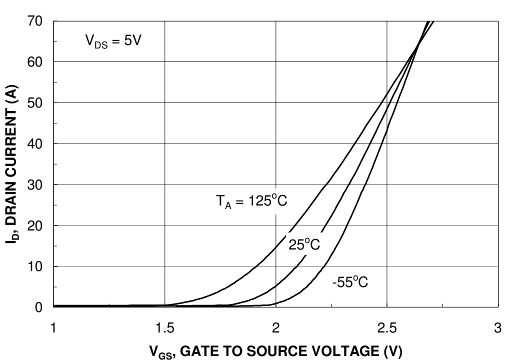


Figure 5. Transfer Characteristics.

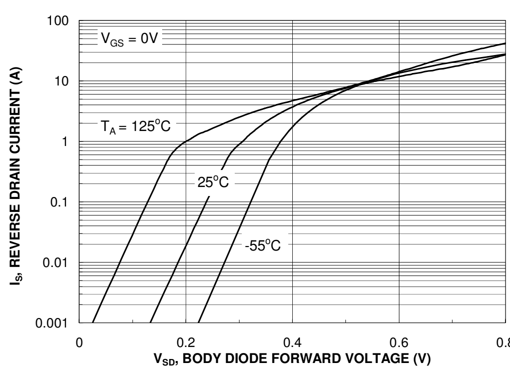


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q2

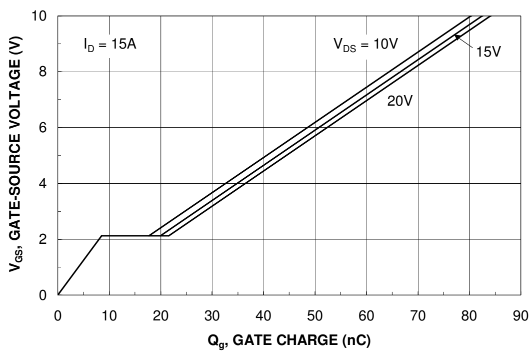


Figure 7. Gate Charge Characteristics.

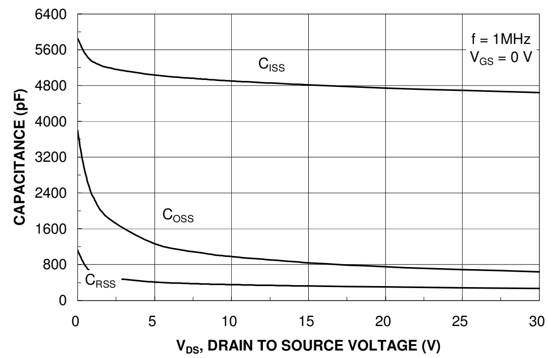


Figure 8. Capacitance Characteristics.

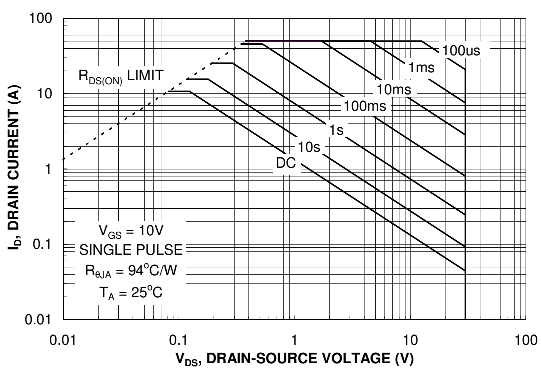


Figure 9. Maximum Safe Operating Area.

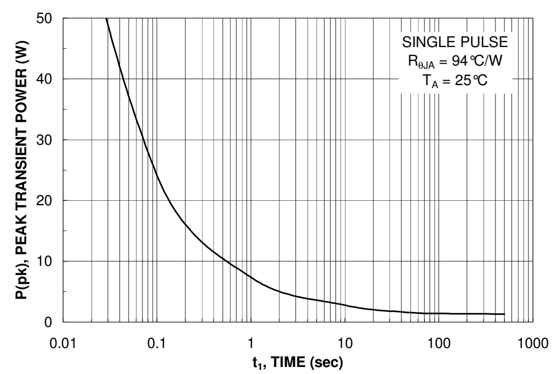


Figure 10. Single Pulse Maximum Power Dissipation.

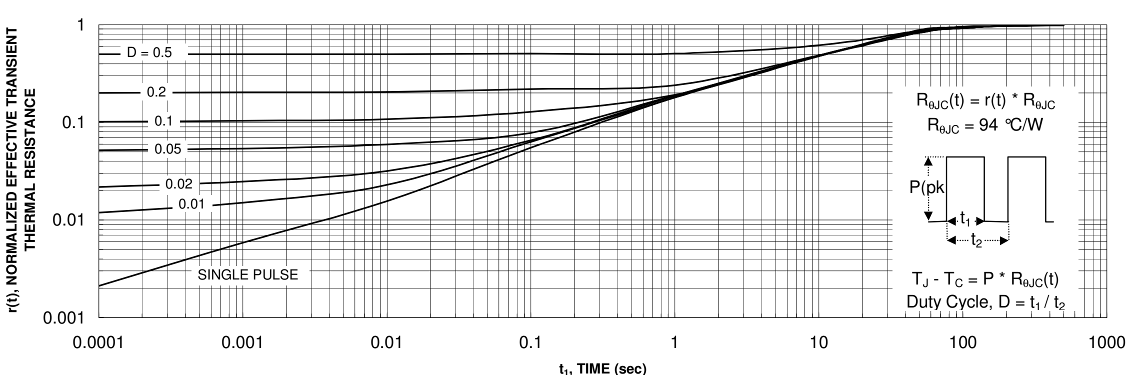


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1d.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics : Q2

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDQ7698S Q2.

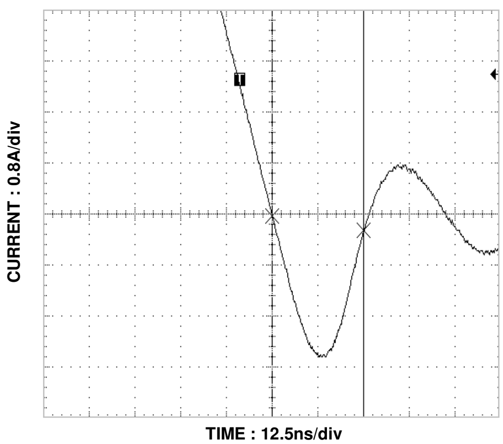


Figure 12. FDQ7698S SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET(FDS6676).

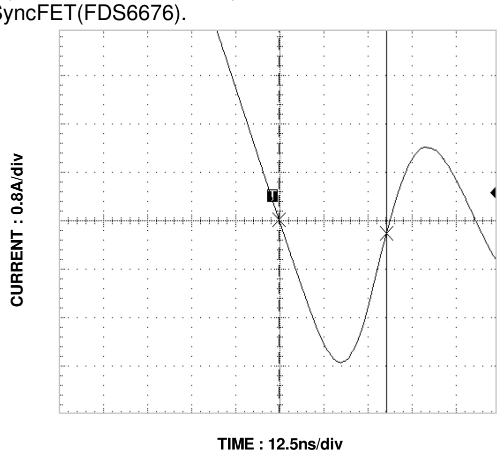


Figure 13. Non-SyncFET (FDS6676) body Diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

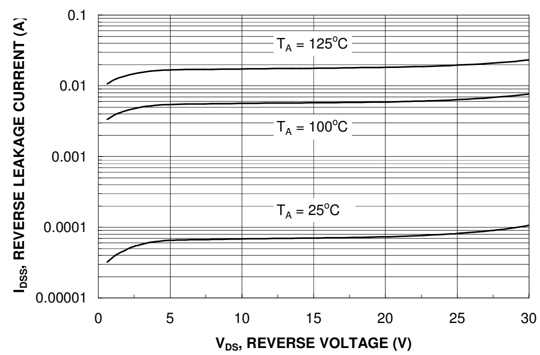


Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.

Additional SyncFET Characteristics

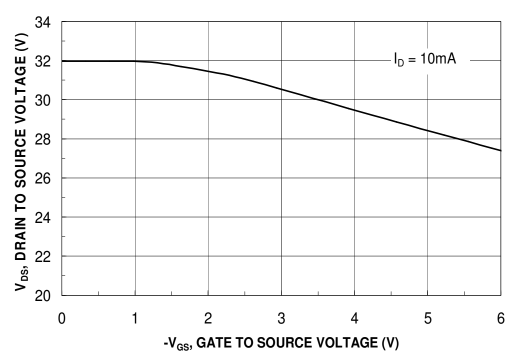


Figure 15. SyncFET Drain to Source Voltage Variation With Negative Gate to Source Bias.

Typical Characteristics: Q1

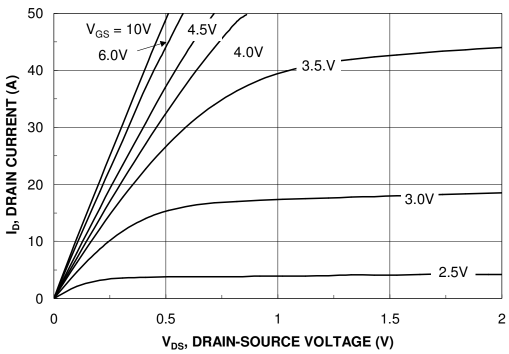


Figure 16. On-Region Characteristics.

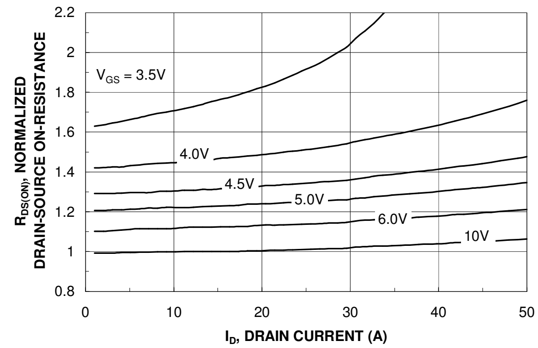


Figure 17. On-Resistance Variation with Drain Current and Gate Voltage.

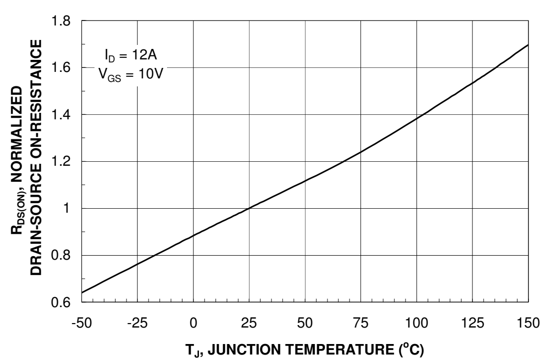


Figure 18. On-Resistance Variation with Temperature.

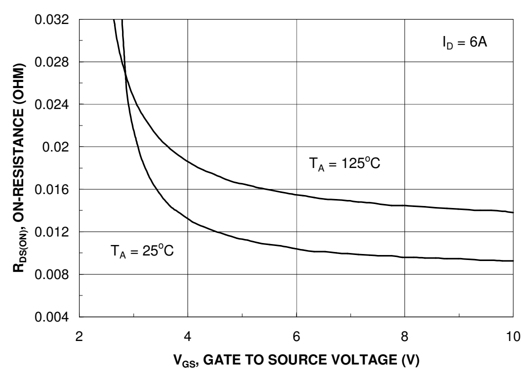


Figure 19. On-Resistance Variation with Gate-to-Source Voltage.

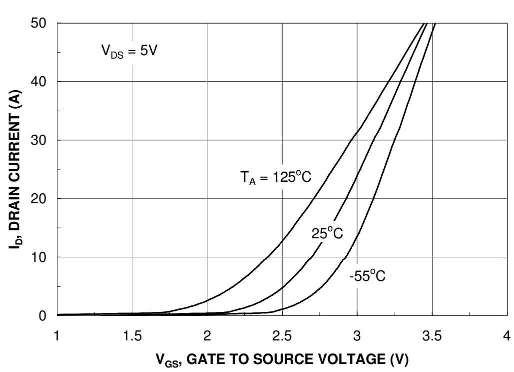


Figure 20. Transfer Characteristics.

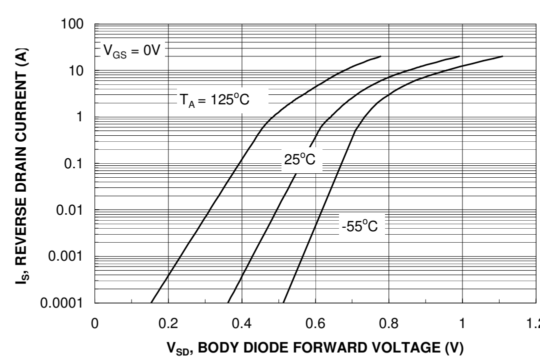


Figure 21. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q1

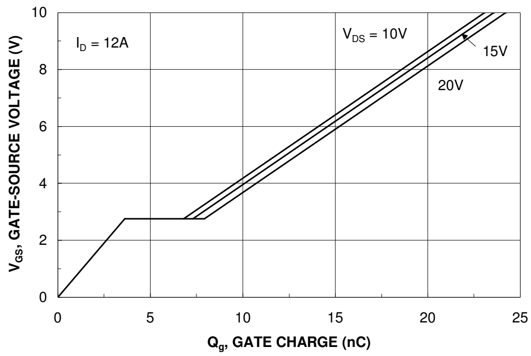


Figure 22. Gate Charge Characteristics.

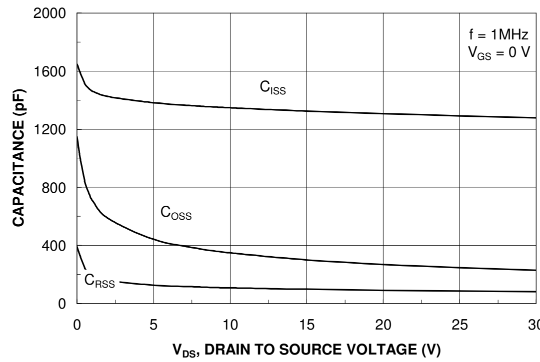


Figure 23. Capacitance Characteristics.

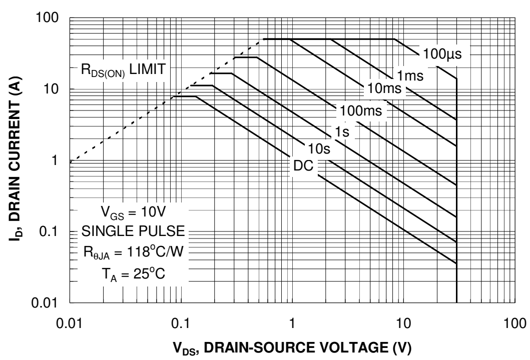


Figure 24. Maximum Safe Operating Area.

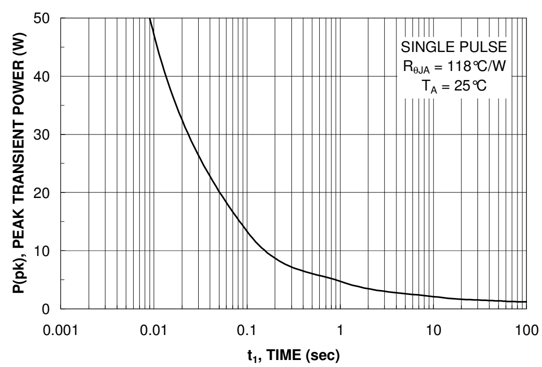


Figure 25. Single Pulse Maximum Power Dissipation.

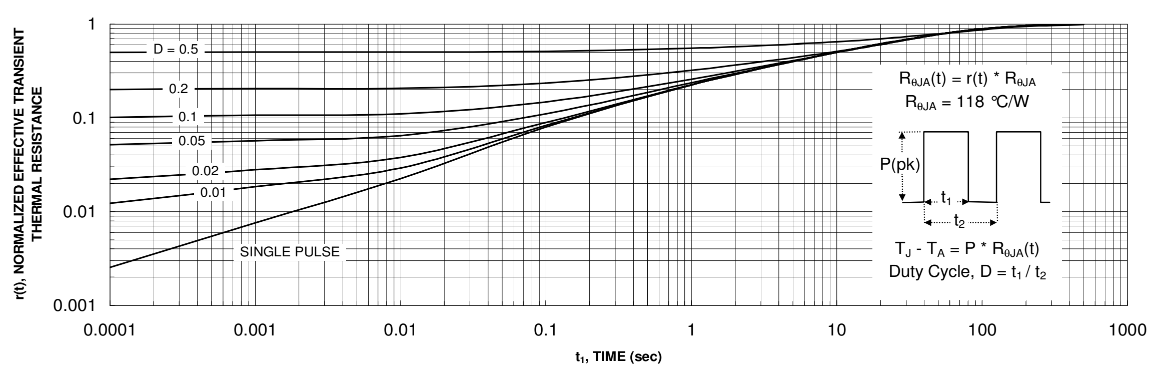
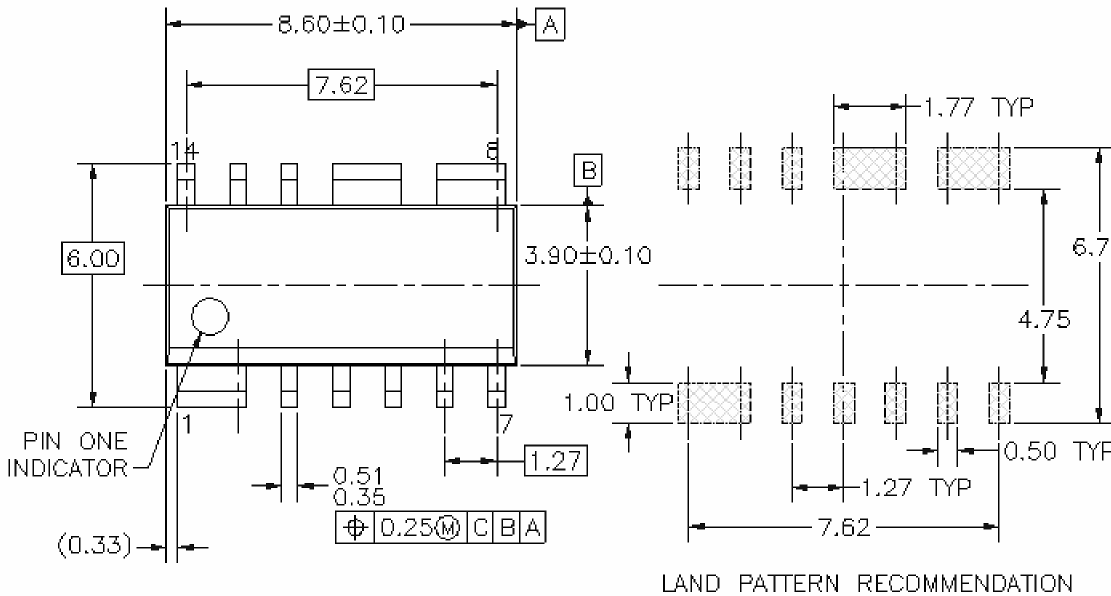
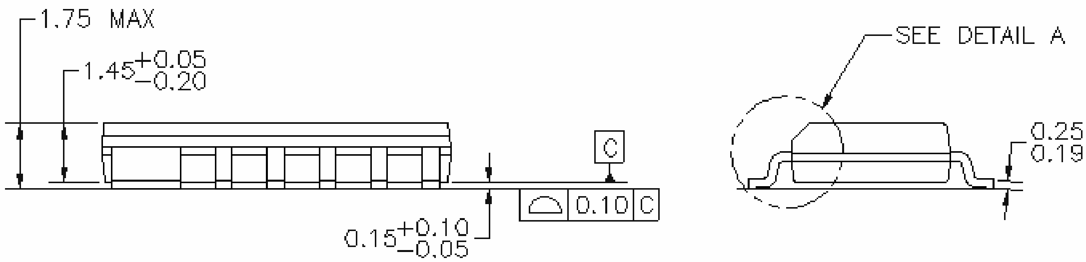


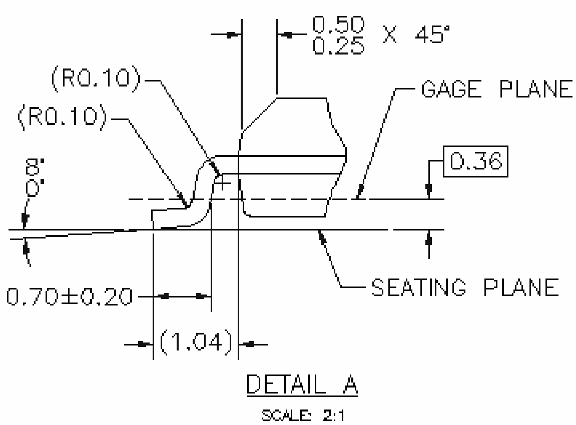
Figure 26. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout







NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

D) STANDARD LEAD FINISH: 200 MICROINCHES / 5.08 MICRONS MIN. LEAD/TIN (SOLDER) ON COPPER.

M14PS2REVA

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.