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FAIRCHILD SEMICONDUCTOR™

April 2002

# FDS4559

## 60V Complementary PowerTrench®MOSFET

### General Description

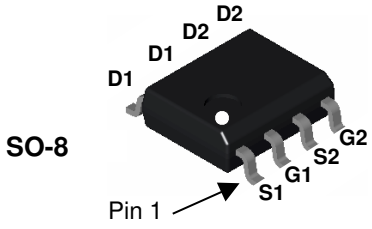
This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

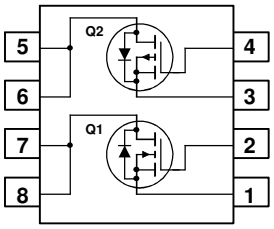
### Applications

- DC/DC converter
- Power management
- LCD backlight inverter

### Features

- **Q1**: **N-Channel**
  4.5 A, 60 V $R_{DS(on)}$ = 55 mΩ @ $V_{GS}$ = 10V
  $R_{DS(on)}$ = 75 mΩ @ $V_{GS}$ = 4.5V
- **Q2**: **P-Channel**
  –3.5 A, –60 V $R_{DS(on)}$ = 105 mΩ @ $V_{GS}$ = –10V
  $R_{DS(on)}$ = 135 mΩ @ $V_{GS}$ = –4.5V




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Q1 | Q2 | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 60 | –60 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 4.5 | –3.5 | A |
| | - Pulsed | | 20 | –20 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2 | | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | | |
| | | (Note 1b) | 1.2 | | |
| | | (Note 1c) | 1 | | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +175 | | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS4559 | FDS4559 | 13” | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings** (Note 1) | | | | | | | |
| $W_{DSS}$ | Single Pulse Drain-Source Avalanche Energy | $V_{DD}$ = 30 V, $I_D$ = 4.5 A | Q1 | | | 90 | mJ |
| $I_{AR}$ | Maximum Drain-Source Avalanche Current | | Q1 | | | 4.5 | A |
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA<br>$V_{GS}$ = 0 V, $I_D$ = –250 µA | Q1<br>Q2 | 60<br>–60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C<br>$I_D$ = –250 µA, Referenced to 25°C | Q1<br>Q2 | | 58<br>–49 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = –48 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | 1<br>–1 | µA |
| $I_{GSS}$ | Gate-Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V<br>$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | Q1<br>Q2 | | | ±100<br>±100 | nA |
| **On Characteristics** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA<br>$V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | Q1<br>Q2 | 1<br>–1 | 2.2<br>–1.6 | 3<br>–3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C<br>$I_D$ = –250 µA, Referenced to 25°C | Q1<br>Q2 | | –5.5<br>4 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 4.5 A<br>$V_{GS}$ = 10 V, $I_D$ = 4.5 A, $T_J$ = 125°C<br>$V_{GS}$ = 4.5 V, $I_D$ = 4 A | Q1 | | 42<br>72<br>55 | 55<br>94<br>75 | mΩ |
| | | $V_{GS}$ = –10 V, $I_D$ = –3.5 A<br>$V_{GS}$ = –10 V, $I_D$ = –3.5 A, $T_J$ = 125°C<br>$V_{GS}$ = –4.5 V, $I_D$ = –3.1 A | Q2 | | 82<br>130<br>105 | 105<br>190<br>135 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V<br>$V_{GS}$ = –10 V, $V_{DS}$ = –5 V | Q1<br>Q2 | 20<br>–20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 4.5 A<br>$V_{DS}$ = –5 V, $I_D$ = –3 5 A | Q1<br>Q2 | | 14<br>9 | | S |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | Q1<br>$V_{DS}$ = 25 V, $V_{GS}$ = 0 V,<br>f = 1.0 MHz<br>Q2<br>$V_{DS}$ = –30 V, $V_{GS}$ = 0 V,<br>f = 1.0 MHz | Q1<br>Q2 | | 650<br>759 | | pF |
| $C_{oss}$ | Output Capacitance | | Q1<br>Q2 | | 80<br>90 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 35<br>39 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | Q1<br>$V_{DD}$ = 30 V, $I_D$ = 1 A,<br>$V_{GS}$ = 10V, $R_{GEN}$ = 6 Ω<br>Q2<br>$V_{DD}$ = –30 V, $I_D$ = –1 A,<br>$V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 11<br>7 | 20<br>14 | ns |
| $t_r$ | Turn-On Rise Time | | Q1<br>Q2 | | 8<br>10 | 18<br>20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q1<br>Q2 | | 19<br>19 | 35<br>34 | ns |
| $t_f$ | Turn-Off Fall Time | | Q1<br>Q2 | | 6<br>12 | 15<br>22 | ns |
| $Q_g$ | Total Gate Charge | Q1<br>$V_{DS}$ = 30 V, $I_D$ = 4.5 A, $V_{GS}$ = 10 V<br>Q2<br>$V_{DS}$ = –30 V, $I_D$ = –3.5 A, $V_{GS}$ = –10V | Q1<br>Q2 | | 12.5<br>15 | 18<br>21 | nC |
| $Q_{gs}$ | Gate-Source Charge | | Q1<br>Q2 | | 2.4<br>2.5 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | Q1<br>Q2 | | 2.6<br>3.0 | | nC |

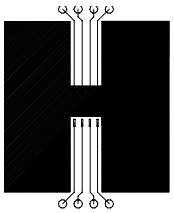
## Electrical Characteristics (continued)

$T_A$ = 25°C unless otherwise noted

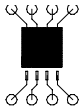
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | Q1<br>Q2 | | | 1.3<br>–1.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = –1.3 A (Note 2) | Q1<br>Q2 | | 0.8<br>–0.8 | 1.2<br>–1.2 | V |

**Notes:**

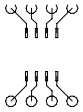
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 $in^2$ pad of 2 oz copper



b) 125°C/W when mounted on a .02 $in^2$ pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

## Typical Characteristics: Q2

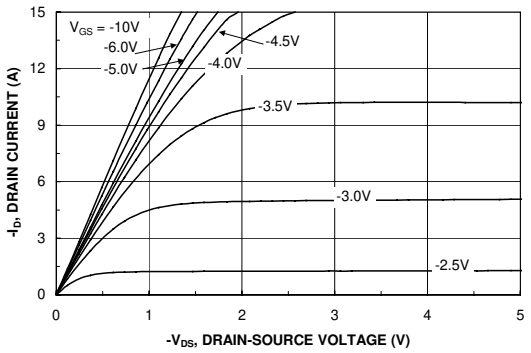



**Figure 1. On-Region Characteristics.**

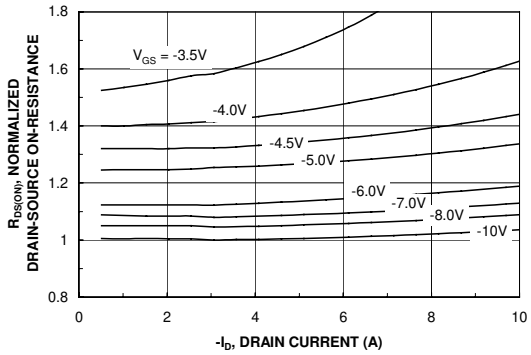



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

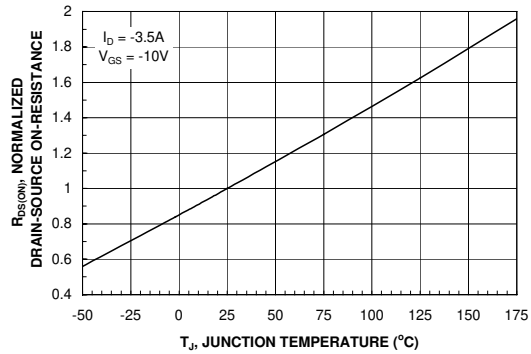



**Figure 3. On-Resistance Variation with Temperature.**

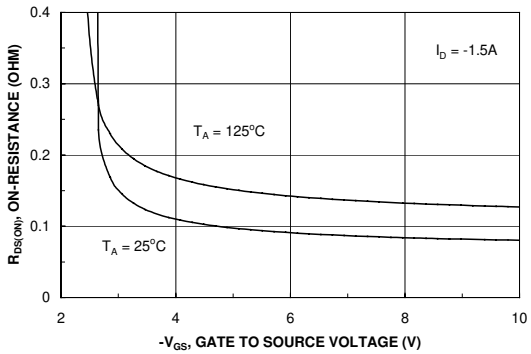



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

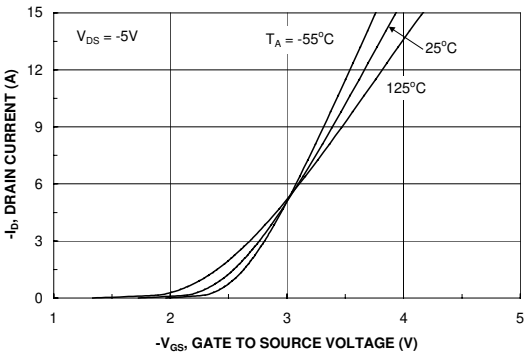



**Figure 5. Transfer Characteristics.**

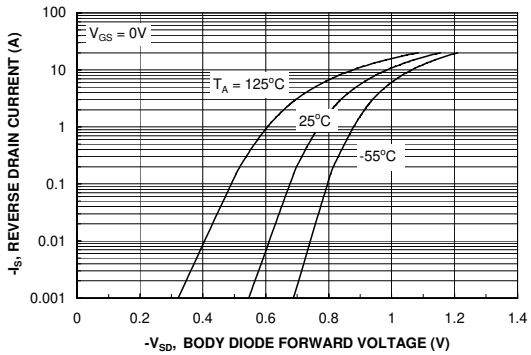



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: Q2

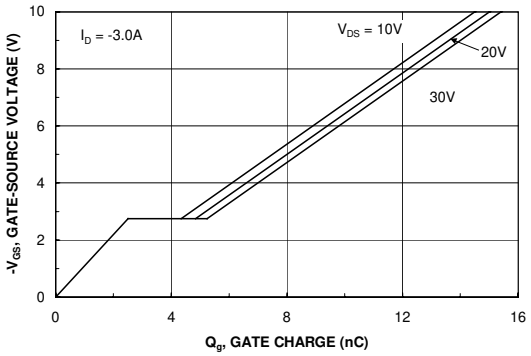



**Figure 7. Gate Charge Characteristics.**

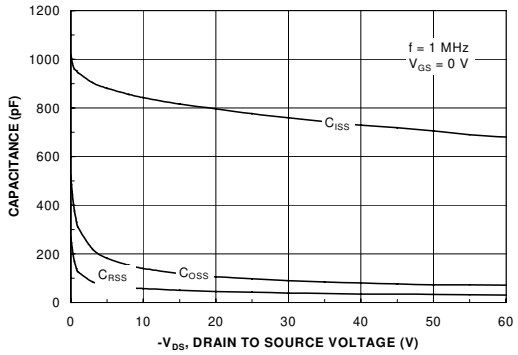



**Figure 8. Capacitance Characteristics.**

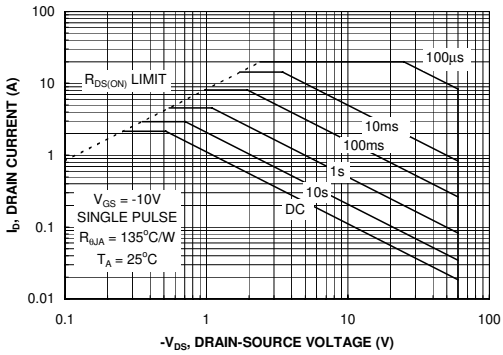



**Figure 9. Maximum Safe Operating Area.**

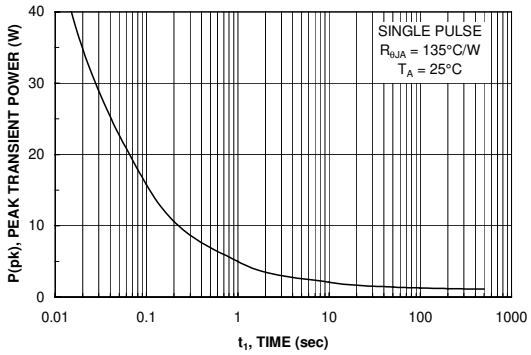



**Figure 10. Single Pulse Maximum Power Dissipation.**

## Typical Characteristics: Q1

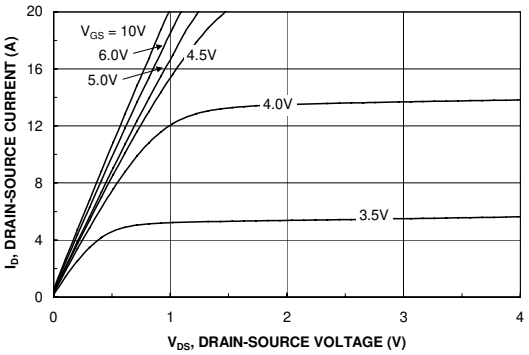



**Figure 11. On-Region Characteristics.**

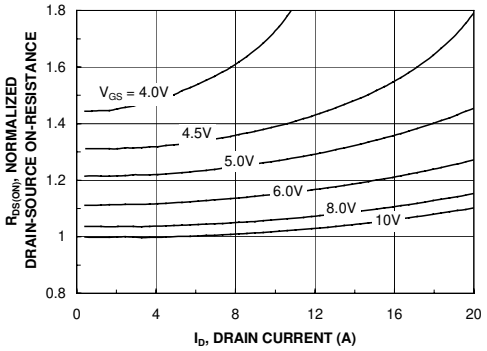



**Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.**

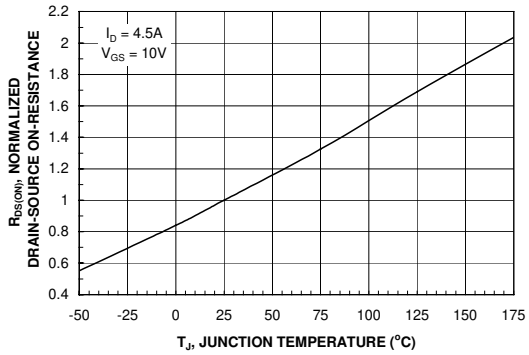



**Figure 13. On-Resistance Variation with Temperature.**

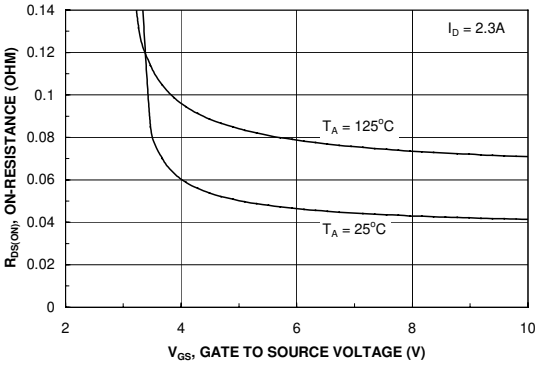



**Figure 14. On-Resistance Variation with Gate-to-Source Voltage.**

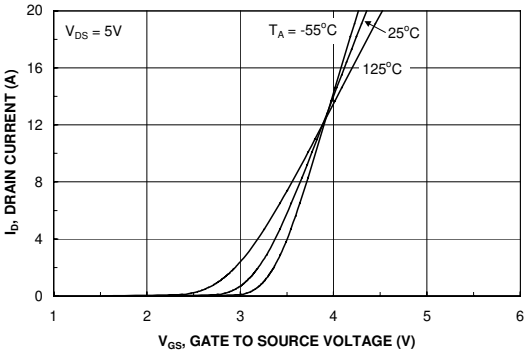



**Figure 15. Transfer Characteristics.**

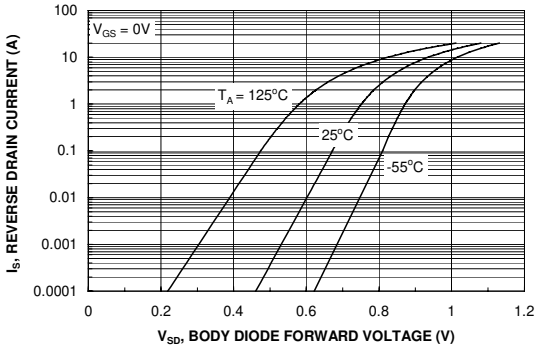



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: Q1

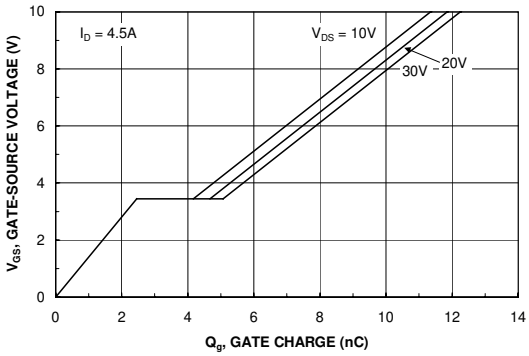



**Figure 17. Gate Charge Characteristics.**

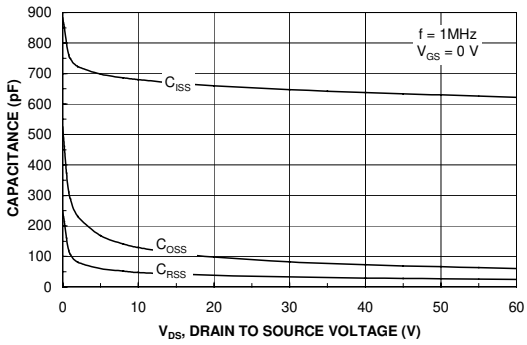



**Figure 18. Capacitance Characteristics.**

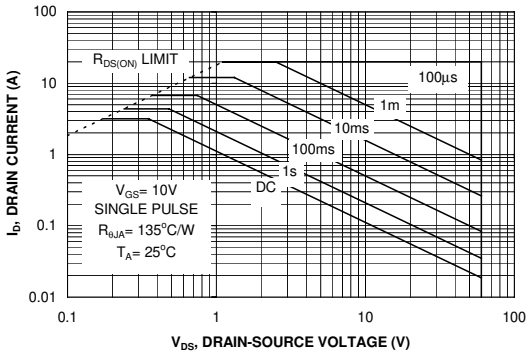



**Figure 19. Maximum Safe Operating Area.**

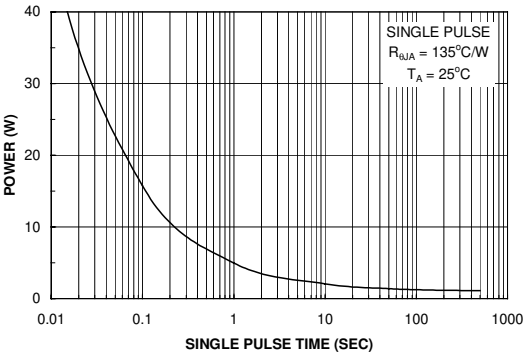



**Figure 20. Single Pulse Maximum Power Dissipation.**

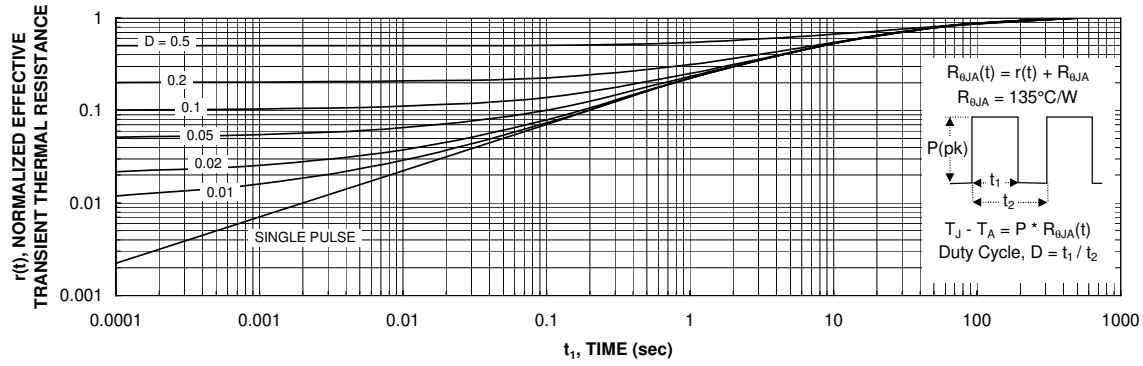



**Figure 21. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
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Rev. I76

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